

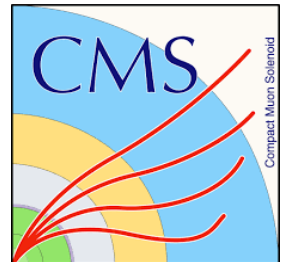
## A mass production test bench at few picoseconds timing resolution for the RAFAEL ASIC

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On behalf of the CMS CEA group



IRFU | CEA Saclay



# Outline

- Reminder, Timing distribution in LHC experiments
- Radiation tolerant fan-out ASIC for CMS experiment
- RAFAEL Specifications
- Characterization results
- RAFAEL test bench
- Production tests
- Outlook

# Reminder, Timing distribution in LHC experiments

## Context

Large Hadron Collider (LHC) : Common R&D project for Compact Muon Solenoid (CMS) phase 2 upgrades are currently underway for high precision clock distribution

## Target

Reach 30-50 ps time resolution with 10-15 ps jitter at the level of frontend



## Strategy

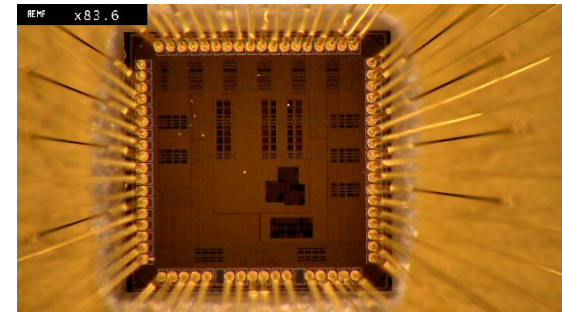
Two options for timing detector :

- LHC clock to each module encoded in control links (baseline)
- Dedicated clock (security solution)

## Need

Having a baseline solution with a fan-out ASIC :

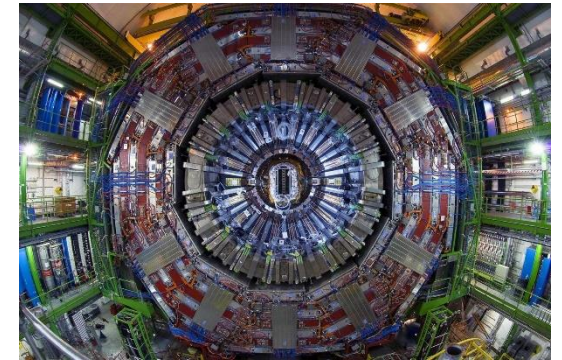
- For clock & data distribution
- Facilitate front-end design



# Radiation tolerant fan-out ASIC for CMS experiment

## RAFAEL

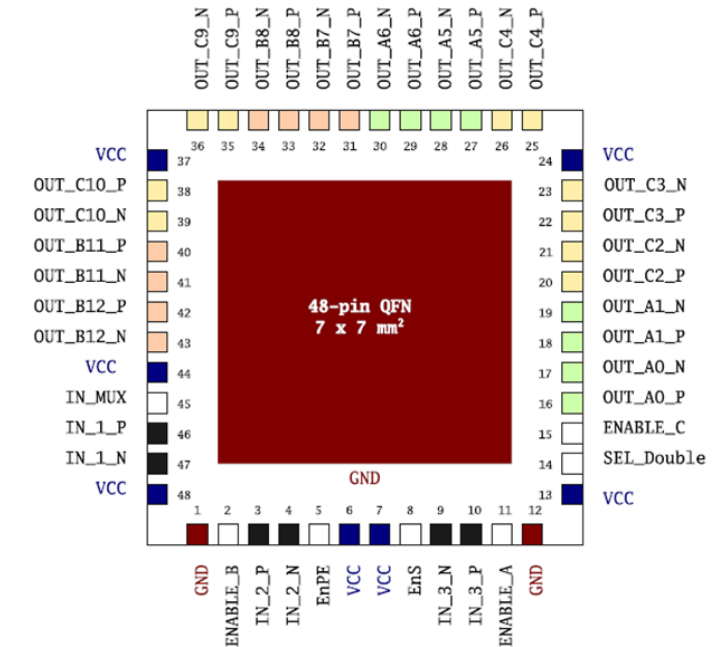
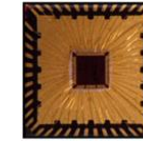
- **R**adiation-hard **F**an-out **A**ASIC for **E**xperiments at **L**HC
- Distribution of clock & fast command differential signals
- Frontend electronics of the precision timing detectors of CMS :
  - High granularity calorimeter (HgCal)
  - MIP timing detector (MTD) → Barrel timing layer (BTL)
- **CEA Saclay** has started designing RAFAEL since September 2019 :
  - ✓ ASIC original design from IRFU with IO IP block design from OMEGA
  - ✓ Test bench design and characterization at IRFU



# RAFAEL Specifications

## Main features

- **Package** => 7 mm x 7 mm 48-pin QFN
- **Technology** => 130 nm Node
- **Configurations** => single buffer or dual buffer
- **Fan-out factors** => 1:13 or (1:6 and 1:7)
- **Frequency range** => DC to 400 MHz
- **Output skew** => channel-channel : 50 ps & part-part : 300 ps
- **Pre-emphasis** settings per group of outputs => 1 mA, 2 mA.
- **Power supply voltage** => 1.2 V
- **Radiation hardness** => tolerant to 200 Mrad cumulative dose
- **Temperature range** => -30°C to +40°C guaranteed

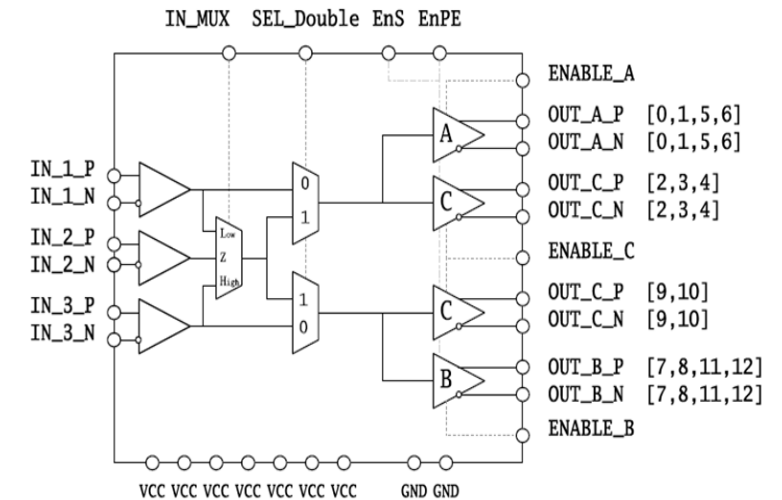


# RAFAEL Specifications

## Possible configurations

A buffer with **3 differential inputs** and **13 differential outputs** :

- **Single fan-out** distributing one of the 3 inputs to up to 13 outputs.
- **Two independent buffers** with fan-out factors of up to 6/7 resp.
- Control of the **Pre-Emphasis** current and the duration of the current boost (pins EnPE and EnS) :
  - Increase current during **rising/falling edges** to adjust bandwidth.
- Groups of outputs (A,B,C) can be activated / deactivated (depending on **ENABLE\_{x} input signal**) :
  - Select the desired **strength of the output drivers**.



# Characterization results examples

## BTL frontend use case

Main functions	Under experimental conditions
<ul style="list-style-type: none"><li>- 3 Inputs : 12 outputs + 1 return path</li><li>- Signal strength : 2mA / 1mA</li><li>- Pre-emphasis : +2mA / +1mA / OFF</li><li>- Pre-emphasis duration : variable</li></ul>	<ul style="list-style-type: none"><li>- Input signal : clock / data</li><li>- Frequency : 40 Mhz</li><li>- Temperature : 30°C</li><li>- Irradiation : 10 Mrad</li></ul>

- Single buffer input mux / fan-out buffer (up to 13 outputs)
- Redundant control via IpGBTs and on board GBT-SCAs
- Negligible effect on jitter

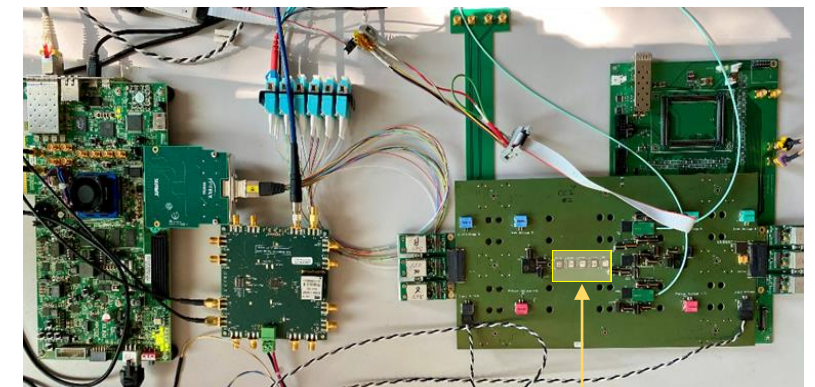
A nice summary of tests results by Fabrice Guilloux:

[2021-01-19\\_TID\\_Power\\_Rafael-V0.pdf \(cern.ch\)](#)

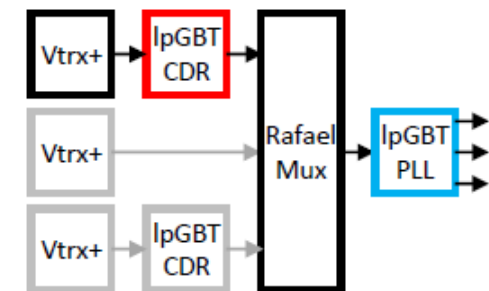
Updated by Irakli Mandjavidze:

[210601\\_Hptd\\_RafaelUpdate.pdf](#)

BTL clock distribution test using CCv2



RAFAEL ASIC



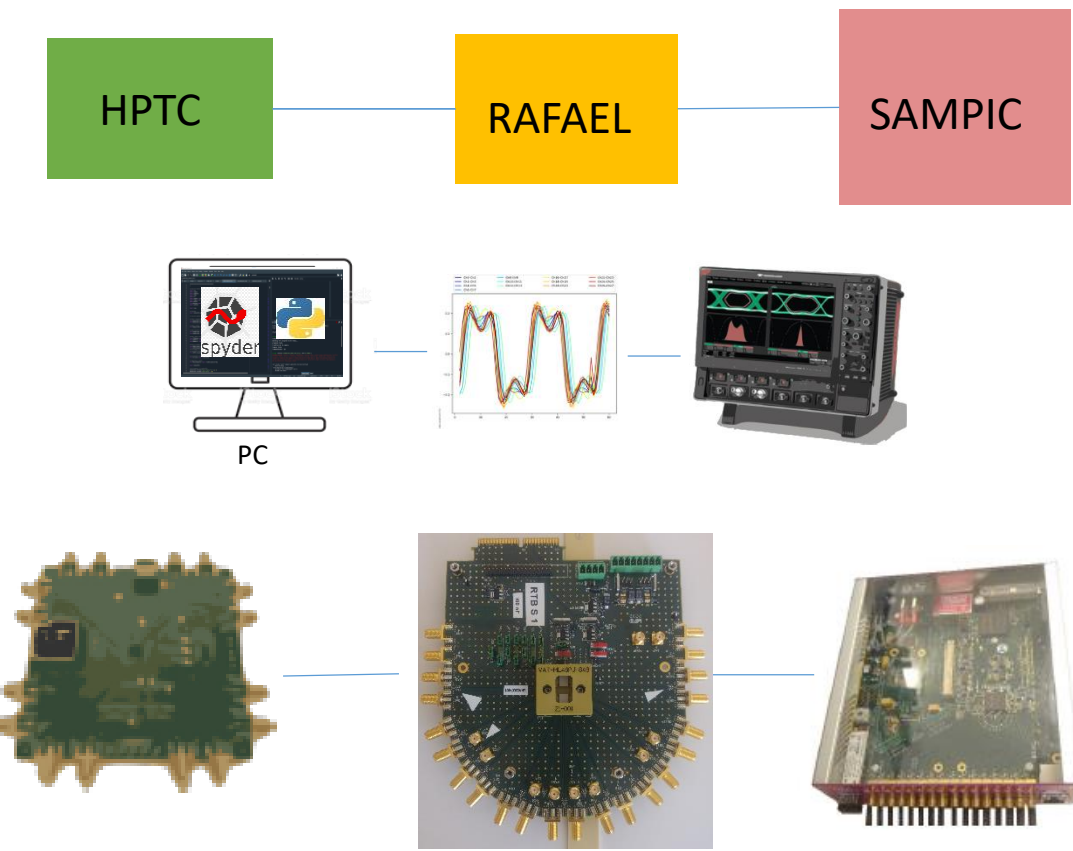






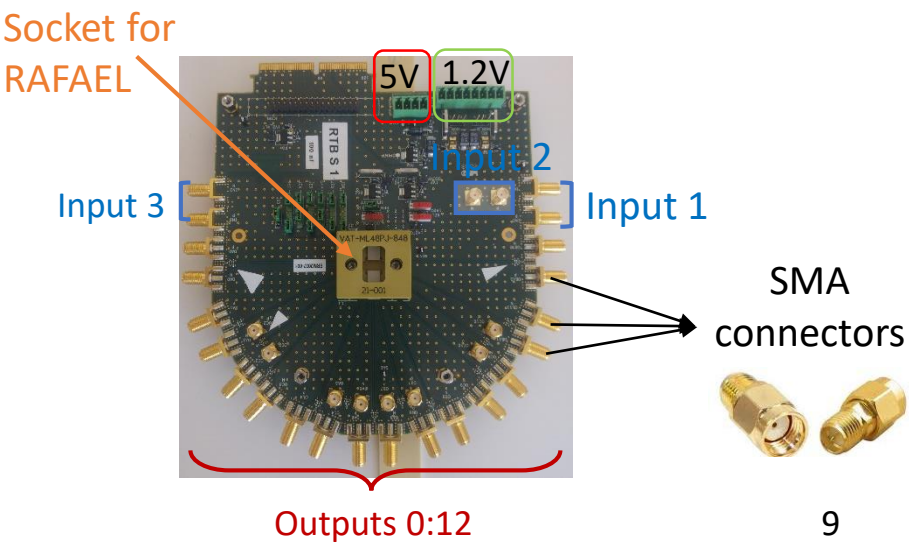
# RAFAEL test bench

## Test bench



Item	Specification
HPTC	40.079 MHz/ 160.316 MHz/ 320.632 MHz
Power supply	TTI MX100P 315W
Oscilloscope	Teledyne Lecroy SDA 820Zi-B (Up to 80 Gs/s) Precision timing measurement
SAMPIC	32 Channels Automated batch of various tests Acquired data analysis

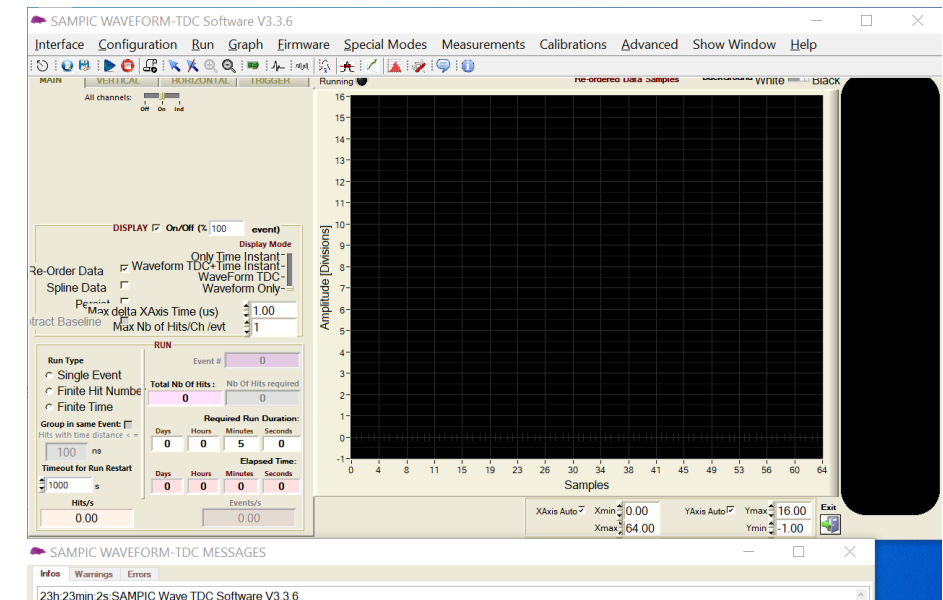
## Test board



# RAFAEL test bench

## SAMPIC

- SAMpler for PICOsecond time : picosecond time measuring system
- Divert SAMPIC module and DAQ system for the proper developpement of RAFAEL test bench
- Channel time resolution **3 – 5 ps rms**
- Use of almost all provided channels (**30/32 channels**)
- **Reconstruction** of differential signals from single-ended
- **Synchronous** measurement using HPTC clock as a reference
- Define acquisition system according to the **configuration file**



# RAFAEL Production

## In-house

Manual	Automated
<ul style="list-style-type: none"><li>- Fine characterization (BTL use case)</li><li>- Limited Asics (~10 units)</li></ul>	<ul style="list-style-type: none"><li>- Systematic validation</li><li>- Group of Asics ~1 k</li></ul>

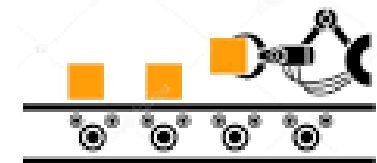
**Solutions proposed by industrials  
for mass production**

## Out-house

Manual	Automated
<ul style="list-style-type: none"><li>- Simple &amp; easy to use</li><li>- 10 – 100 k units</li></ul>	<ul style="list-style-type: none"><li>- Interfaced with tester robot</li><li>- Mass prod ~100 k</li></ul>

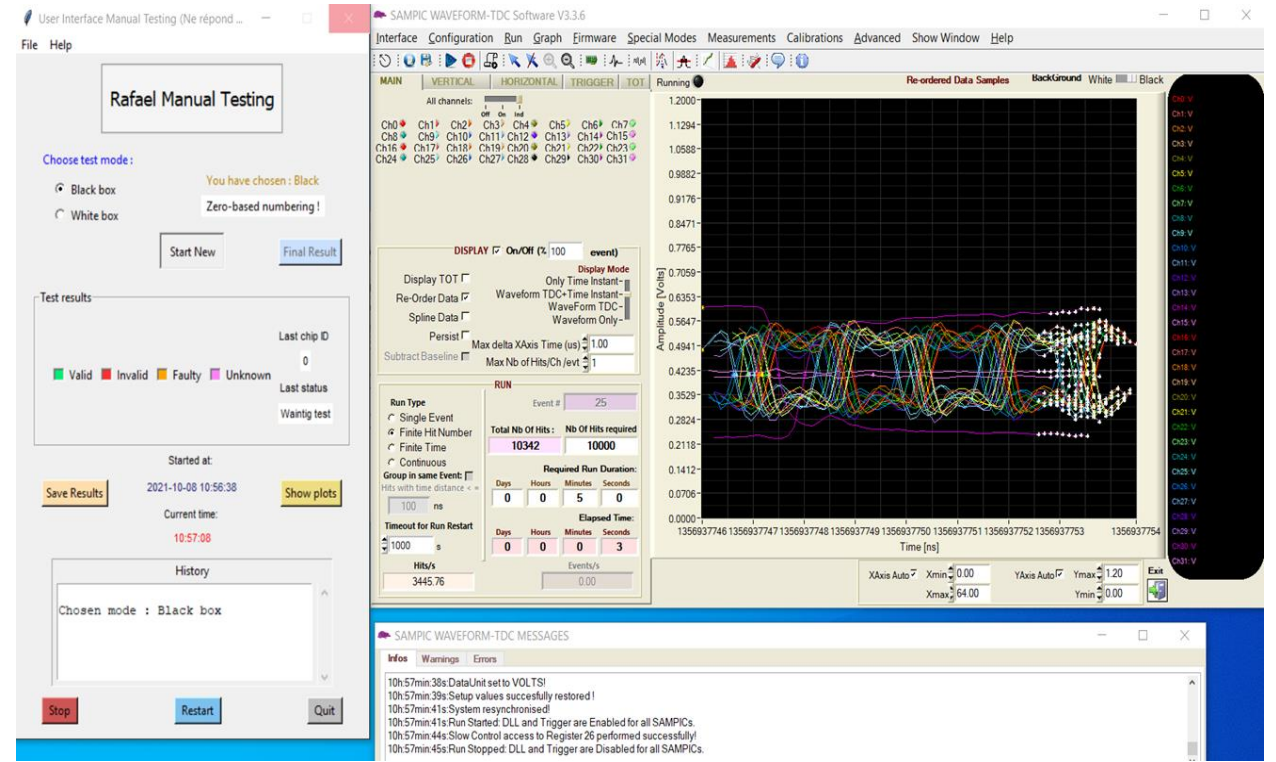
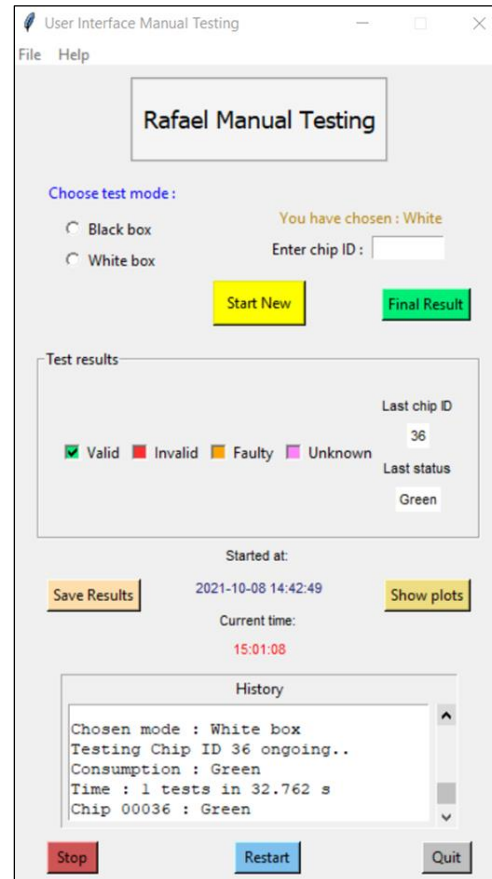
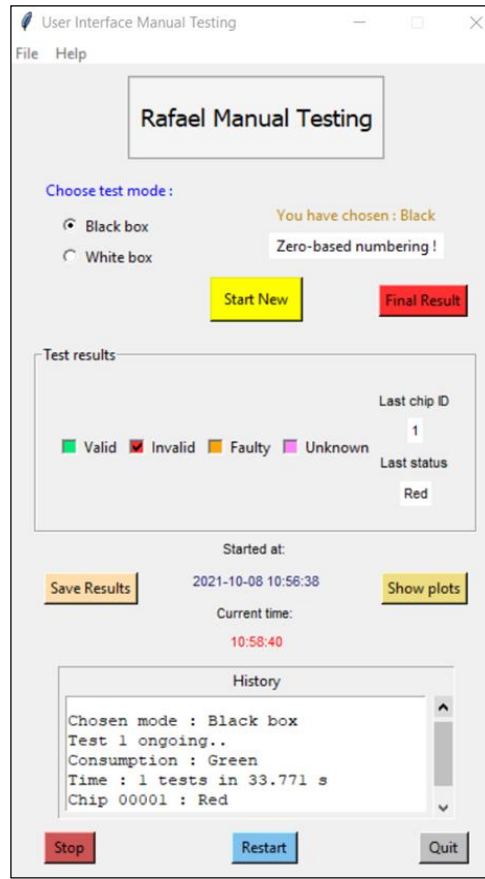
### Targets :

- Anticipating the final production
- Monitor and record data (DAQ)
- Rapid test (~1 min/Asic)



# Rafael Manual testing

## Graphical user interface (GUI)



Complete data acquisition and analysis system for RAFAEL

# In-house tests

## Overview

Total production about 45 000	
Use case	Number
<u>BTL</u> : single-buffer mux / fan-out	~ 2 500 ASICs
<u>HgCal</u> : double-buffer fan-out	~ 32 000 ASICs

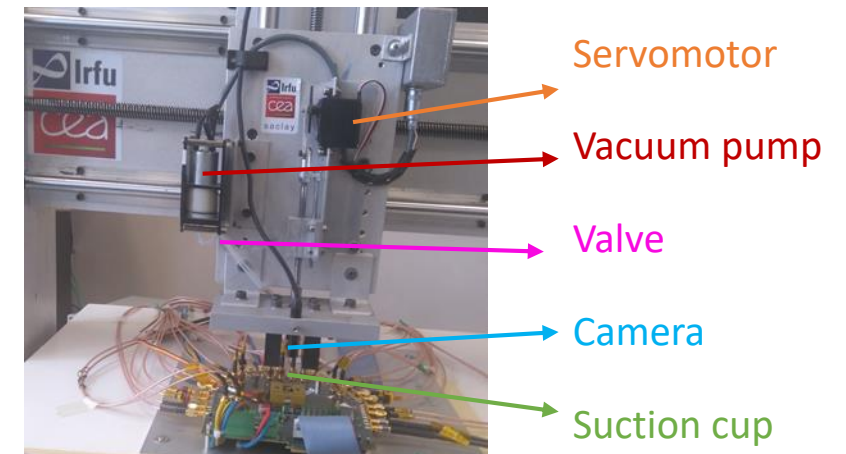
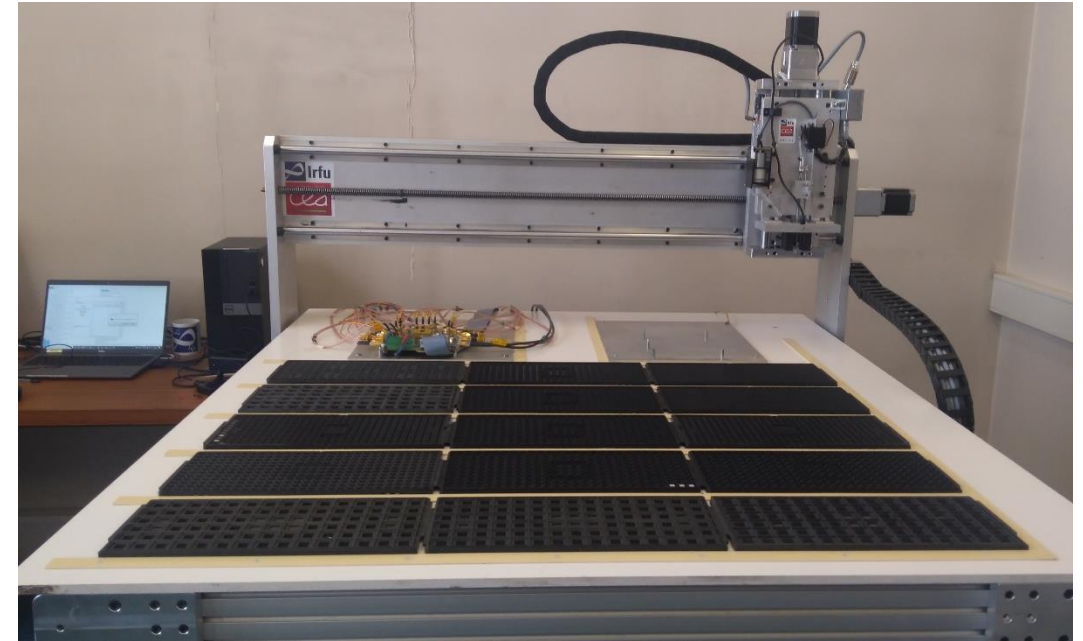
Systematic verification  
and testing

Use of the existant  
Lab robot

**Automated** process with ensuring good **interaction**

between different measurement systems

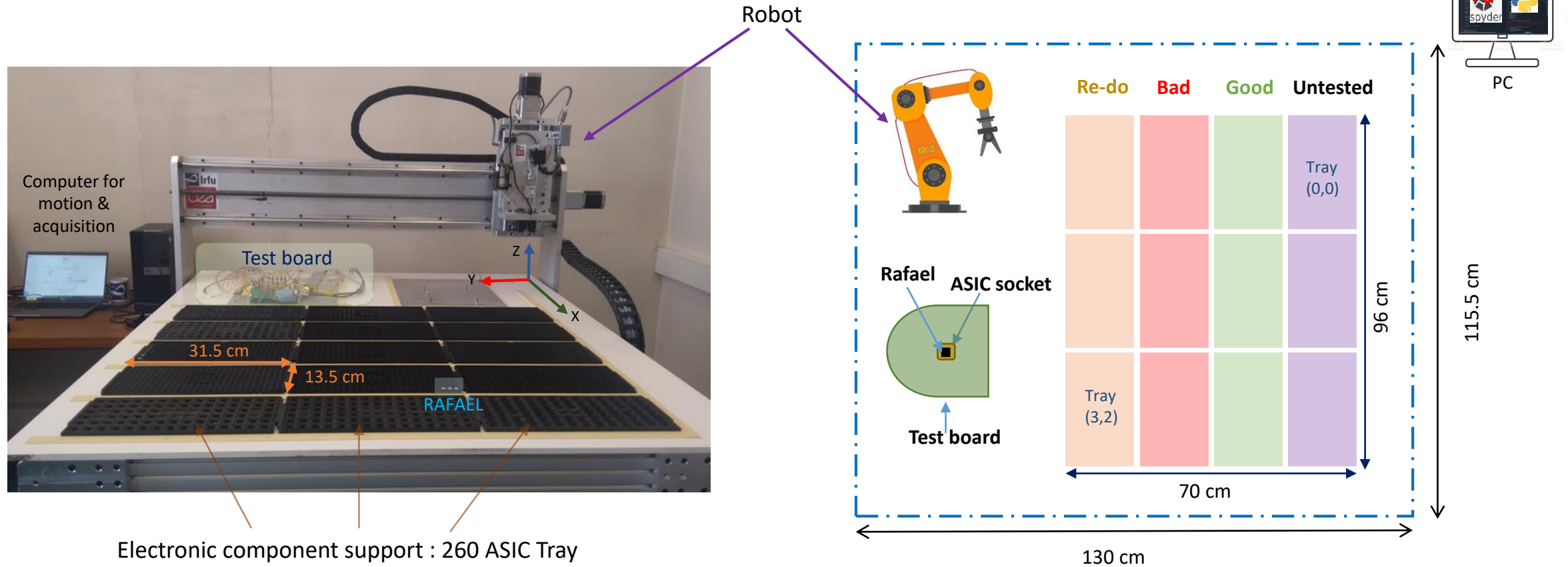
(Power supply/ Temperature sensor / SAMPIC)





# In-house automated tests

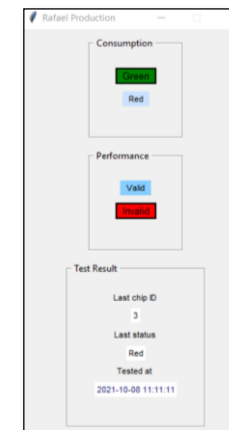
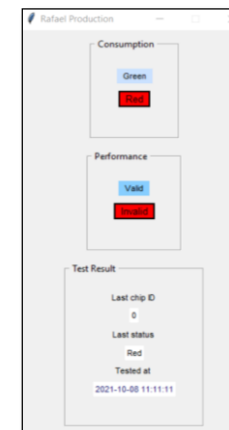
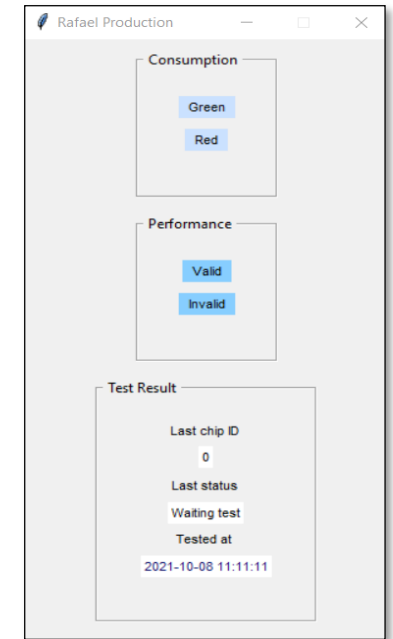
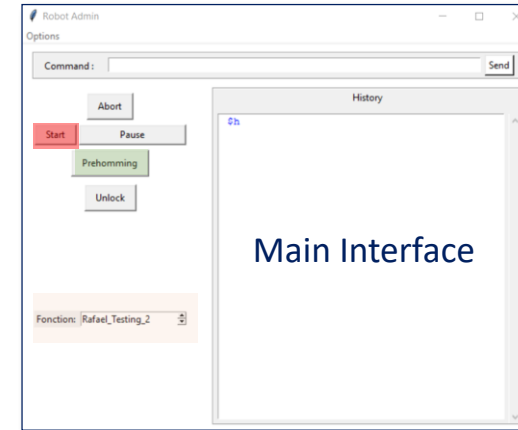
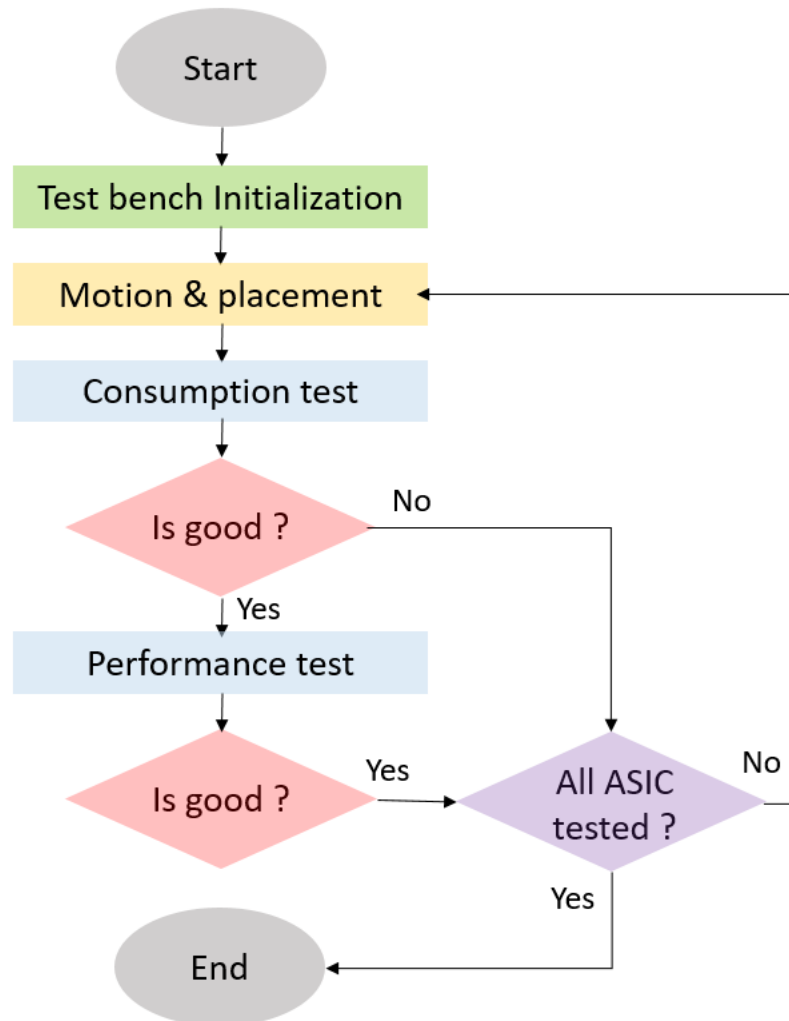
## Top view of the automated testing process



# In-house automated tests

## Mass production testing flowchart

Scripts en  
Python





# Outlook

- RAFAEL : **baseline** for clock & fast command distribution in **BTL** and **HgCal**
- RAFAEL clock distribution tests verified => desired **specification achieved**
- **Anticipate** final production → **~45 000** ASIC planned for **2022**
- Production validation **In-house** tests :
  - RAFAEL test bench → **DAQ** working fine & some mechanical **displacement** problems
  - **Manual** and **automated** production testing modes are ready
  - For **statistics** purposes and choosing final acceptance criteria
- **Out-house** production :  
**User-friendly** interfaces → simple & rapid

**THANK YOU**

**FOR YOUR ATTENTION**

# Backup



# BTL clock distribution tests using CCv2 board

## Performance testing of the embedded clock distribution

