

## SYSTEMES DE MESURE DE TEMPS À LA PICOSECONDE A BASE DU CIRCUIT SAMPIC



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# INTRODUCTION PHILOSOPHIQUE

- Je voudrais **mesurer le temps de façon très précise**
- J'ai un nombre **assez important de voies** ...
- J'ai un **taux d'acquisition par voie** qui est **raisonnable** ...
- Je ne veux pas dépenser beaucoup d'argent ...
- ...et je souhaiterais vraiment voir **la forme de mes signaux** ...



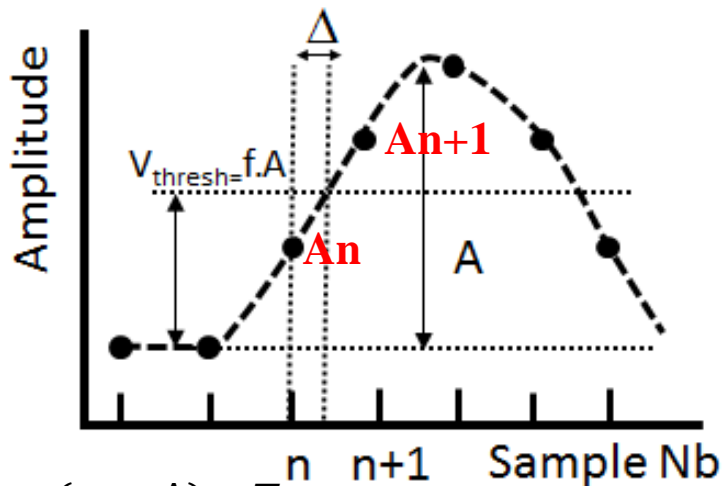
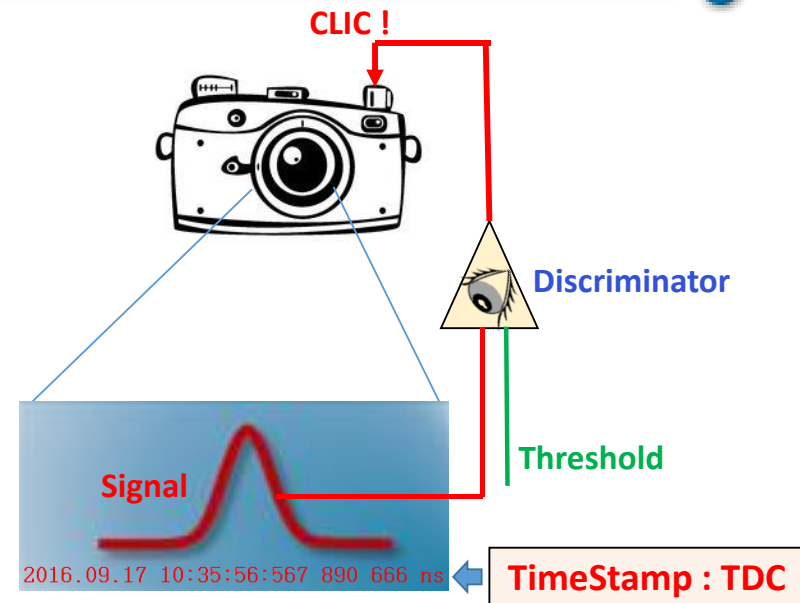
Un compromis serait un **TDC** qui  
**fournit juste la partie**  
**intéressante de la forme d'onde**  
**du signal** ...



# CONCEPT DU “WAVEFORM TDC”

**WTDC**: a TDC which also permits **taking a picture of the real signal**. This is done via sampling and digitizing only the interesting part of the signal.

Based on the digitized samples, making use of **interpolation** by a digital algorithm, fine time information will be extracted.



$$t_0 = (n + \Delta) * T_s$$

$$\text{with } \Delta = \frac{f * A - A_n}{A_{n+1} - A_n}$$

## Advantages:

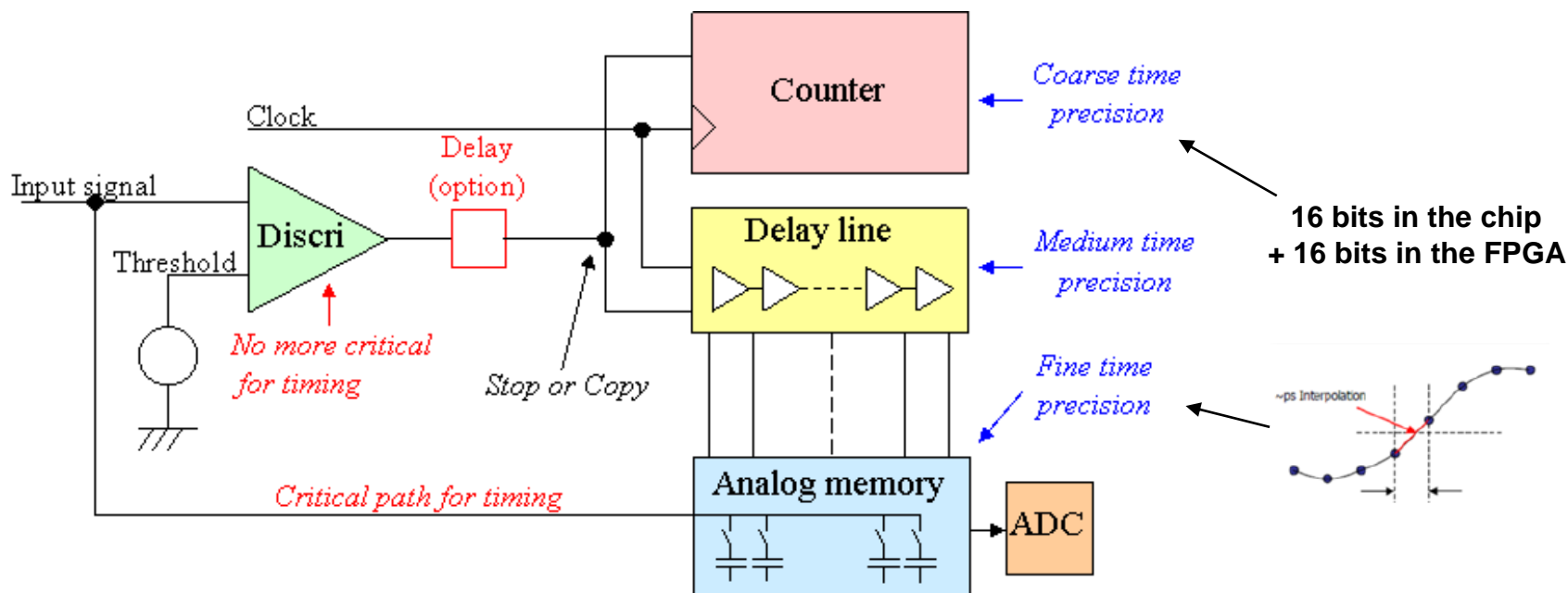
- Time resolution ~ **few ps rms**
- **No “time walk” effect**
- Possibility to extract other **signal features**: charge, amplitude...
- **Reduced dead-time...**

## But:

- waveform conversion (**200 ns to 1.6 μs**) and readout times are fast but don't permit counting rates as high as with a classical TDC

# STRUCTURE D'UN WAVEFORM TDC

- Mix of DLL-based TDC and of analog-memory based Waveform Digitizer
- The TDC gives the time of the samples and the samples give the final time precision after **interpolation** => **resolution of a few ps rms**
- Digitized waveform gives **access to signal shape...**
- Conversely to TDC, discriminator is used only for triggering, **not for timing**



# ARCHITECTURE GLOBALE DE SAMPIC



**One Common servo-controlled DLL:** (from 0.8 to 10,2 GS/s)  
 used for medium precision timing & analog sampling

**One Common 16-bit Gray Counter** (FClk up to 160MHz) for **Coarse Time Stamping (TS)**.

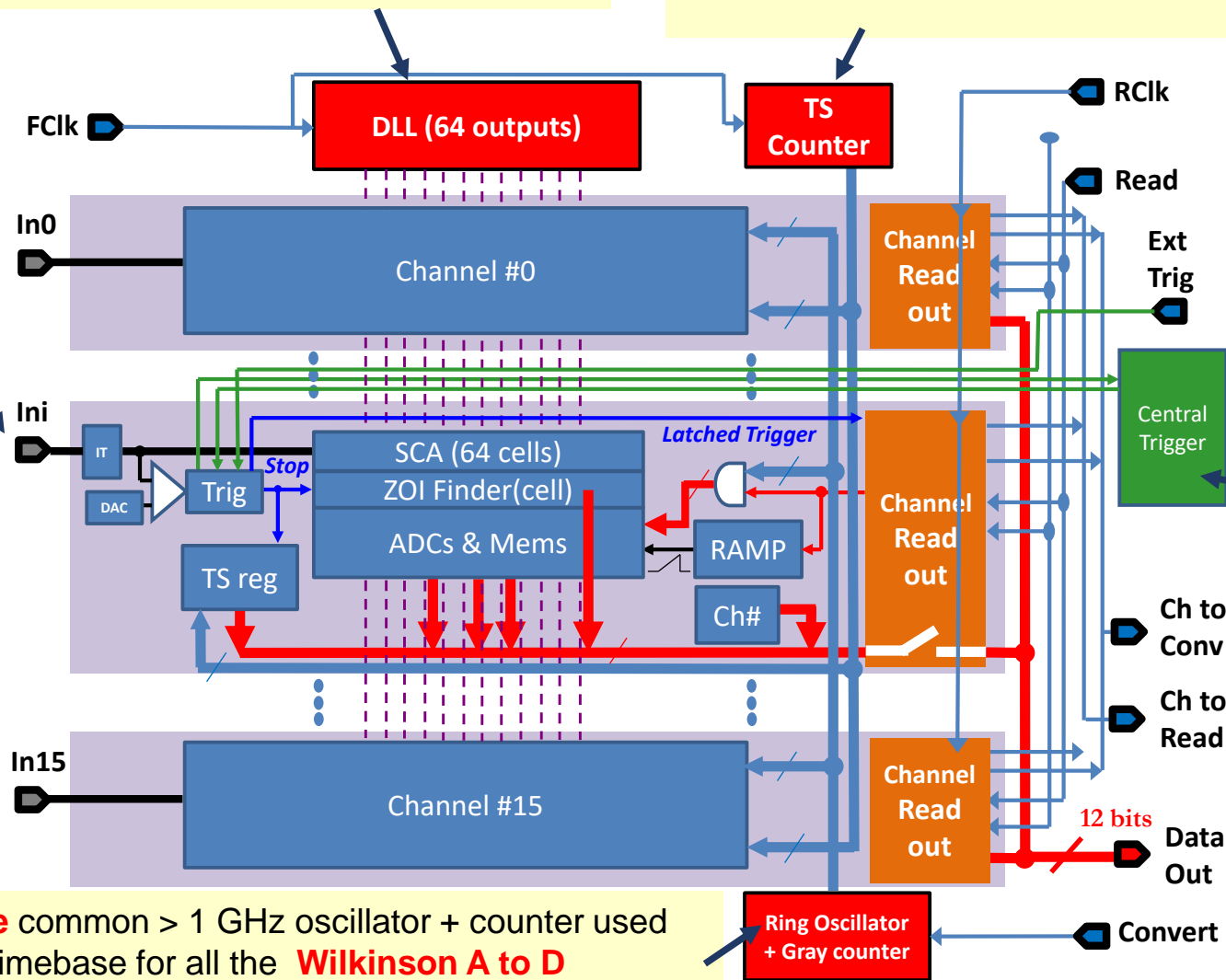
**16 Channels,**  
 each with:

-1 discriminator for self triggering

-Registers to store the timestamps

- 64-cell deep SCA analog memory

- 11-bit ADC/ cell  
 (Total : 1024 ADCs)

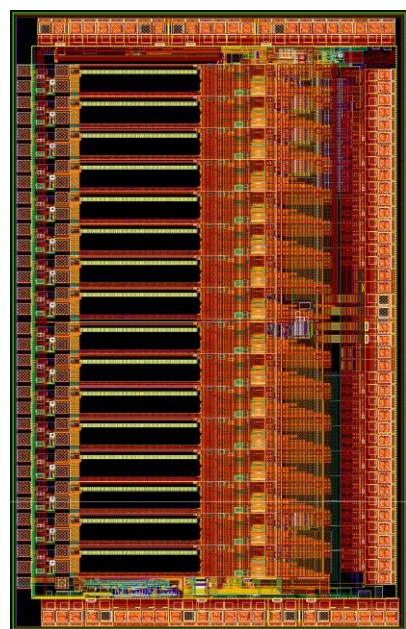
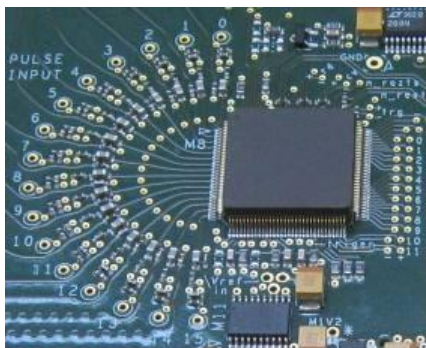
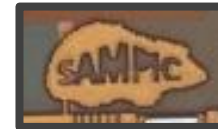


**SPI Link**  
 for Slow  
 Control

**One**  
 Central  
 Trigger  
 block

**Read-Out interface:**  
 12-bit  
 LVDS bus  
 running  
 at > 160  
 MHz (> 2  
 Gbits/s)

**One common > 1 GHz oscillator + counter** used  
 as timebase for all the **Wilkinson A to D**  
**converters.**



SAMPIC V5  
 (TSI 0,18μm technology)

- Till Version V3D (V4) Technology: **AMS CMOS 180nm** (Surface: 8 mm<sup>2</sup>, Package: QFP 128 pins, pitch of 0.4mm )
- Most produced version is **V3D** (should have been called V4) submitted in **December 2017** but received only in **January 2019**
- 1300 chips have been packaged in 128-pin plastic TQFP package
- Due to the (temporary ?) stop of the CMOS 0.18μm technology at AMS, we looked for equivalent ones.
- **TSI Microelectronics** is also proposing his own version of the former IBM CMOS 0.18μm technology, with some rule differences with AMS on the top metal layers.
- **We migrated** the design to TSI technology => **SAMPIC\_V5**.
- We took benefit of this new submission for improving some historical weaknesses (sampling at **10.2 GS/s**, first sample, linearity of posttrig delays, internal calibration of ADC, version register, ...)
- We also designed a **second version dedicated to slower sampling**, covering the range **between 350MS/s and 2GS/s**. → **SAMPIC VSlow**
  - Fully pin to pin compatible. Only difference is the **main clock frequency**.
- Both versions submitted in **January 2021**. Back in **May** (very effective work of TSI), packaged **end of May** and **worked very well**.

## ➤ Triggering:

- **Self-Trigger**
- **Central Trigger:** (OR, multiplicity of 2 & 3) with possibility of **common deadtime** or selecting **only channels** participating in decision.
- **Channel chained** : (to previous one)
- **“Ping-Pong” or Toggling Mode:** channels work in pairs.
- **PostTrig** (8-step full window very useful for low frequencies)
- **TOT-Filter** : events are rejected based on the TOT value.

## ➤ Measurements:

- **TOT** : based on the signal of the discriminator
- **ADC conversion** (selectable between 7 and 11 Bits)
  - **Auto-Conversion** : conversion automatically started when an event is detected, independently for each channel.
  - **Handshake with FPGA** : permits building **2<sup>nd</sup> and 3<sup>rd</sup> Level triggers** based **on many chips or boards** for a common event selection

## ➤ AUTO Calibration :

- Dedicated signal sources are implemented in the chip in order to perform **time INL calibration** in standalone and **ADC calibration**.

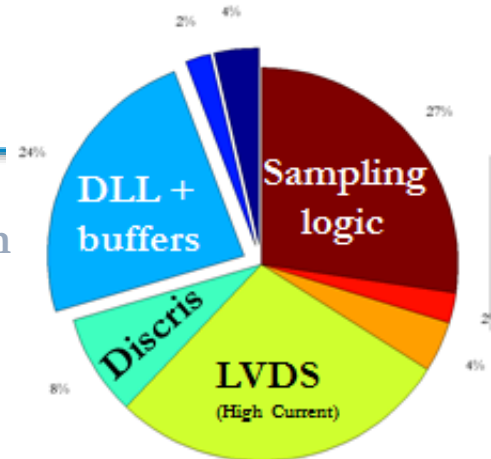
## ➤ Integrated DACS: all necessary DACs for controlling the chip are integrated (current ramp for ADC, Ring Osc, TOT etc...)

# PERFORMANCES GLOBALES

## SAMPIC V3 – V5

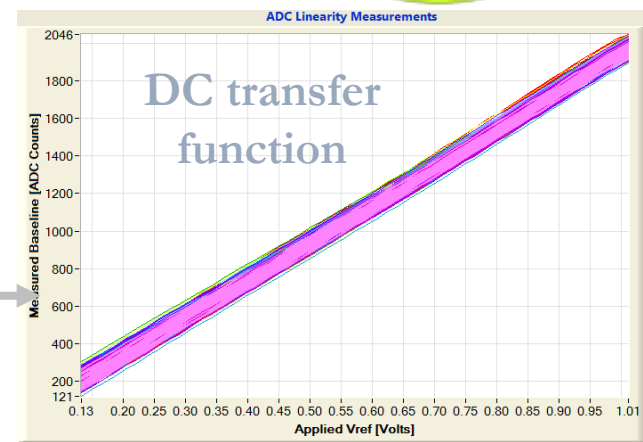
- Power consumption: **~10mW/channel**
- 3dB bandwidth > **1 GHz**
- Sampling rate up to **8,5 (10.2) GS/s**
- Discriminator noise **~ 2 mV rms**
- Counting rate > **2 Mevts/s** (full chip, full waveform), up to 10 Mevts/s with Region Of Interest (ROI)

Power distribution



### Wilkinson **ADC conversion** @ **~1 (1,45) GHz**

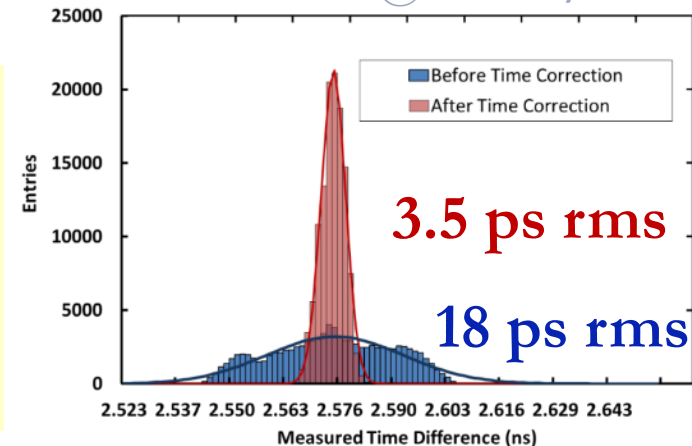
- Dynamic range of **1V**
- Gain dispersion between cells **~ 1% rms**
- Non linearity < **1.4 %** peak to peak
- After correction of each cell (linear fit): noise = **0.7 (10GS/s) to 1.3 mV rms (1.6 GS/s)**



### Time Difference Resolution (TDR):

- Raw non-gaussian sampling time distribution due to DLL non-uniformities (TINL)
- Easily **calibrated & corrected**
- TDR goes from **~ < 5 (10GS/s) to ~18 ps rms (1.6 GS/s)**

Ex: TDR @ 6.4 GS/s



## ➤ **Integration**

- Connectors for fast and numerous analog signals, crosstalk
- Number of components on board

## ➤ **Calibration**

- **Clock distribution and Synchronization** : inside module/crate, and between systems.

## ➤ **Triggering**

- Coincidences, Comb logic, External Trig → System Level
- Self-triggering → Buffers become full → potential loss of hit correlation

## ➤ **Data Acquisition**

- Software/ Libraries → plug and play for physicists!
- Data Saving to disk

# SYSTÈMES SAMPIC: LES MODULES 16 À 64 VOIES

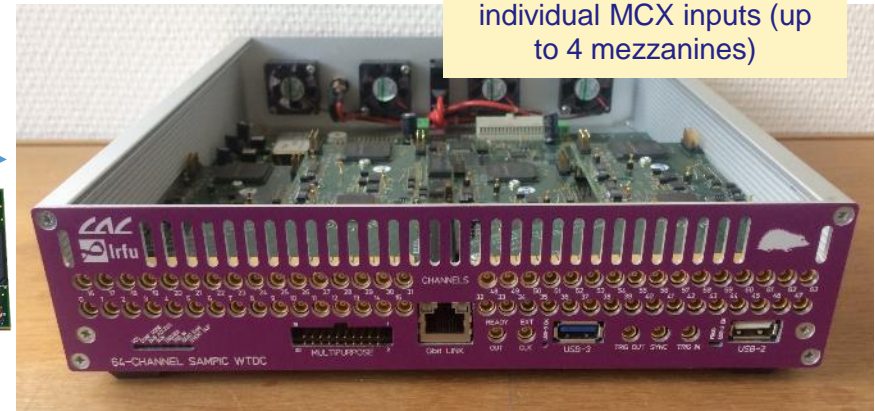
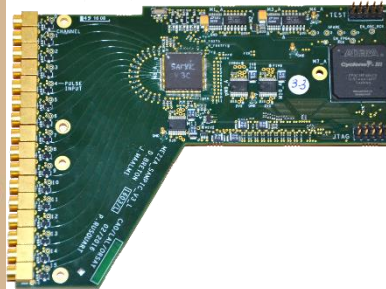
- **16-, 32-, 48- and 64-channel** modules are based on motherboards (2 o 4 slots) and 16-ch daughter boards.
- Motherboard: synchronization, triggering, and acquisition.
- Daughter-board: Front-End Interface with SAMPIC
- Acquisition through **Gbit Ethernet UDP** (RJ45 or Optical), **USB2 → USB3**

16 or 32-channel module  
(1 or 2 mezzanines)

16-channel mezzanine

64-channel module with  
individual MCX inputs (up  
to 4 mezzanines)

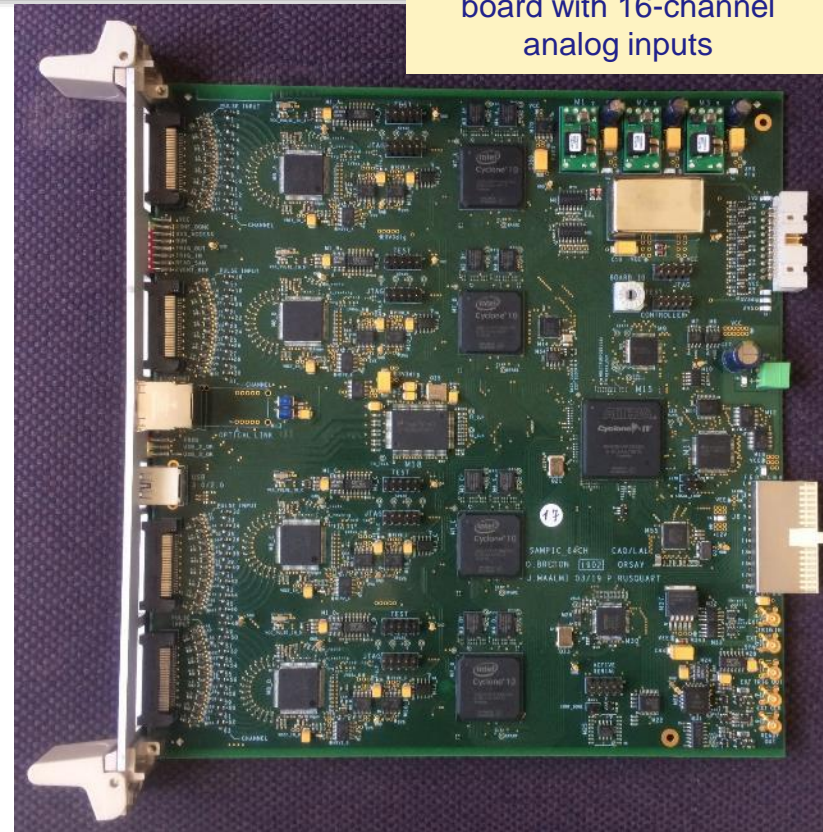
64-channel module with 16-  
channel input connectors  
(can be analog or  
differential digital)



# LE CHASSIS SAMPIC 256 VOIES

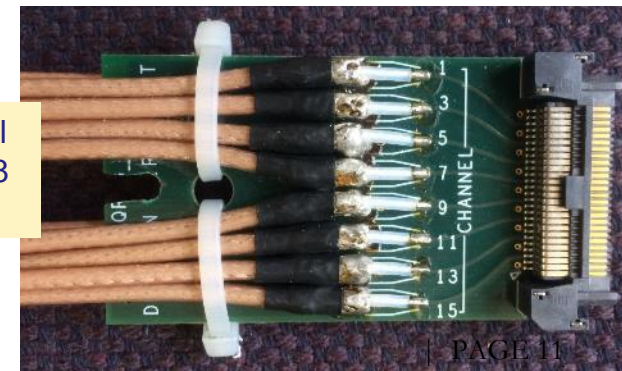
- In order to build systems with more channels, a **64-channel board** has been developed.
- It makes use of **SAMTEC QRF8** 16-channel connectors (very low crosstalk) for analog inputs
- **256-channel mini-crates** (standard and compact versions) have also been developed based on this new board.
  - A new control and DAQ software has been developed together with a C library
- Central **Control Board** permits smart **3<sup>rd</sup> level triggering** and acquisition through **Gbit Ethernet UDP** (RJ45 or Optical), **USB2 ( → USB3?)**
- Time difference resolution at crate level remains **of the order of 5ps rms.**

64-channel integrated board with 16-channel analog inputs



256-channel crate

16-channel coaxial to SAMTEC QRM8 interface board



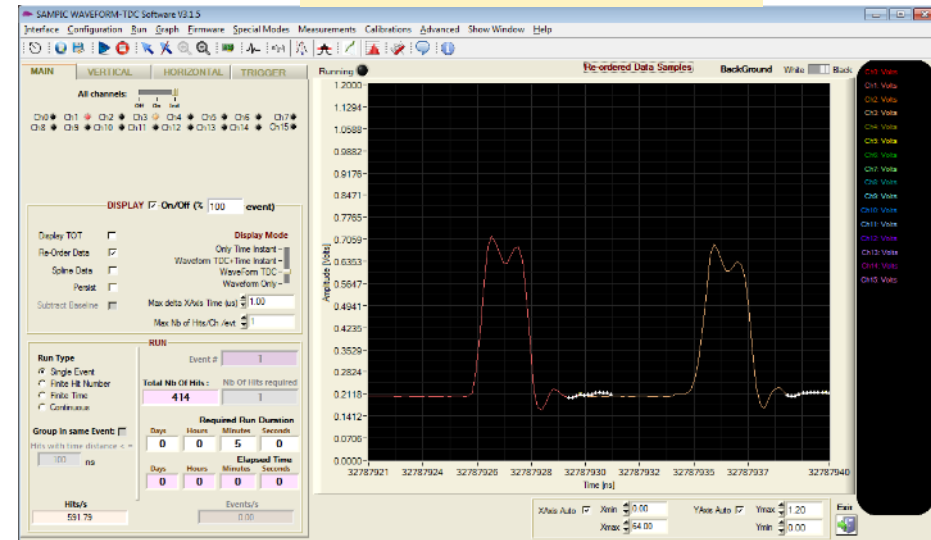
# ACQUISITION SOFTWARE

## Main panel

- An acquisition software has been developed up to 64 or 256 channels (also C libraries)

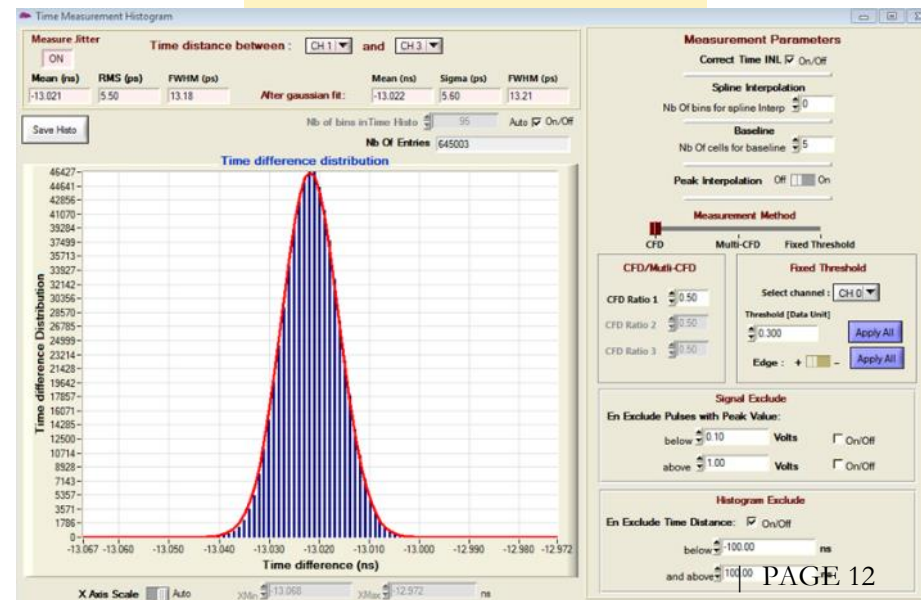
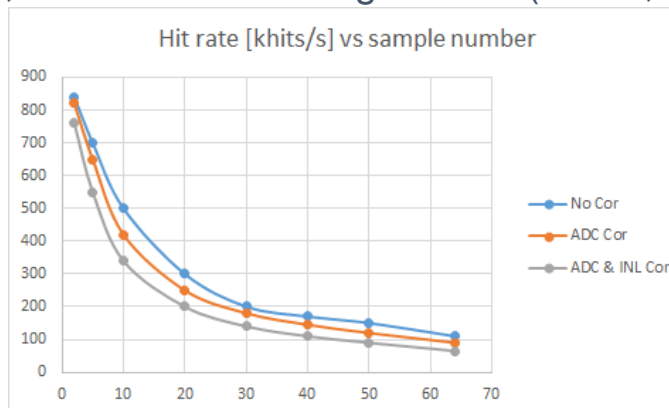
=> full characterization of the chip & modules

- Special display for **WTDC mode**
- Data saving on disk.
- Currently used by all SAMPIC users.
- A smart panel dedicated to time measurement is available. It permits selecting the parameters used for **extraction of time**

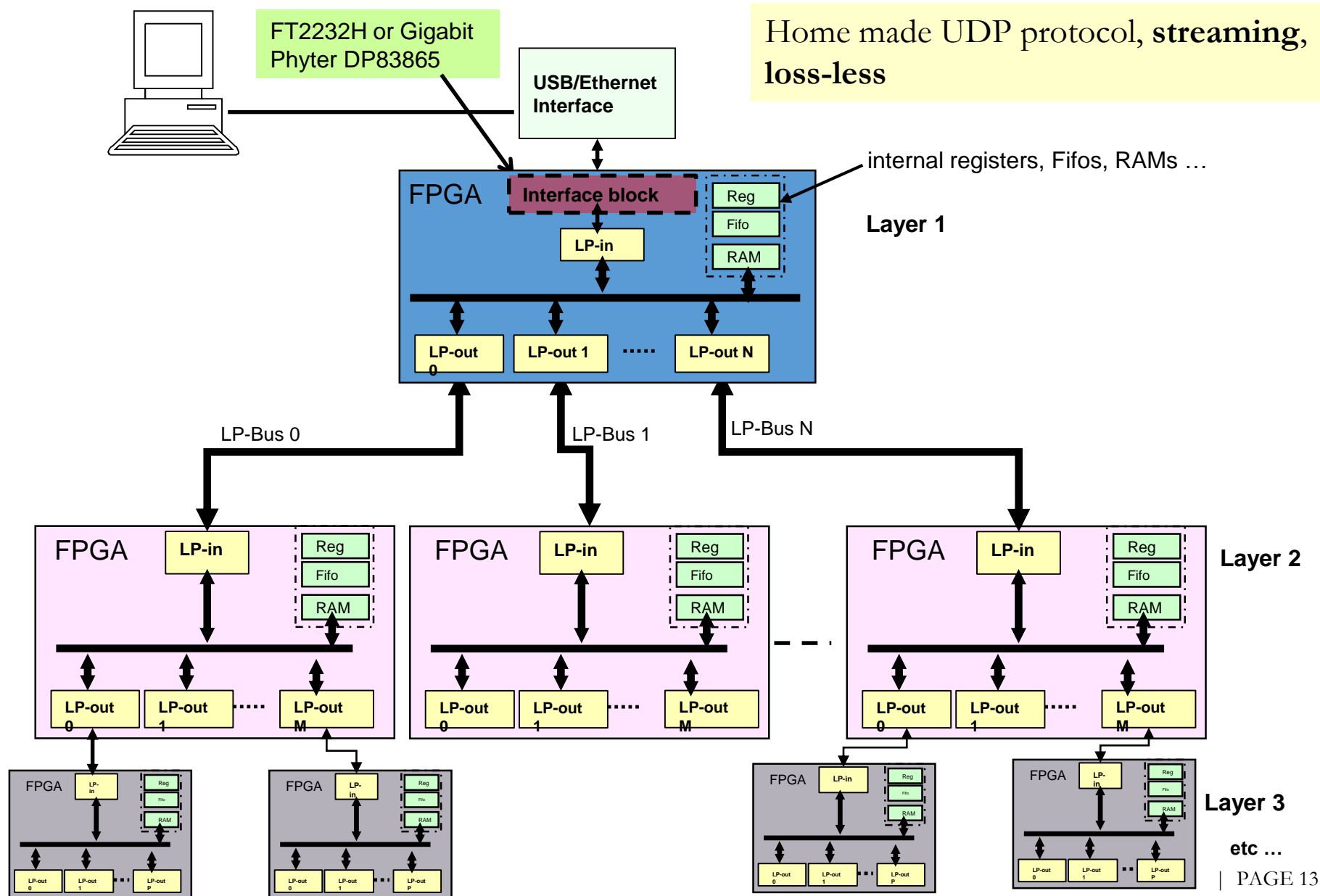


## Time Measurement panel

- Recorded hit rate** depends on: the number of waveform samples, the corrections applied (ADC, Time INL), the mode for saving on disk (ASCII, binary)...



# PROTOCOLE MULTI-LAYER POUR LE CTRL/DAQ



Different Calibrations are needed for SAMPIC :

➤ **ADC calibration:**

- Current Ramp: DAC inside the chip → automated calibration.  
→ defines **number of bits** of the conversion (7 to 11 Bits).
- Transfer function : **gain** and **offset** of each Wilkinson ADC converter
  - Need to **vary input signal**
  - External DAC for the Baseline on the board
  - **Internal DAC** for internal Calibration injected on the input

➤ Trigger Threshold Offsets: DAC inside the chip → automated calib

➤ **Time INL calibration:**

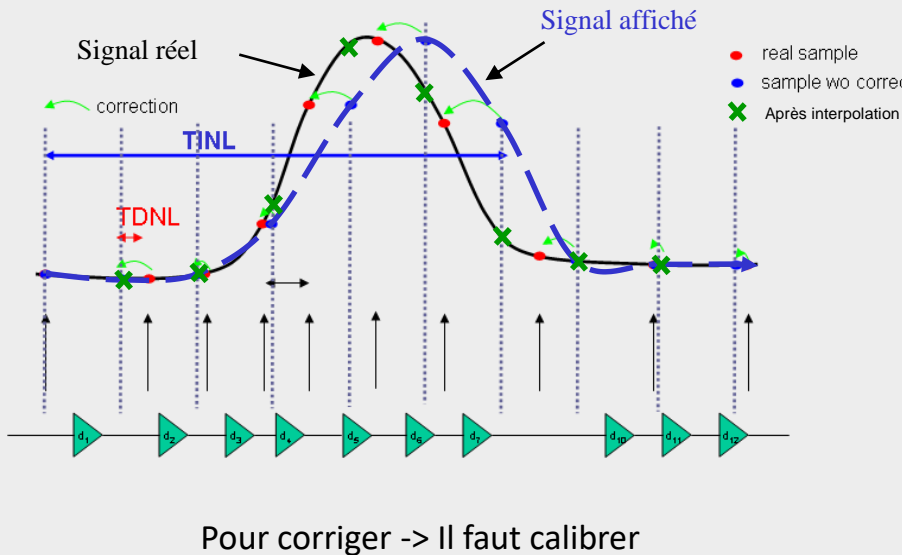
- Need external sinewave generator : best results but fastidious
- **Internal Oscillator** for time INL calibration → automated calib

➤ **TOT measurement** calibration : needs **pulse** with **variable width**.

Special **INPUT Block**, with **Bypass switch** to inject DAC for **internal ADC calibration** or asynchronous Oscillator for **internal Time INL calibration**.

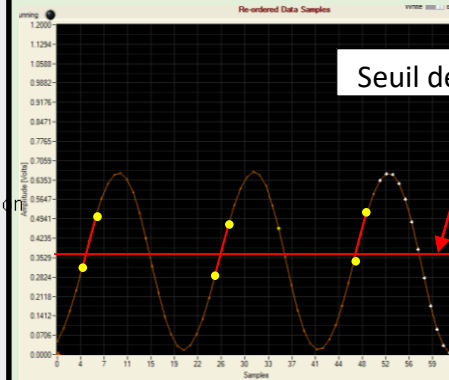
# CALIBRATION DE L'INL EN TEMPS

## Effet de non linéarité de l'échantillonnage

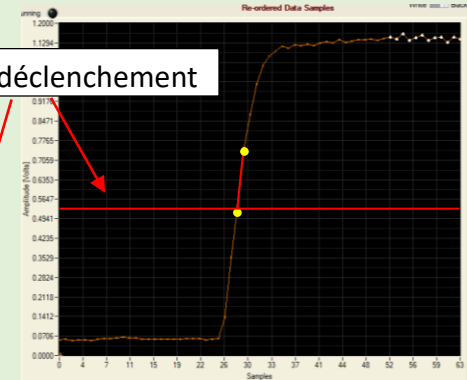


## La calibration:

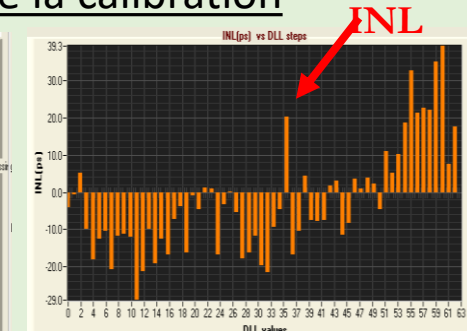
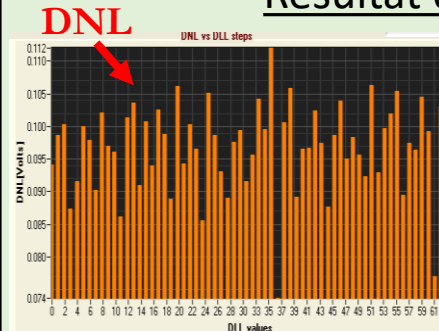
### Signal Externe



### Signal généré par SAMPIC



## Résultat de la calibration

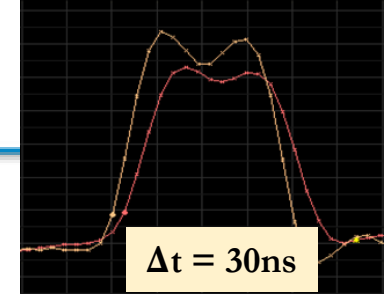
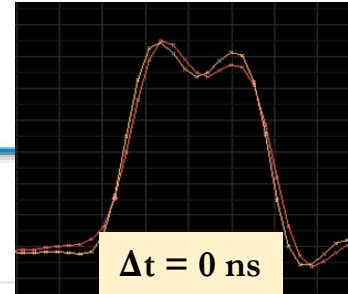
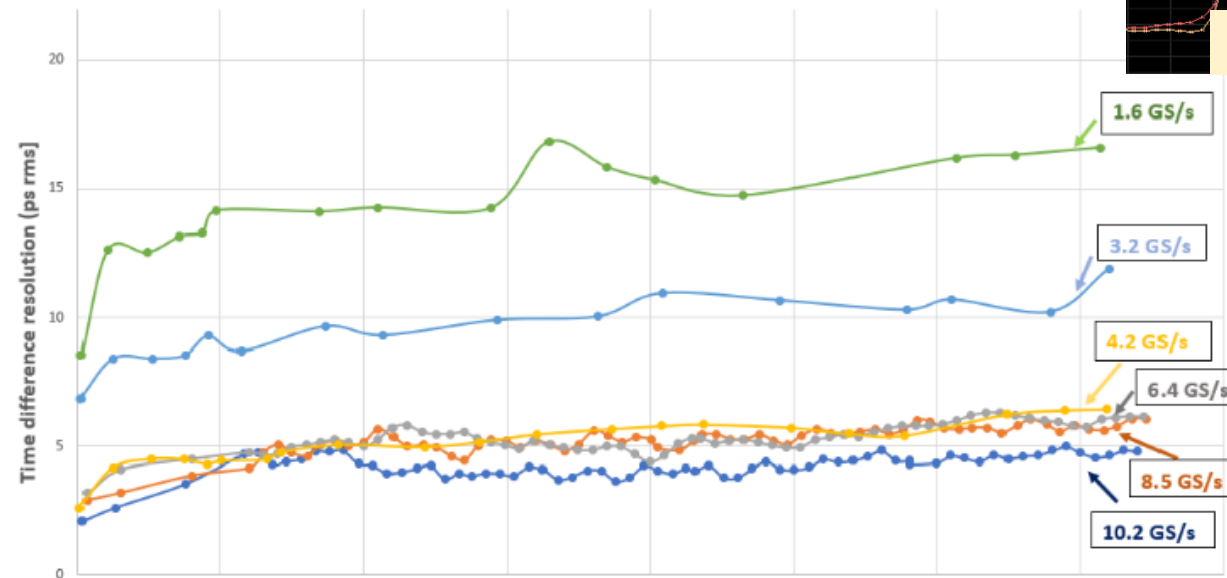


**Calibration Externe :** - très bonne correction d'INL mais fastidieuse, non envisageable à grande échelle.

**Calibration Interne:** - moins bonne correction mais peut être automatisée par Soft.

# TIME RESOLUTION

TDR with external calibration

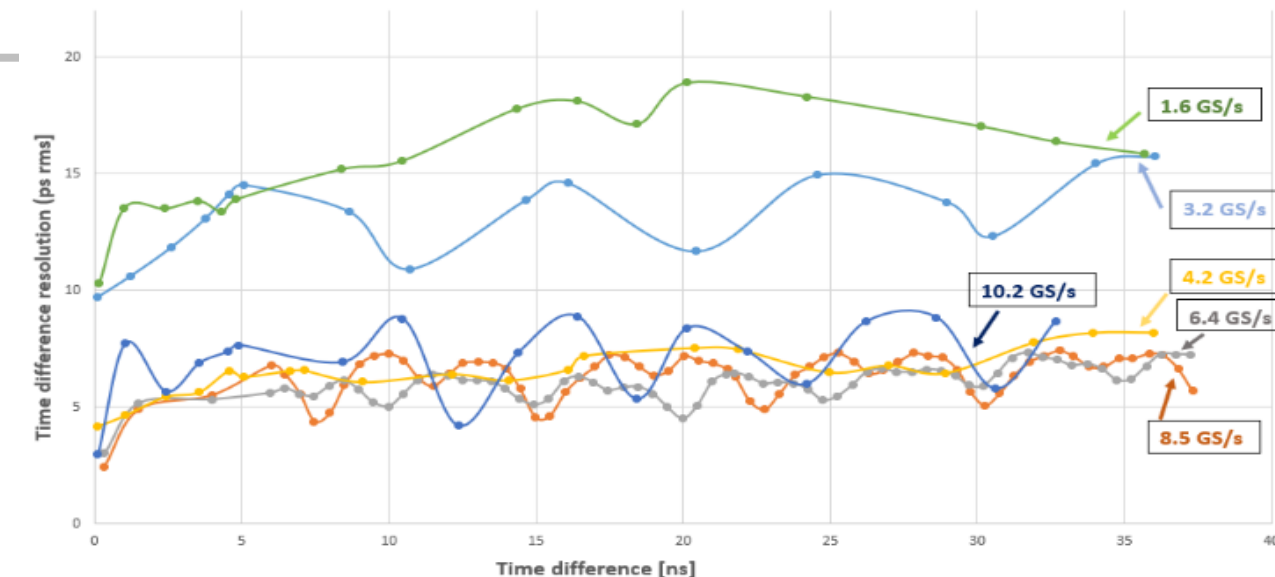


Delays for measurement made by a **cable box**: rise time degrades with delay

With **external time-calibration** :

- **TDR of ~5 ps rms** for  $4.2 < F_s < 8.5$  (**10,2**) GS/s
- **TDR < 10 ps rms** for 3.2 GS/s
- **TDR < 18 ps rms** for 1.6 GS/s

TDR with internal calibration



With **self-calibration**

- Limited jitter degradation (~20%)
- Permits **full integration** in **compact detection systems**

# NEED FOR EVENT FILTERING...

- Whatever the application, it is mandatory to find ways to **reject the wrong events** as early as possible in the readout chain in order to **keep the dataflow at a reasonable level**.
- Like a standard TDC, the Waveform TDC is natively **self-triggered** on each of its channels. This may produce very **large hit rates**, which may cause a **saturation of the output buffers**, especially since the **waveforms** have to be extracted (partially or in totality) together with the **time** information.
- In order to reduce the dataflow, it is necessary to **filter the good events before conversion**. A **central trigger located in the ASIC** can then help defining trigger conditions and drastically reducing the hit rate.
- Moreover, providing the adequate signals out of the chip permits performing in the surrounding **FPGAs a second and third level trigger** (depending on systems) based on smarter detector conditions and **increasing the counting noise rejection** by a huge factor.
- Noise filters can also be based on the characteristics of the signals as produced by the different detectors. For instance, a **real time filter based on the TOT \*** has been implemented in SAMPIC. When used with signals issued from crystals and SiPMs, it permits **rejecting above 99%** of the dark count noise from the SiPMs.

# TRIGGER IN 256-CHANNEL SYSTEM

A powerful and fully configurable trigger scheme has been implemented in the 256-channel system

Panel for L1 TRIGGER  
(each FE board)

MAIN VERTICAL HORIZONTAL EXT & L3 TRIG L2 TRIG L1 TRIG TOT

ALL FEBs

**Select Front-End Board High Level Trigger Option**  
 FEB High Level Trigger (FEB HLT) is: L2 ☐ L3 ☐

**Enable/Disable SAMPIC High Level Trigger:**  
 (to select High Level Trigger enable Build L2 (and L3))

SAMPIC 0 HLT OFF ☐ ON ☐   
 SAMPIC 1 HLT OFF ☐ ON ☐   
 SAMPIC 2 HLT OFF ☐ ON ☐   
 SAMPIC 3 HLT OFF ☐ ON ☐

ALL SAMPICs

**Channel Trigger Parameters**  
 All Channels

**Channel Trigger Mode**

☐ Self Trigger  
☐ External Trigger  
☐ Central Trigger  
☒ Chained to previous Channel

Internal Threshold (relative to Baseline)  
 0.600 1.000  
 0.400 1.400  
 0.200 1.600  
 0.000 1.800  
 0.000  
 Edge ☐ ☐ ☐

**SAMPIC Central Trigger Parameters**

**Central Trigger Type**

☒ Central  
☐ Triggered CHs >= 2  
☐ Triggered CHs >= 3

**Central Trigger Effect:**  
 Only if participating to CT ☐ Trig All Channels ☐

**Primitive Source:**  
 Raw Discr ☐ Gated Discr ☐

Channels Primitives Gate Length: 0 x 1/8 Clk Period = 0.00 ns

**Central Trigger Channel Sources:** All channels

Ch0 ☐ Ch1 ☐ Ch2 ☐ Ch3 ☐ Ch4 ☐ Ch5 ☐ Ch6 ☐ Ch7 ☐  
 Ch8 ☐ Ch9 ☐ Ch10 ☐ Ch11 ☐ Ch12 ☐ Ch13 ☐ Ch14 ☐ Ch15 ☐

Panel for L2 TRIGGER  
(each FE board)

MAIN VERTICAL HORIZONTAL EXT & L3 TRIG L2 TRIG L1 TRIG TOT

Enable Build Level 2 Trigger ☐

Select Front-End Board: ALL FEBs

**Front End Board L2 Trigger is:**

AND ☐ AND with External Trigger Gate = 0 ns

AND ☐ AND ☐ AND ☐ AND ☐ AND ☐

SAMPIC0 ☐ SAMPIC1 ☐ SAMPIC2 ☐ SAMPIC3 ☐

Primitives Gate Length 20 ns Latency Gate Length 20 ns  
 (Ch To Conv)

Panel for L3 TRIGGER  
(Controller board)

MAIN VERTICAL HORIZONTAL EXT & L3 TRIG L2 TRIG L1 TRIG TOT

**External Trigger Options**

Level ☐ Software ☐ Internal Osc ☐ External Sig  
 TTL ☐ NIM ☐ Edge ☐

Select FEB: ALL FEBs

Select SAMPIC: ALL SAMPICs

Use Ext Trig as Enable Trig ☐

Open Gate on Ext Trig ☒

Local Ext Trig Gate 80 ns

**Enable Build L3 Trigger** ☐

(WARNING 1: to Enable Build L3, Enable Build L2 must be selected)  
 (WARNING 2: At least one 'AND' must be selected in the L3 building combinatory!)

**L3 Trigger is:**

AND ☐ AND with External Trigger Gate = 80 ns

AND ☐ AND ☐ AND ☐ AND ☐ AND ☐

FEB0 ☐ FEB1 ☐ FEB2 ☐ FEB3 ☐

AND ☒ OR ☐ Left ☐ Right ☐ Force 0 ☐ Force 1 ☐

6-option menu

# PICOTECH & T2K

512-channel gamma-detector prototype @ PicoTech

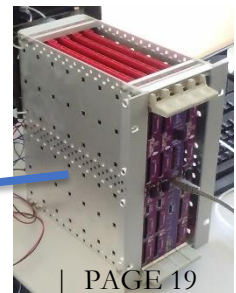
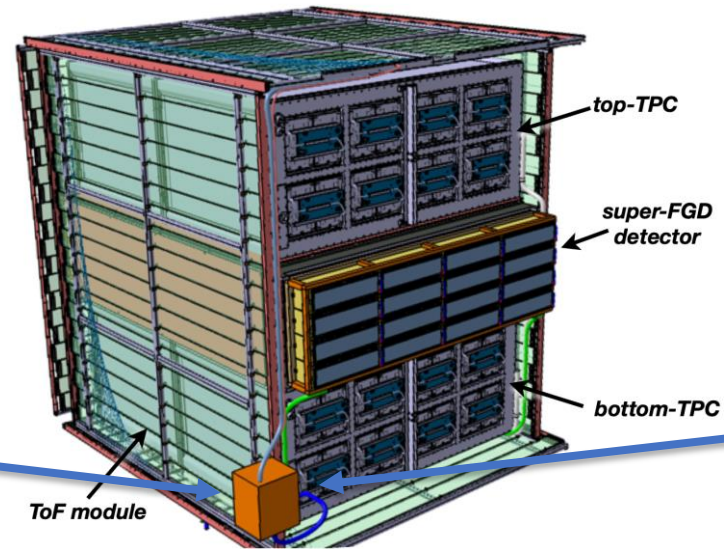


PicoTech prostate scanner

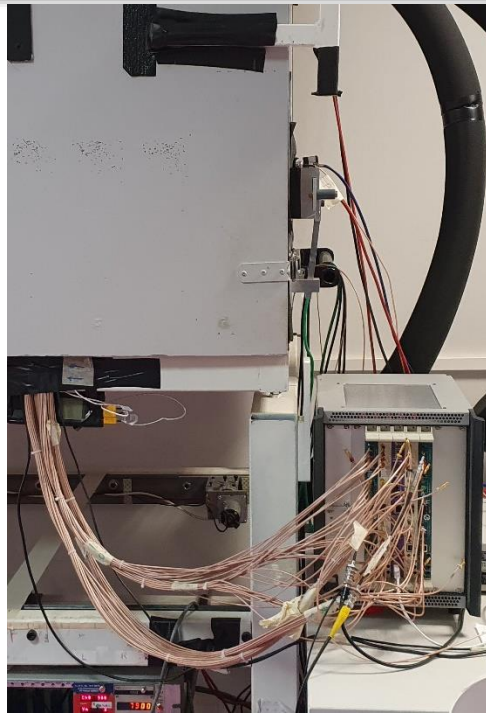


ND280 Timing Detector:

- Tests @ CERN with 64-channel WaveCatcher
- 256-channel customized water-cooled SAMPIC crate

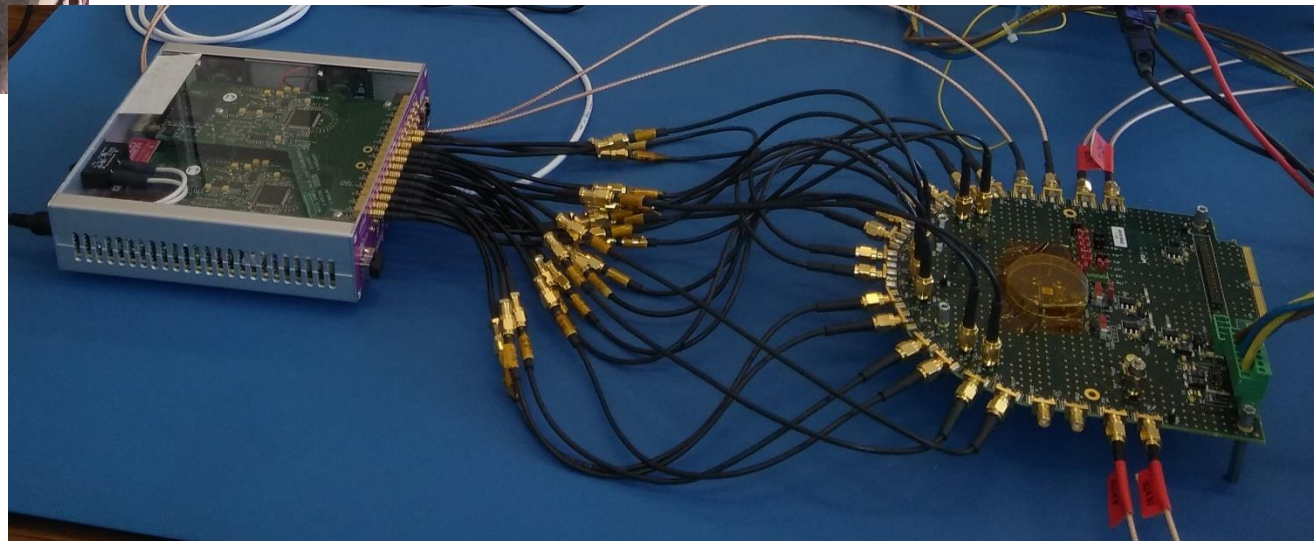


# MINI-LIQUIDO & RAFAEL



- **Mini-LiquidO** prototype at CENBG
- Readout by a 64-channel WaveCatcher crate.
- We take a picture of the full detector for each event and time resolution is a key element for the precision of offline reconstruction.
- Next step for LiquidO electronics is moving to SAMPIC ~ **2000 channels for prototype of L-PET scanner (ANR 2021)**

- Test bench (will be robotized) for the production and characterization of the **100,000 RAFAEL ASICs** (Clock Buffer for CMS) at IRFU
- Readout @ 8,5 GS/s by 32-channel SAMPIC module.
- Channel time resolution measured is **< 3 ps rms !**



# CONCLUSION

## SAMPIC circuit

**SAMPIC** is a full **System On Chip**:

- Analog or digital input, fully digital output, sampling from **1.6 to 10.2 GS/s**
- Works like a TDC: raw counting rate can go **>> 100 kHz/ch.**
- All the DACs and calibration generators are integrated
- It just requires power, clock, and a simple interface with an FPGA
- **Small power consumption ~10 mW/channel**
- Large choice of smart triggers

It can be used for a **highly integrated tiny module** (cm<sup>3</sup> as well as for **large scale detectors** (nuclear or high energy physics, TOF-PETs, ...).

Successful migration to **TSI 0.18μm** (also sourced from IBM 0.18μm)

**A second version has been designed for slower sampling (~350 MS/s to ~2 GS/s)**

## SAMPIC Systems

- **SAMPIC Systems: 16 ch to 256 ch.**
- Timing resolution < **5ps** at the system level.
- Powerful **Software(s)** and C library
- Possibility to **synchronize multiple crates.**
- **Complex Systems:** mechanics, components, test & validation etc... → no more than 256ch Crate.

**Future developments:**

- Design of a **Master Board** for **clock** and **trigger** distribution of **multiple crates.**
- Implement **Individual DAQ links** in the crates
- Implement **10 Gbit-Ethernet** on the Controller Board ?



# ANNEXES

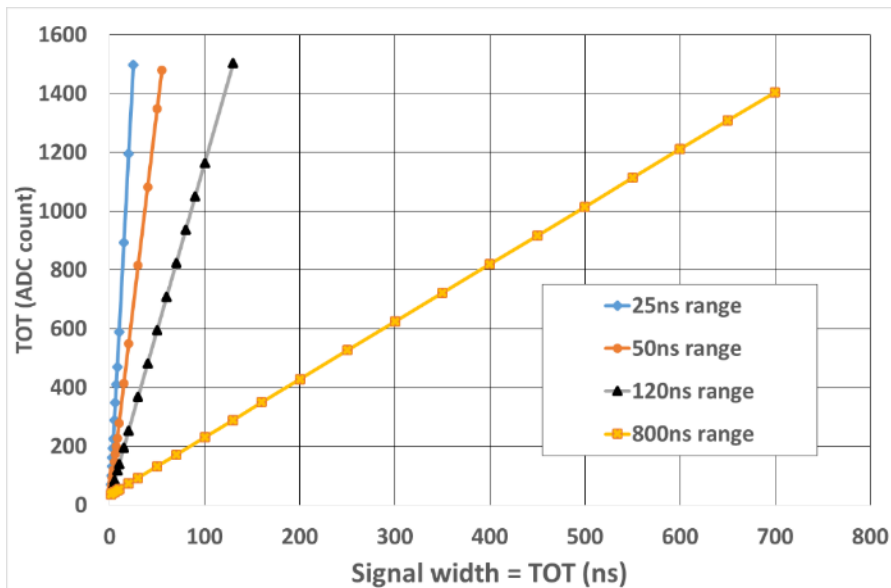
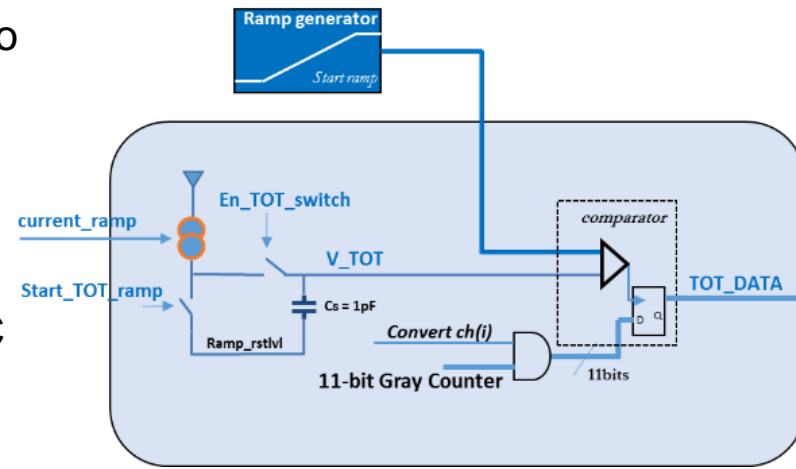
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# TAKING DATA WITH DETECTORS

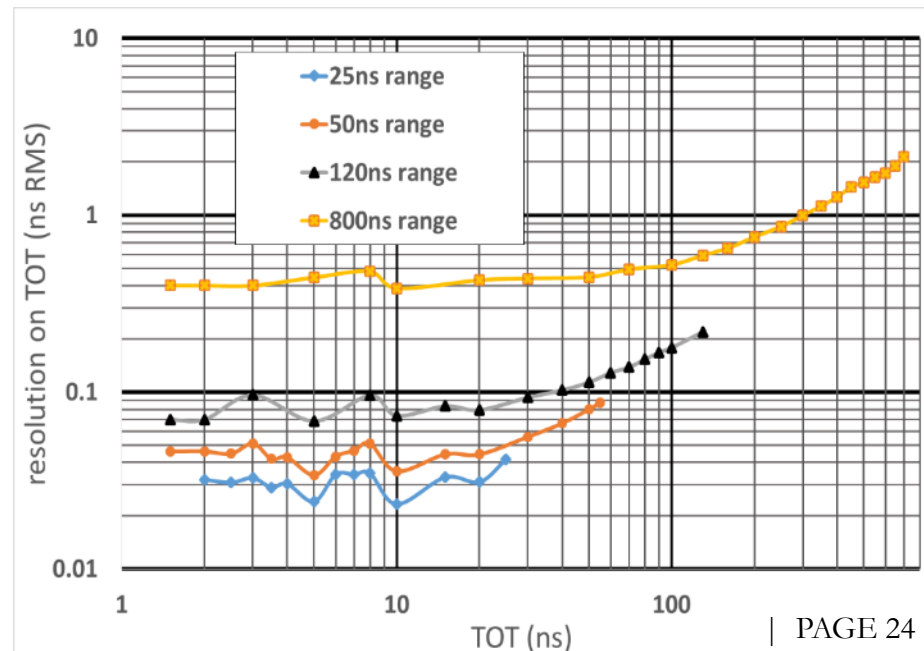
- SAMPIC modules are already used with different detectors on **test benches or test beams**.
- Tested with **PMTs, MCP-PMTs, APDs, SiPMs, fast Silicon Detectors, Diamonds**: performances are equivalent to those with high-end oscilloscopes
- Different R&Ds ongoing with the **TOF-PET** community (CERN, IRFU, IN2P3, PicoTech...)
- SAMPIC is used for many beam tests **at CERN, DESY, FermiLab, ...**
- **TOTEM** developed a CMS-compatible motherboard housing SAMPIC mezzanines. 192 measurement channels have been used on the LHC.
- SAMPIC is the baseline readout option for **many detectors** of the **SHIP and SND@LHC** collaborations.
- Used for **T2K** near detector Upgrade: 256-channel **Timing Detector**.
- Used for characterization of ultra-fast detectors (**Photek** for MCP-PMTs (IEEE paper))
- Used for the **characterization and production test bench of high performance ASICs (IRFU for CMS)**
- Used at IJCLab for the readout of the **new LiquidO detector R&D concept => Neutrino physics, PET scanner**

# TOT MEASUREMENT

- SAMPIC is meant for digitizing a short signal, or only a small part of a longer one (eg rising edge) to extract the timing → then **the other edge** is skipped
- Addition of a **ramp-based Time to Amplitude Converter** in each channel seen as a 65th memory cell during digitization → ~10bit TOT TDC
- A **TOT-based filter** is also integrated in the chip

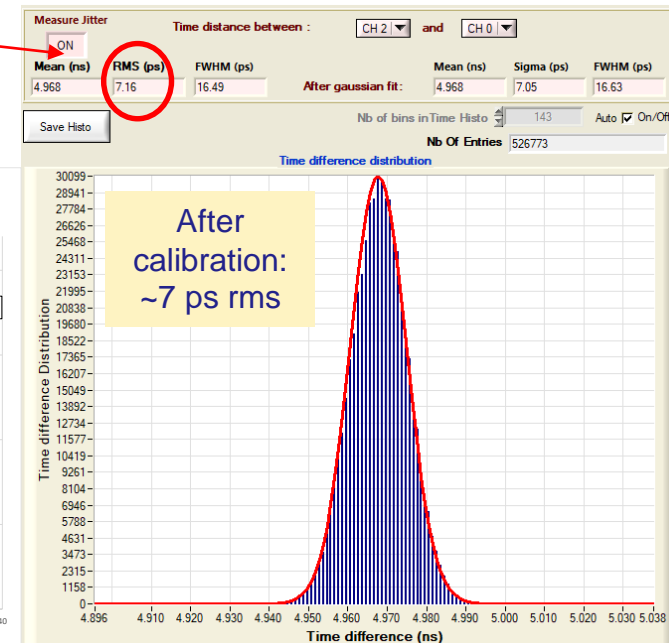
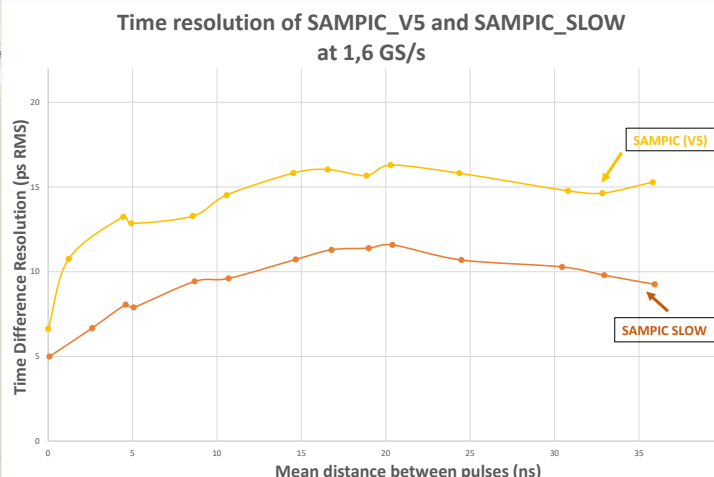
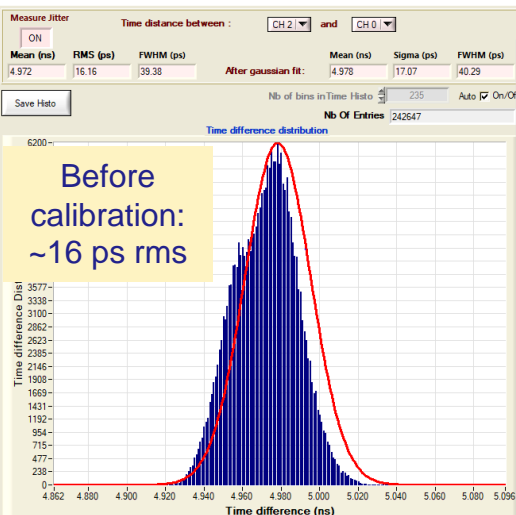


Measurement ranges between 2 and 700 ns.



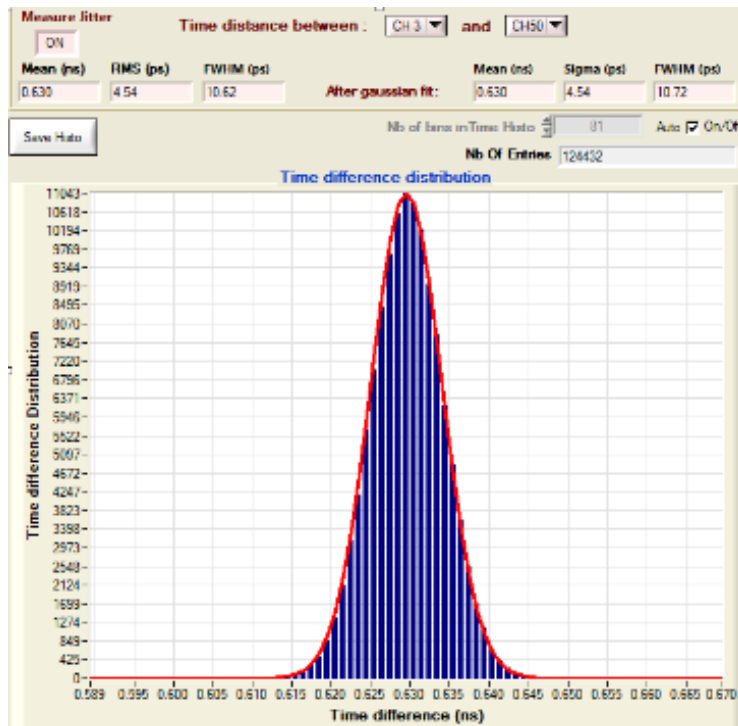
# SAMPIC\_SLOW

- A second version dedicated to slower sampling has been developed.
  - **Wider time window** should permit effective multi-sample offline reconstruction
  - Pin to pin compatible with standard version. Only difference is the main clock frequency.
  - DLL optimized for running between 350MS/s and 2GS/s
  - All delays servo-controlled to main clock have been adapted
  - Analog memory cell has been enlarged (as much as easily possible but not yet optimum)
- First **preliminary tests** are very encouraging.
  - TDR @ 1.6 GS/s < 10ps rms ! (**mainly limited by SNR**, already very good without calibration)
  - Noise @ 1.6 GS/s ~ 1.05 mV rms



# TDR between 2 chips

- Between 2 chips:**  
 @  $F_s = 6.4 \text{ GS/s}$   $\Delta t = 0.63 \text{ ns}$   
 $\Rightarrow$  **TDR = 4.5 ps rms**



- ADC conversion time can be reduced (by decreasing the resolution): factor 2 for 10 bits (800 ns), 4 for 9 bits (400 ns), 8 for 8 bits (200 ns), 16 for 7 bits (100 ns).

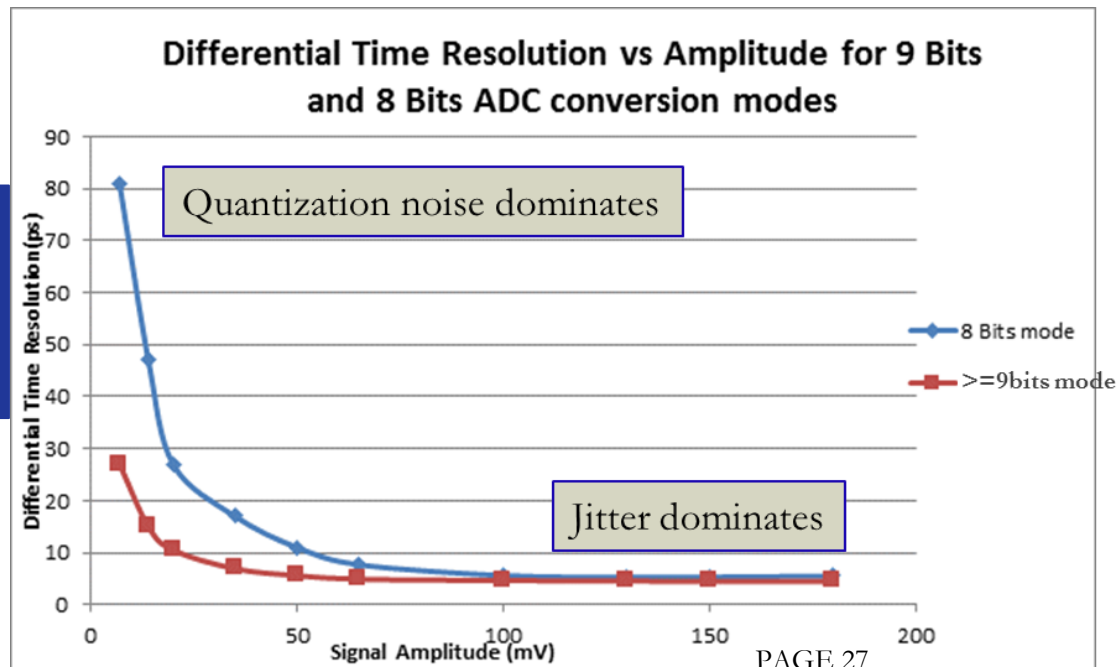
→ **decrease of channel instantaneous dead time**

- The quantization noise affects the timing precision only for very small signals

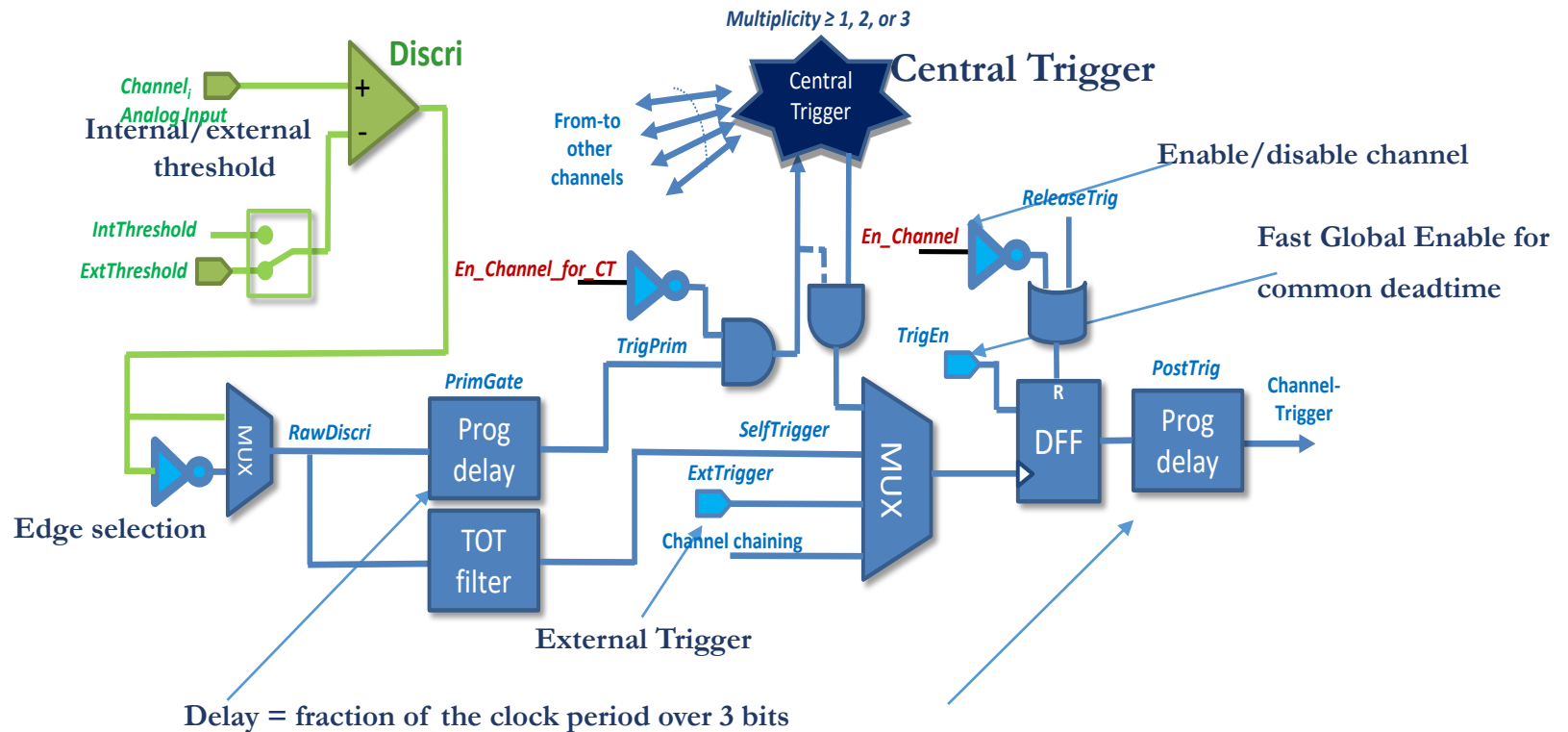
⇒ as expected **no significant change** measured for 11, 10 and 9-bit modes

⇒ **for digital signals, 8 bits or less is adequate => reduced dead time (< 200 ns)**

**No degradation on timing  
for pulses above 100mV for  
8 bits**



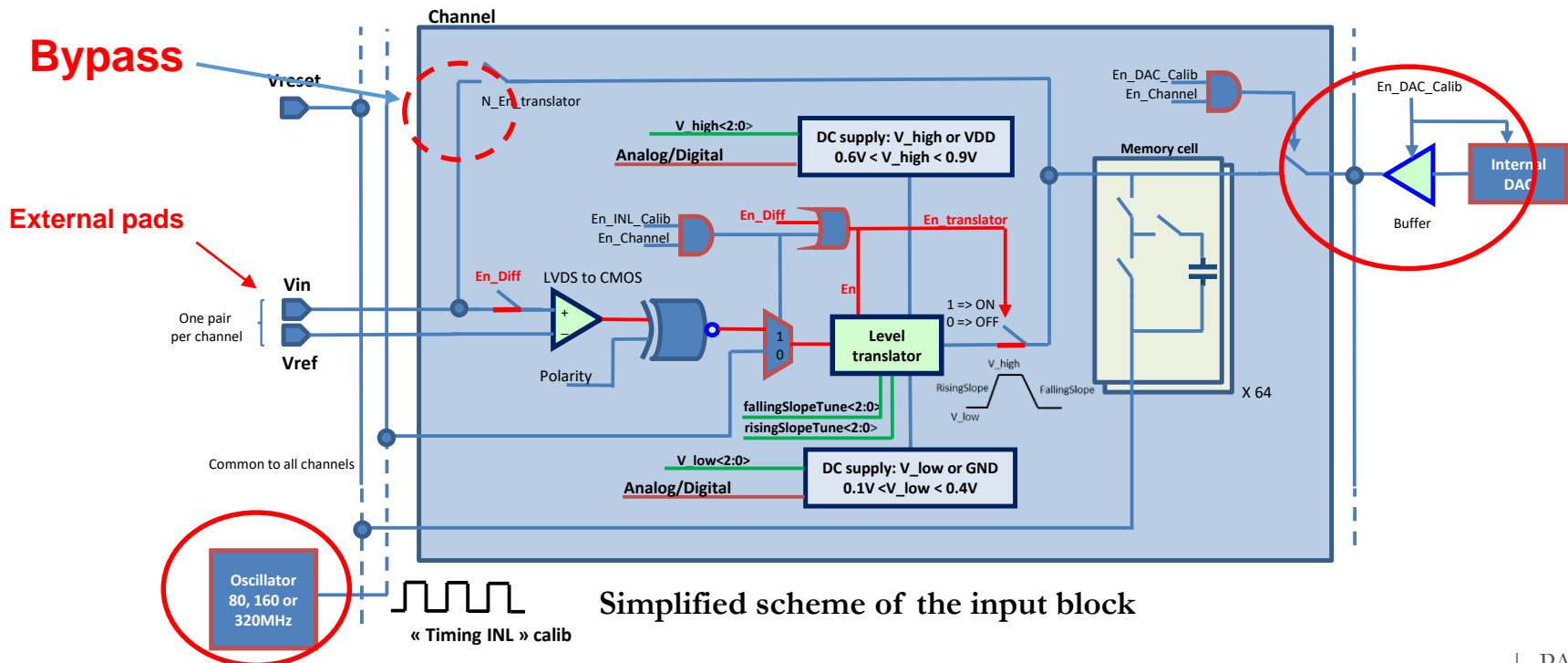
# SAMPIC INTERNAL TRIGGER SCHEME



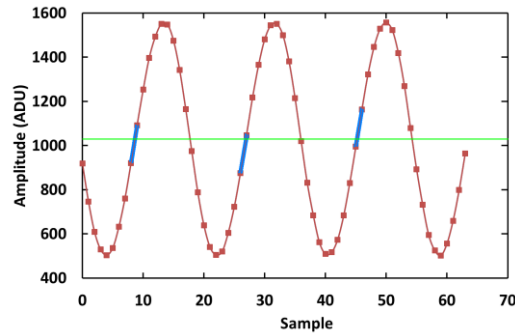
**Only the triggered channels are in dead time**

# SAMPIC INPUT BLOCK (FROM V3)

- **Input block :**
  - Input signal can feed the memory directly (**Bypass Mode**) or pass through a **translator block**
  - It permits among others:
    - **Self calibration of the chip (amplitude & time)**
    - Compatibility with **digital unipolar & differential signaling**
- **When fixed amplitude** at translator output → we only need to read a **few samples** (ROI) and fast conversion can be used ( $\leq 8$  bits) => **behaves like a TDC**



# TIME INL CALIBRATION AND CORRECTION



Method we introduced in 2009 and used since for our analog memories, assuming that a sinewave is nearly linear in its zero crossing region: **much more precise than statistical distribution**

- Search of zero-crossing segments of a free running asynchronous sine wave

**=> length[position]**

- Calculate the average amplitude for zero-crossing segment for each cell.

- Renormalize (divide by average amplitude for all the cells and multiply by the clock period/number of DLL steps)

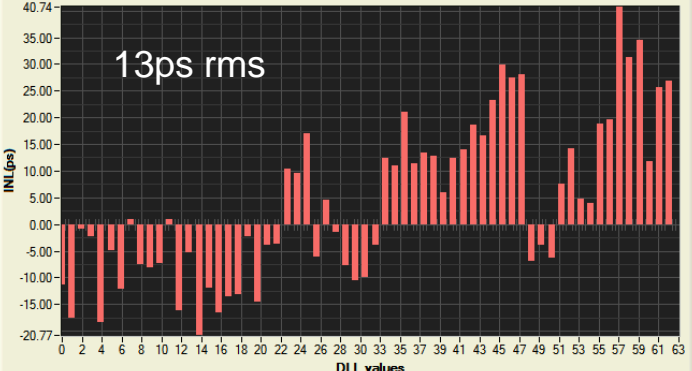
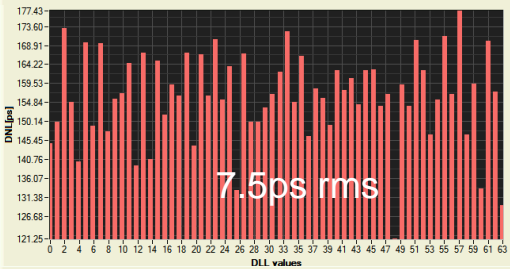
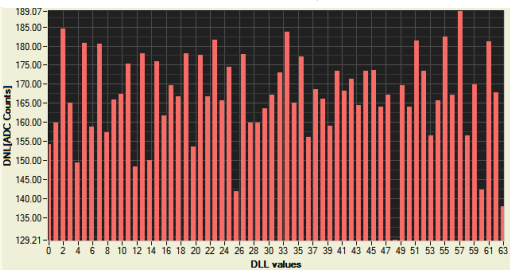
**=> time duration for each step = “time DNL”**

- Integrate this plot:

**=> Fixed Pattern Jitter = correction to apply to the time of each sample = “time INL”**

**Time INL correction:**

- **Simple addition** on  $T_{\text{sample}}$
- Also permits the calculation of real equidistant samples by interpolation or digital filtering.

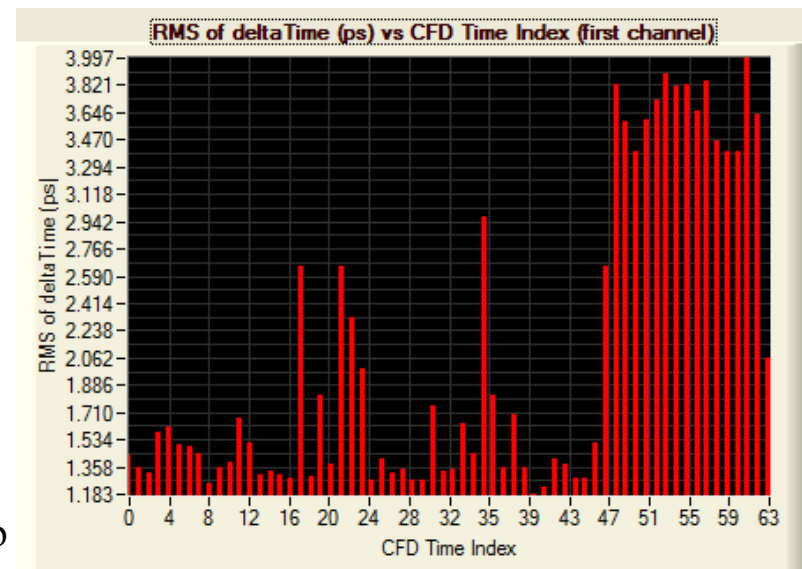


# TRICKS FOR UNDERSTANDING RESOLUTION

- This is how we measure the contributions to the resolution:  
we run at 6.4 GS/s, send two 500 mV pulses separated by 2.5 ns to two channels:

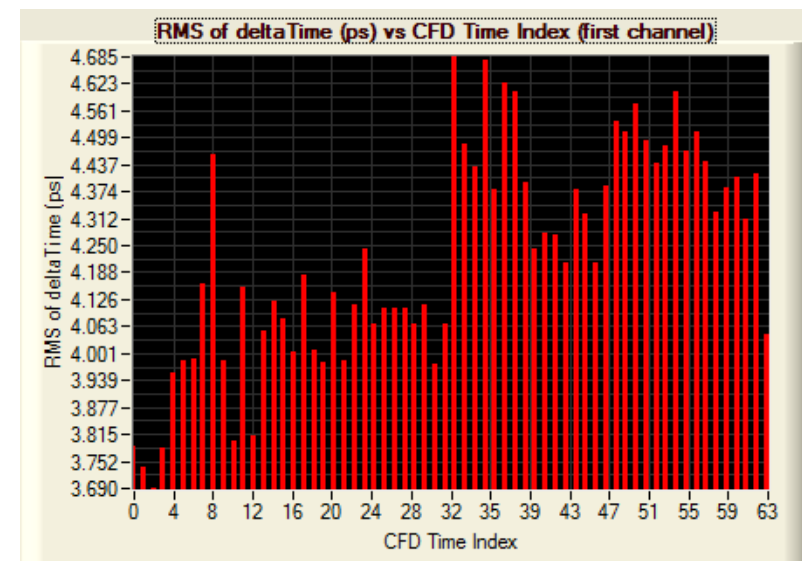
1. of the same mezzanine
2. of two different mezzanines

Same chip



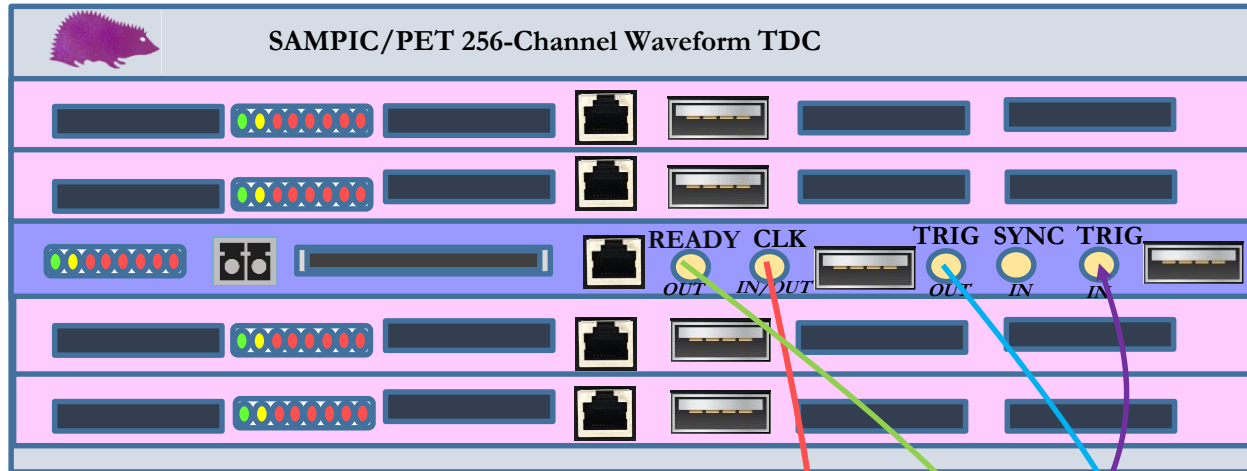
- From this we can extract that **the jitter contribution is:**
- ~ 1.5 ps rms from the DLL
- ~ 1.8 ps rms from the clock distribution on the motherboard
- ~ 2.4 ps rms from the clock distribution on the mezzanine

Different chips



# SYNCHRONISATION DE DEUX CRATES 256-CH

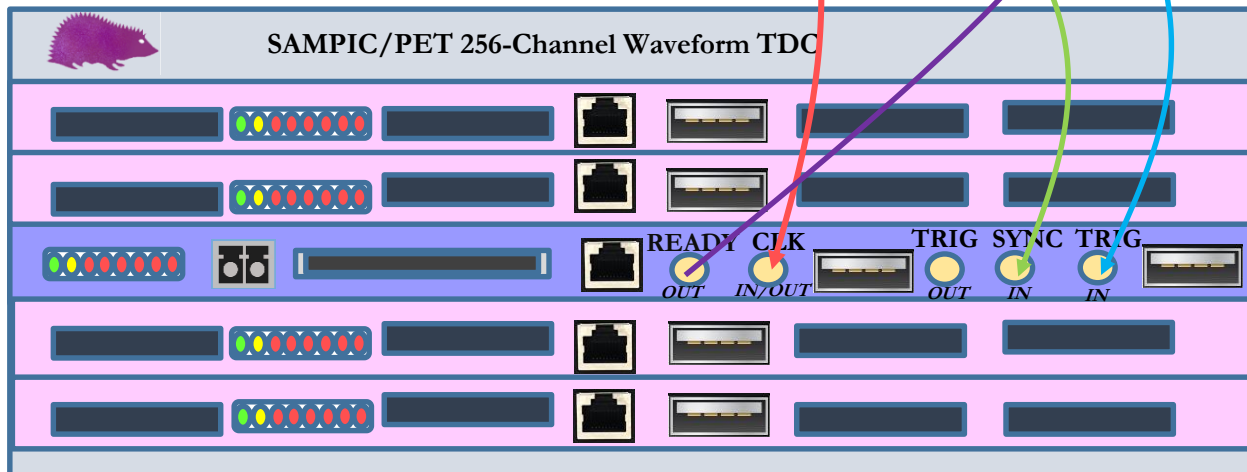
Master Crate



64-ch FE Board

Controller-4FE Board

Slave Crate



Clk

sync

ready

enable\_trig

# SAMPIC: PERFORMANCE SUMMARY

		Unit
Technology	AMS CMOS 0.18 $\mu$ m	
Number of channels	16	
Power consumption (max)	180 (1.8V supply)	mW
Discriminator noise	2	mV rms
SCA depth	64	Cells
Sampling speed	0.8 to 10.2	GSPS
Bandwidth	> 1	GHz
Range (unipolar)	~ 1	V
ADC resolution	7 to 11 (trade-off time/resolution)	bits
SCA noise	~ 1	mV rms
Dynamic range	> 10	bits rms
Conversion time	0.1 (7 bits) to 1.6 (11 bits)	$\mu$ s
Readout time / ch @ 2 Gbit/s (full waveform)	< 450	ns
Single Pulse Time precision before correction (4.2 to 10.2 GS/s)	< 15	ps rms
Single Pulse Time precision after time INL correction (4.2 to 10.2 GS/s)	< 3.5	ps rms