

M. M. Vignetti ^{(a) *}, F. Calmon ^(a), P. Pittet ^(a), G. Pares ^(b), R. Cellier ^(a), L. Quiquerez ^(a), T. Chaves de Albuquerque ^{(a) **}, E. Bechetoille ^(c), E. Testa ^(c), J.-P. Lopez ^(c), D. Dauvergne ^(d), J. Hérault ^(e), A. Savoy-Navarro ^(f)

(a) Institut des Nanotechnologies de Lyon, Villeurbanne (France), (b) CEA-LETI, Grenoble (France), (c) Institut de Physique Nucléaire de Lyon, Villeurbanne (France), (d) Laboratoire de Physique Subatomique & Cosmologie, Grenoble (France), (e) Centre Antoine Lacassagne, Nice (France), (f) Laboratoire d'AstroParticule et Cosmologie, Université Paris-Diderot, Paris (France)

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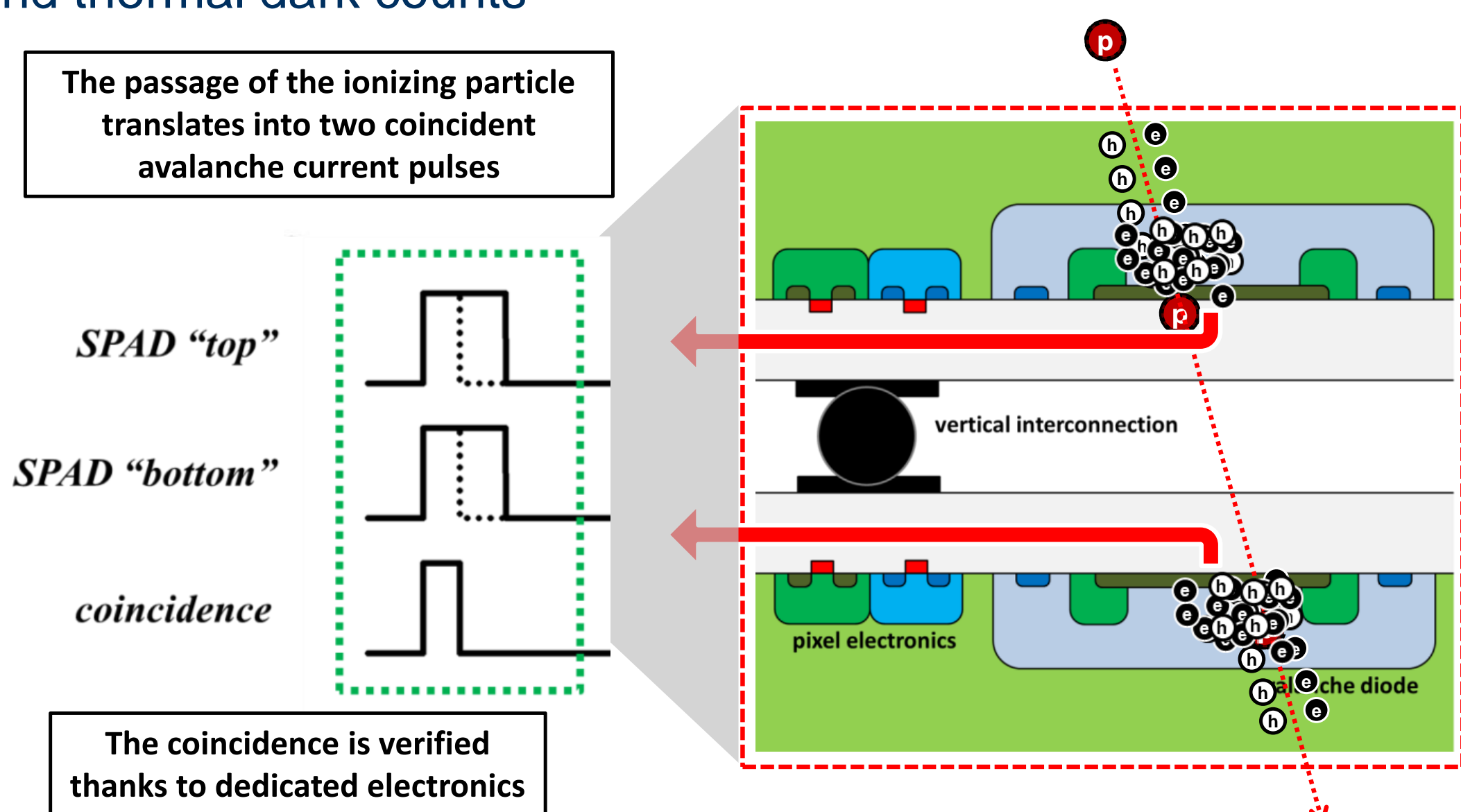
Introduction

This study aims at developing new charged particle detectors based on recent advances in 3D CMOS microelectronics for high energy physics and emerging medical applications such as hadrontherapy and Proton Computed Tomography (pCT). These 3D CMOS integrated detectors are based on two aligned avalanche diodes operated in Geiger mode with on-chip coincidence detection. Such detectors will provide an alternative to existing technologies with expected advantages in terms of limit of detection (very low noise count rate resulting from on chip coincidence detection), spatial (pixel size < 50x50 μm^2) and timing (10-100ps with an hold-off time of 10-100ns) resolutions, high counting rate (>10MHz), scalable solution (with detection areas from tens of μm^2 to hundreds of mm^2), co-integrated low-complexity readout electronics (digital), low material budget, compact and efficient implementation based on standard CMOS technology.

A coincidence-based avalanche detector

3D-SICAD: a novel position sensitive detector for charged particle tracking, exploiting modern 3D-integration techniques

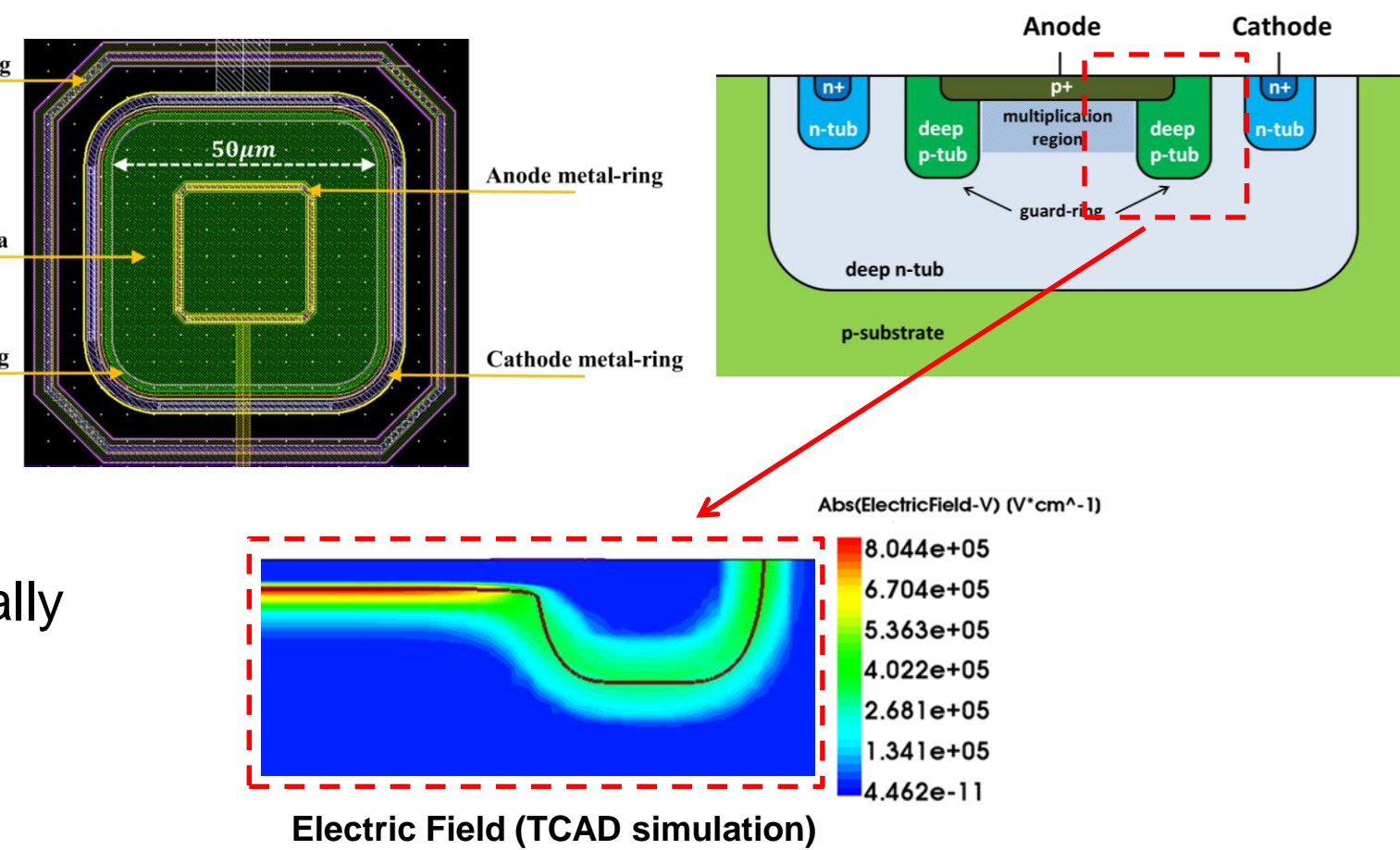
- The passage of an ionizing particle through the pair of vertically aligned avalanche diodes triggers a breakdown process in each cell, producing two substantially coincident electrical signals
- The detection of a coincidence event allows discrimination of the signal produced by an incoming ionizing particle from background ultra-violet, visible and near-infrared photons and thermal dark counts



The avalanche diode working above the breakdown voltage (Geiger mode) is called SPAD (Single Photon Avalanche Diode)

Avalanche diode design in a commercial CMOS technology

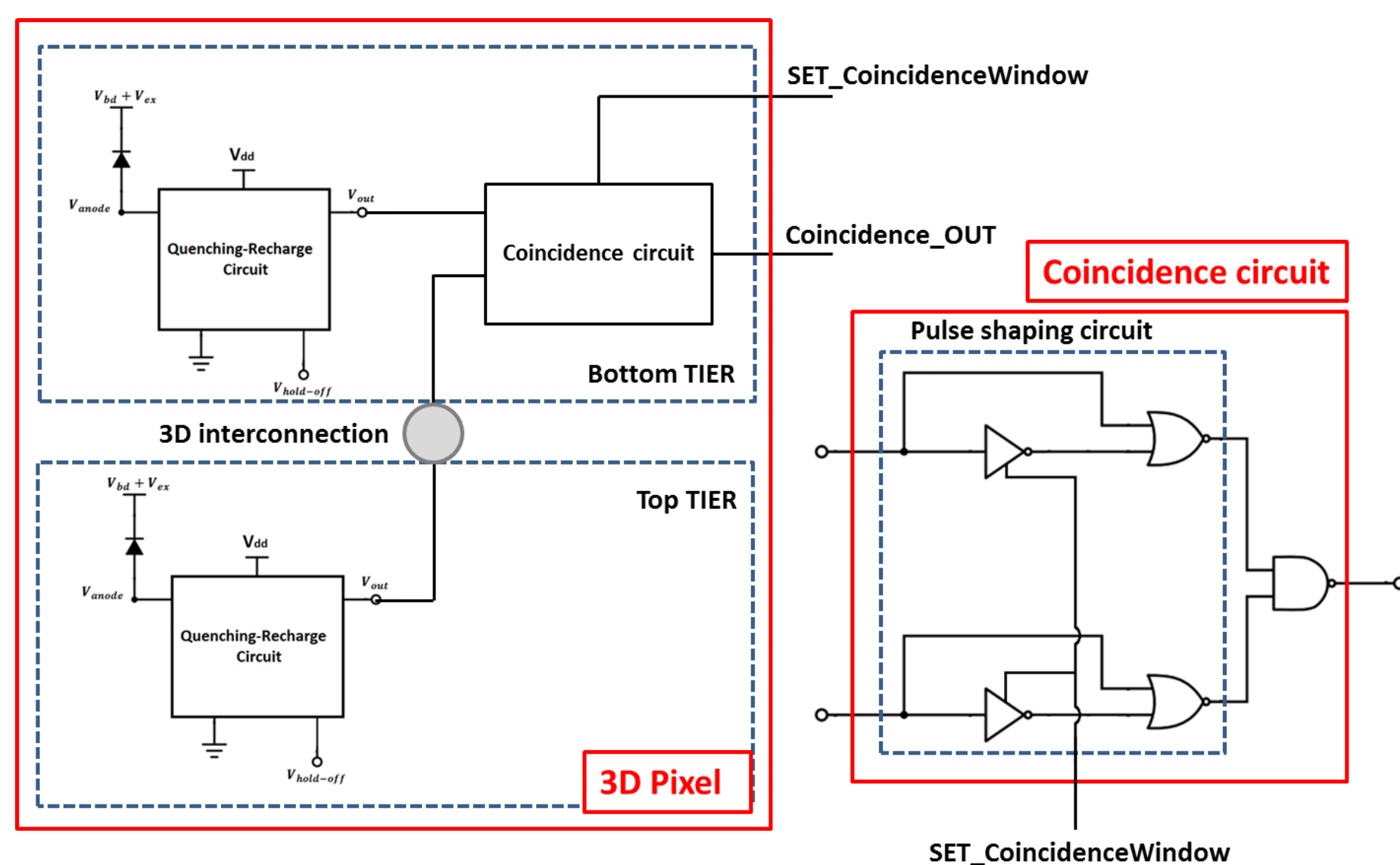
- TCAD study to choose the correct architecture (AMS HV-CMOS 0.35 μm technology implementation)
 - Premature Edge Breakdown prevented
 - Expected low band-to-band tunneling generation thanks to a low n-type doping in the multiplication region
 - Already used for design of CMOS avalanche diodes showing good Dark Count Rate (DCR) levels
 - Diode architecture and CMOS technology eventually chosen according to a trade-off between performance (based on simulation and literature results) and affordable tape-out costs



Pixel electronics

3D-level pixel electronics:

- Check in a tunable time-window, a coincidence between a pair of vertically aligned avalanche diodes.
- 3D-electronics minimizing the impact of possible parasitics introduced by the vertical interconnections.



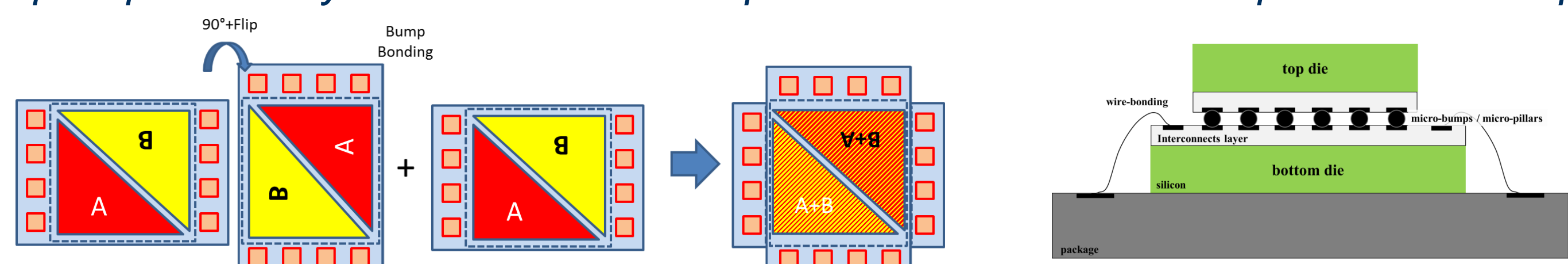
Tape-out and 3D integration

A test-chip has been submitted for tape-out on April 2015 in a MPW run.

- Avalanche diode test structures
- Several 3D pixels cells for coincidence-based detection
- Small 2x2 matrix cells exploiting a hybrid coincidence-based detection:

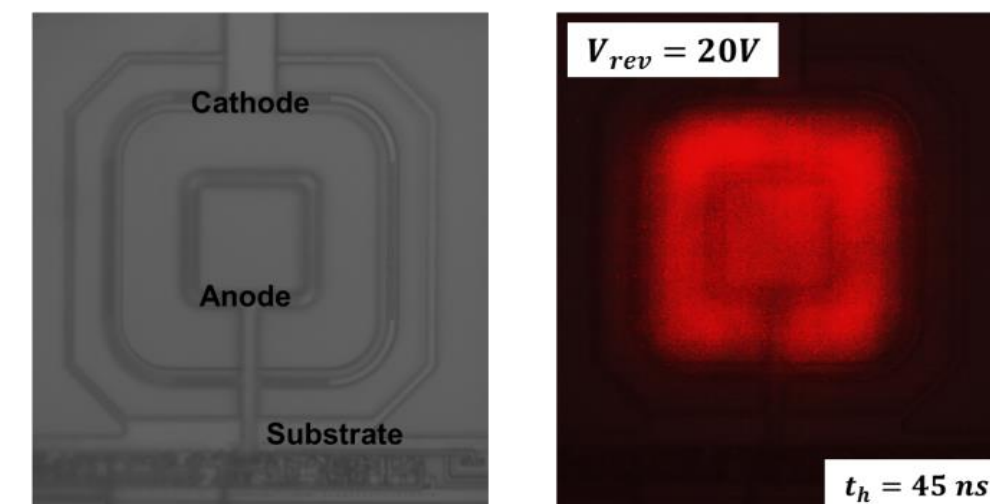
3D integration: flip-chip assembly

Flip-chip assembly of 2 identical test-chips after 90° rotation and flip of one test chip

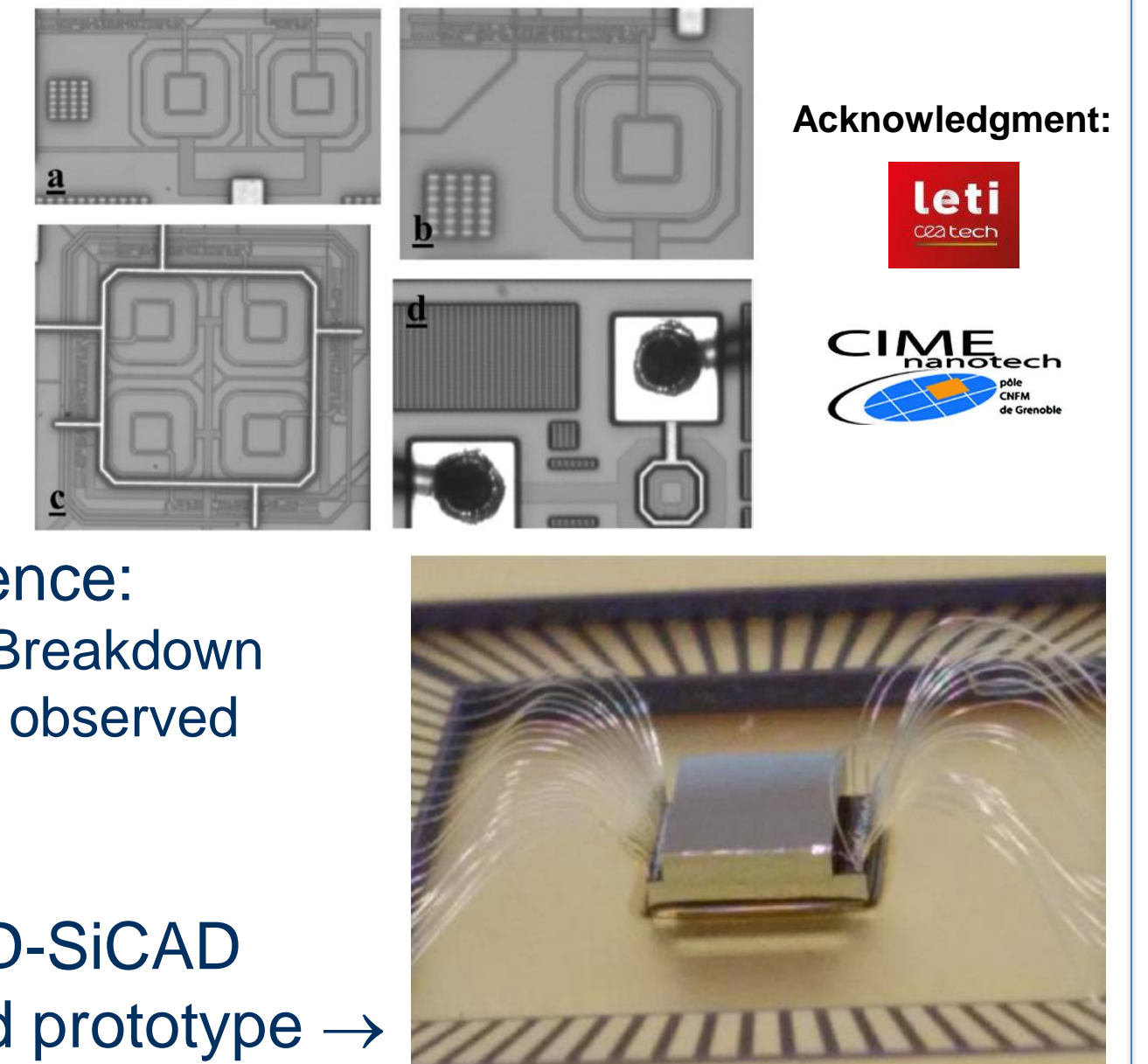


Prototype realization

- a single pixel 3D-SiCAD cell
- a 2 x 2 matrix 3D-SiCAD cell
- test-structures for characterization purposes



← pixel luminescence: no Premature Edge Breakdown and no hot spots are observed



- Measured Dark Count Noise (DCR) median value of around 70 Hz/ μm^2

3D-SiCAD stacked prototype →

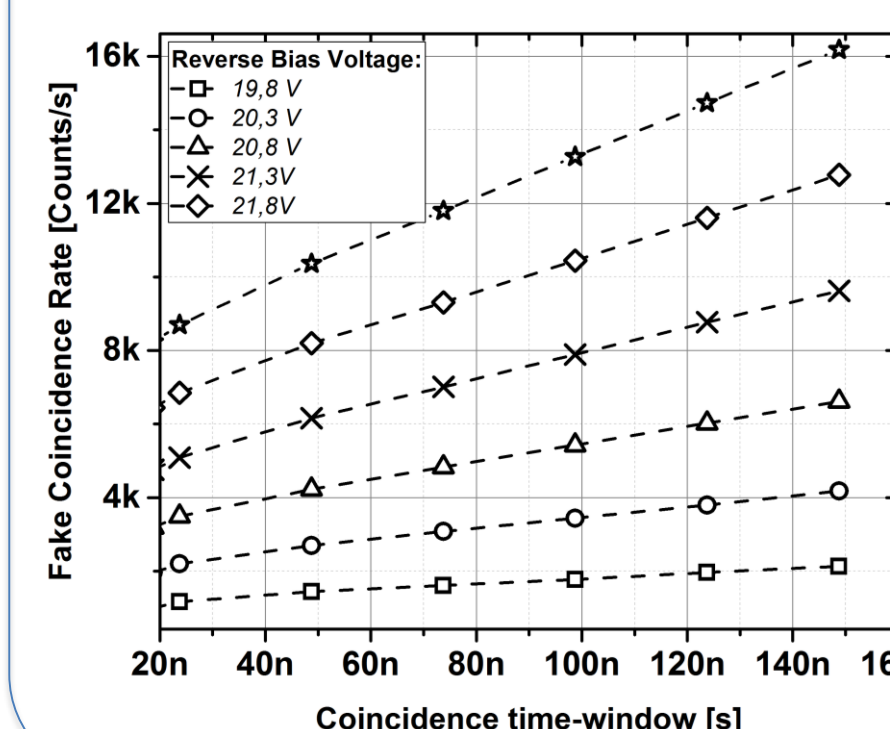
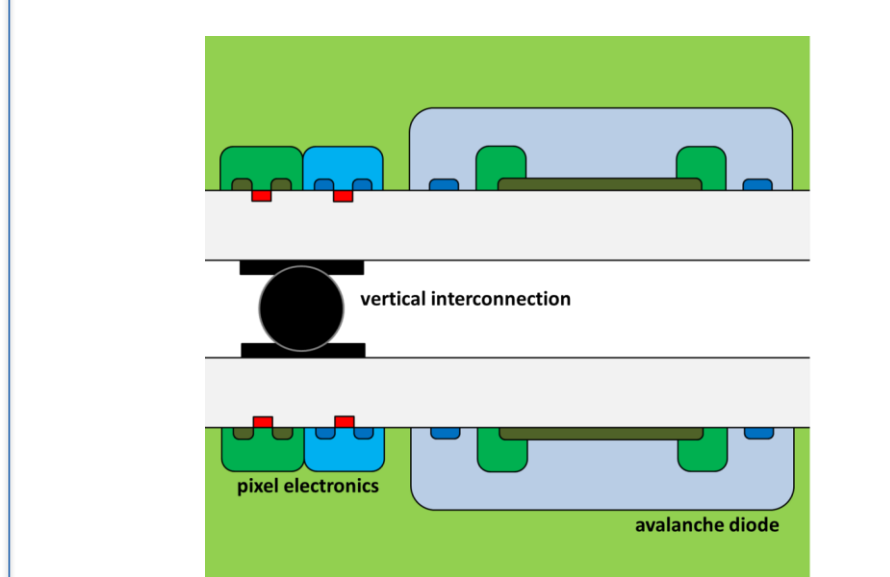
Benefit of the “coincidence-mode” operation

Validation of the “coincidence-mode” operation →

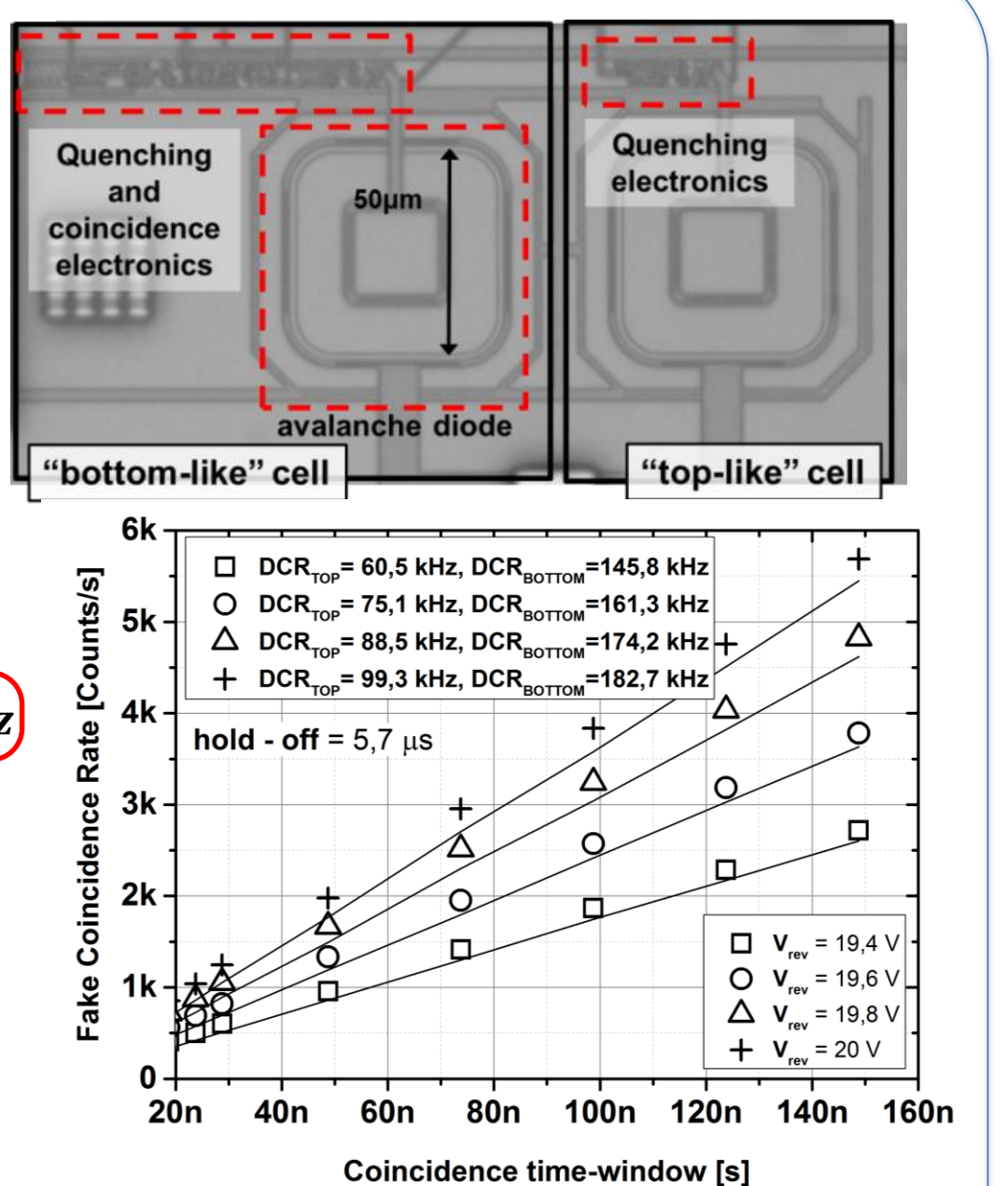
(coincidence counts between two adjacent SPAD pixels)

- Measured data match very well with the predicted fake coincidence rate
- Excellent noise rejection can be achieved if a sufficiently small time-window is adopted

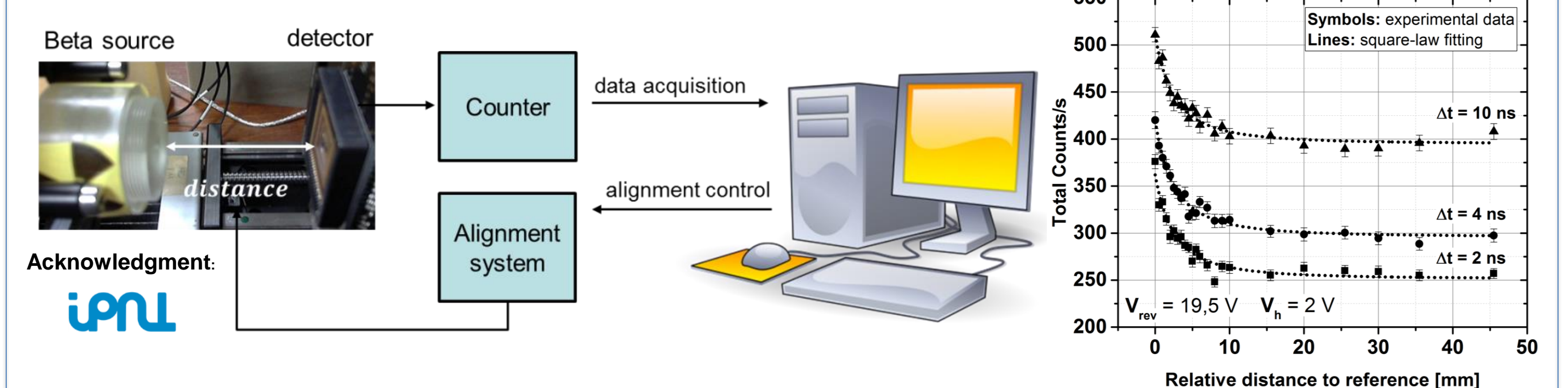
$$@V_{ex} = 1V, \Delta t = 20 \text{ ns} \rightarrow FCR \approx 600 \text{ Hz} \text{ versus } DCR_{top} = 86 \text{ kHz}, DCR_{bot} = 174 \text{ kHz}$$



- Noise Characterization : Fake Coincidence Rate (accidental counts between two vertically aligned SPAD cells in a 3D-SiCAD pixel)
- Measured data do not match with the predicted fake coincidence rate
- The recorded FCR is larger than expected
- FCR curves are shifted by a certain off-set related to the adopted reverse bias voltage
- The observed off-set can be explained by real coincidence counts due to optical cross-talk occurring between the two SPADs (can be avoided with metal layers between SPAD)



Charged particle Detection Capability Characterization

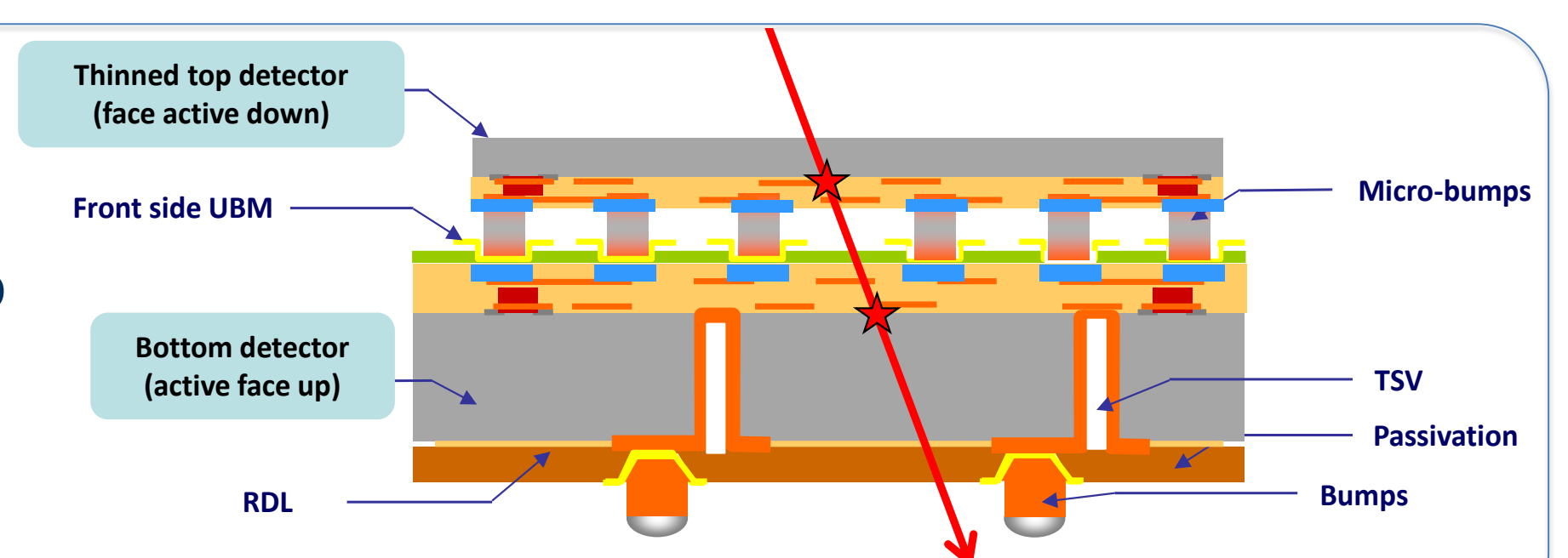


- Results demonstrated particle detection capability for the realized 3D-SiCAD prototype (^{90}Sr source)
- Fitting study of inverse square law data provided an estimation of the activity of the adopted ^{90}Sr source which is in excellent agreement with the nominal value
- The use of single SPAD devices would not allow distinguishing the signal of beta particle from the background counts in a acquisition time of “only” 10 seconds

Perspectives

New prototype with state of the art 3D integration technology:

- Micro-bumps between the two stacked dies
- Through Silicon Vias (TSV) to avoid wire-bondings
- Allow abutted 3D chips onto printed circuit board for large detector area



References

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