Simulation and design of a novel 3D SPAD pixel in CMOS FDSOI technology

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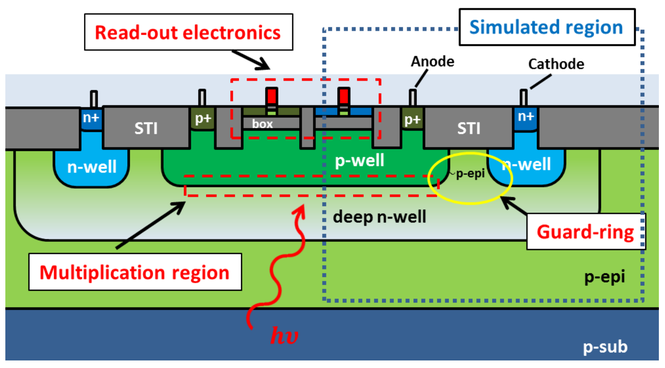
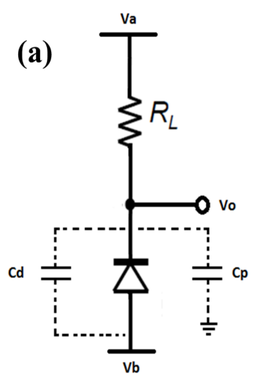
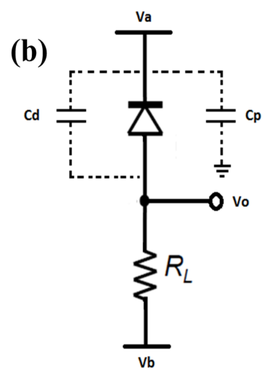
Introduction

A novel SPAD architecture implemented in Silicon-On-Insulator (SOI) CMOS technology is proposed [1]. Thanks to its intrinsic 3D structure, the proposed solution is expected to allow very small pixels while enabling a very high fill factor. Furthermore, the pixel read-out electronics as well as the whole detector electronics can benefit of the well-known advantages brought by SOI technology with respect to bulk CMOS, such as higher speed and lower power consumption. TCAD simulations based on realistic process parameters provided by the foundry are carried out in order to optimize and validate the avalanche diode architecture for an optimal electric field distribution in the device and to obtain a first order estimation of the main parameters of the SPAD, such as the breakdown voltage, the avalanche triggering probability and the dark count rate.

3D Pixel Concept for SPAD in FDSOI technology







The pixel is defined as a monolithic 3D structure consisting of:

- an avalanche diode beneath the Buried Oxide (BOX)
- dedicated electronics in the SOI layer

The design is performed according to the features of an advanced Fully-Depleted SOI technology:

- Several diffusions are available in the substrate below the BOX for the design of the avalanche diode.
- Back-gate contacts (meant for transistor threshold tuning) can be used to connect the diode with the pixel electronics.

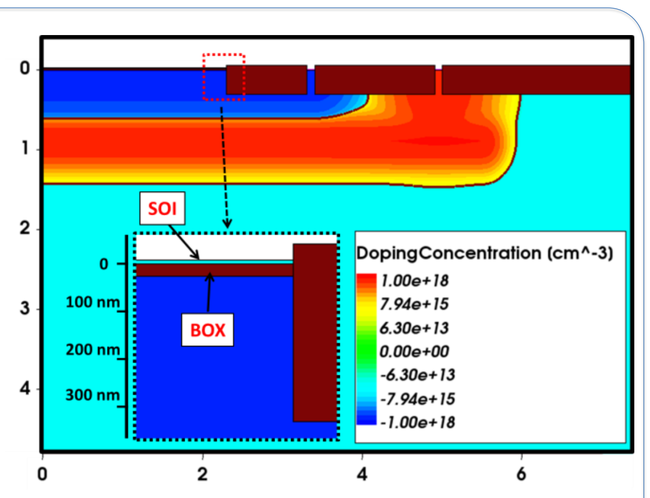
Diode biasing options:

a) Diode BOTTOM (output node is the cathode): back-gate insensitive solution.
b) Diode TOP (output node is the anode): electronics is back-gated at every avalanche cycle.

TCAD model

Geometry:

- 2D geometry representing the radial cut of an avalanche diode with cylindrical symmetry: emulation of a 3D geometry while dramatically reducing the overall comp-tational time.
- realistic doping parameters provided by the foundry.



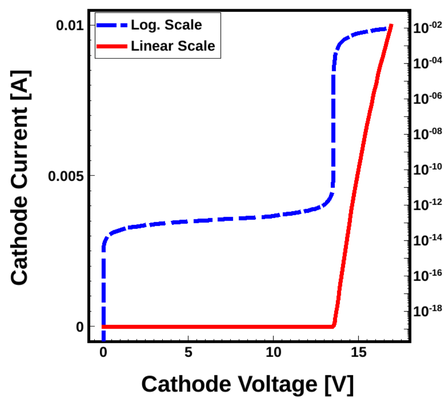
Physical models:

- drift-diffusion model for carrier transport, Fermi-Dirac statistics
- doping dependence of the carriers' mobility [2].
- "van Overstraeten – De Man" model for the ionization coefficients [3].
- Shockley-Read-Hall (SRH) [4] and band-to-band (B2B) tunneling [5] processes as the main contributors for the evaluation of the electron – hole pair (EHP) generation-recombination within the avalanche diode [6].

Results and Discussion

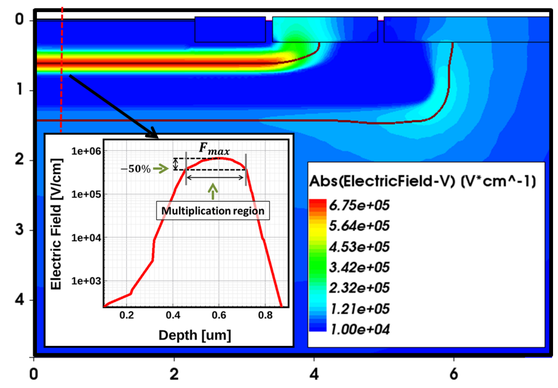
Breakdown voltage extraction:

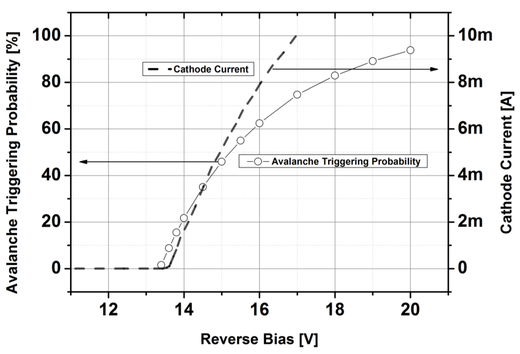
- The simulated reverse bias I-V curve of avalanche diode shows a breakdown voltage $V_{bd} = 13.5V$.
- No experimental data is available for the adopted technology that would allow validating this result.



Premature Edge Breakdown (PEB) prevention:

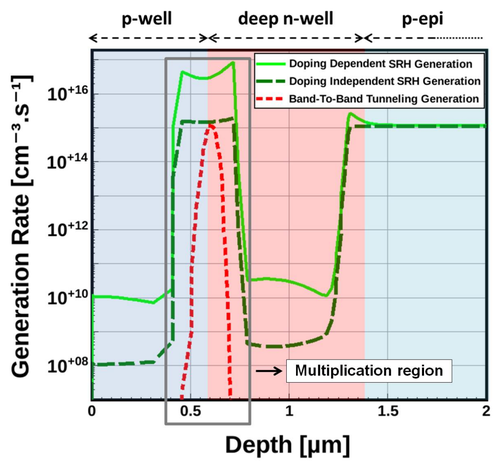
- The electric field color map of the pixel, grounded anode, $V_{rev} = 16.5\,V$, i.e. excess bias voltage $V_{ex} = 3\,V$) shows an uniformly distributed electric field all over the device active region.
- The retrograde n-type doping in the deep n-well effectively acts as guard-ring preventing any peripheral breakdown at the p-well edges.





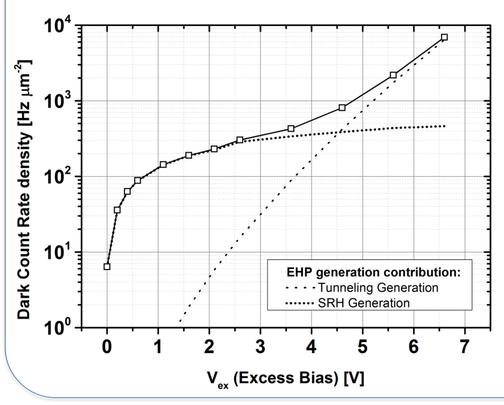
Avalanche triggering probability P_{tr}

- "avalanche triggering probability": the probability that an EHP generated in the multiplication region can successfully trigger an avalanche.
- Calculated as a function of the reverse bias voltage, by implementing a numerical method based on [7].



EHP generation within the avalanche diode sensitive region:

- SRH generation seems to be the dominant generation mechanisms in the avalanche diode sensitive region (at least up to $V_{ex} = 3\,V$).
- tunneling generation is very narrowly distributed along the junction, leading to a minor contribution to the overall EHP generation.
- The physical source of the device DCR seems to be only temperature dependent.



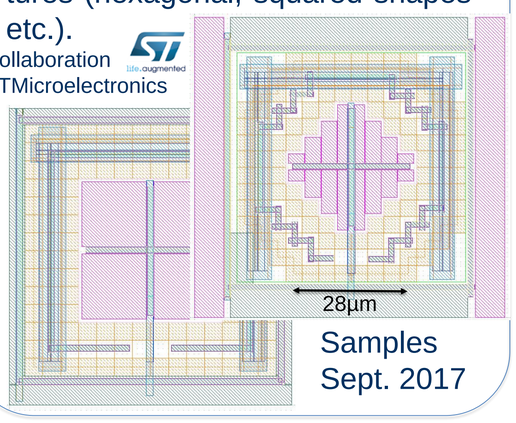
Dark Count Rate

- DCR as a function of the excess bias is obtained by combining EHP generation terms (tunneling generation and SRH generation) with the calculated avalanche triggering probability P_{tr} .
- The tunneling generation is to be considered at high excess bias ($> 3V$).
- The curve is close to what can be found in literature for devices having similar breakdown voltages, i.e. DCR~ $150\ Hz/\mu m^2$ for $V_{ex} = 1V$ see ref [8].
- It is really hard to make any conclusion without any support coming from experimental data, which is not available at the moment.
- A deeper study on the adopted models and their parameters would be really of crucial importance to better calibrate the adopted models and get any better clue about the device DCR.

Test-chip in fabrication

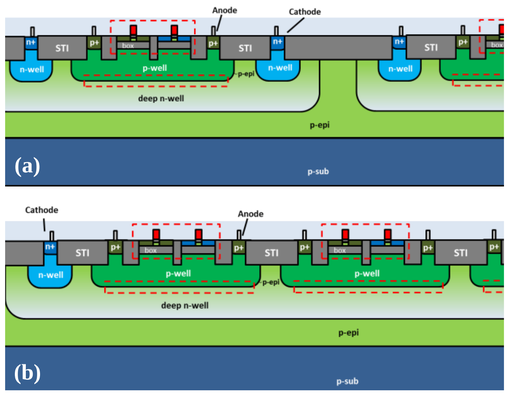
- Test-chip tape out (1mm²) : April 2017, technology CMOS28FDSOI, including different SPAD architectures (hexagonal, squared shapes etc.).

Collaboration STMicroelectronics



Samples Sept. 2017

Perspectives



Matrix arrangements for the proposed pixel

a) provides shielding of the pixel electronics by grounding the p-well. The output is thus sensed at the cathode which penalizes the fill-factor as every pixel needs an independent deep n-well.
b) enables higher fill factor (common deep n-well) but the electronics need to be insensitive to back-gating effects.

References

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