

Discussion on the integrator specifications with comparison of the 3 options

Debriefing meeting at LPC , 28 April 2016
François Vazeille

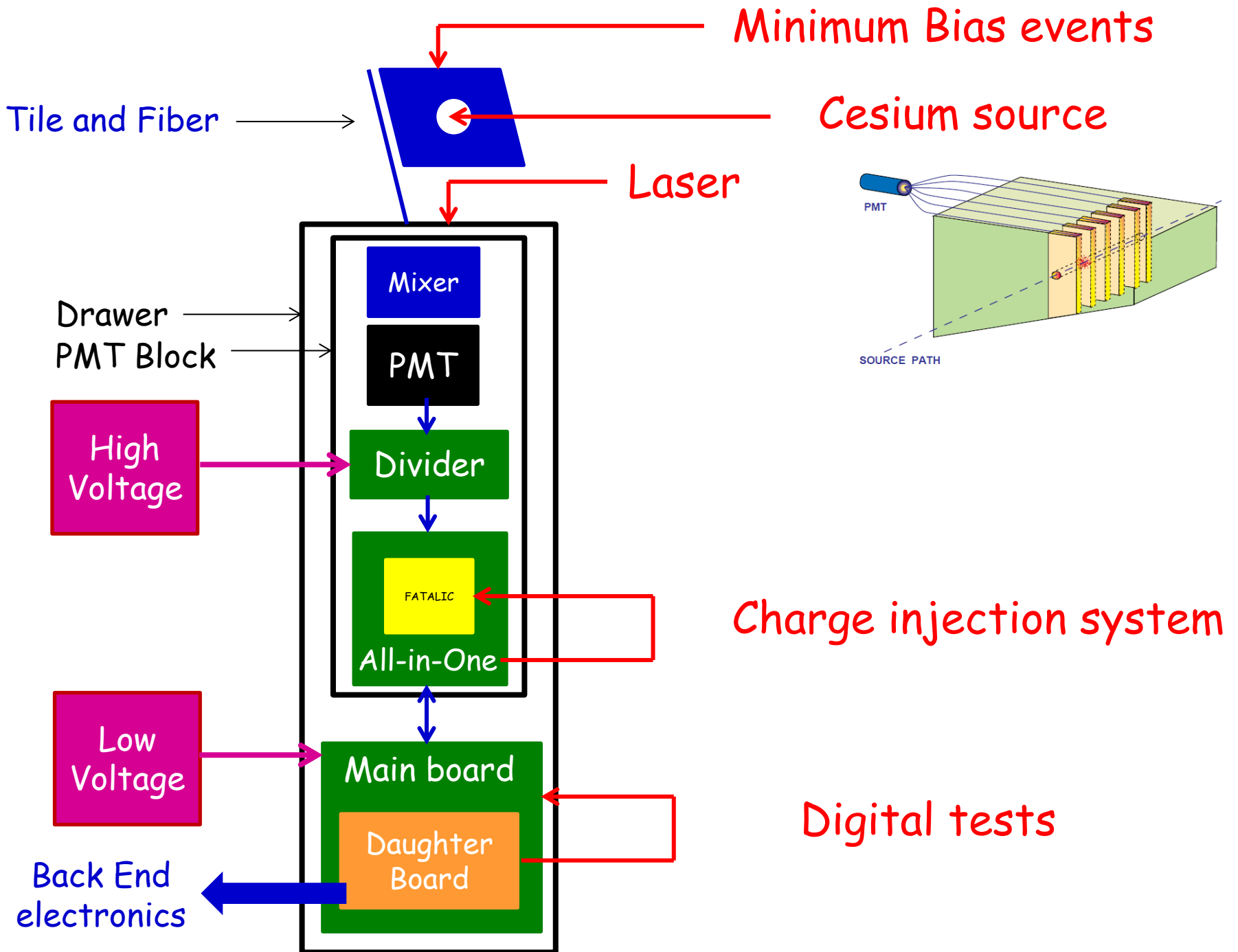
- Summary of the TileCal Calibration systems in the upgrade scheme.
- TileCal data for the Cesium source moving.
- TileCal data for the Luminosity measurements.
- Chicago integrator.
- Argonne integrator.
- Clermont-Ferrand integrator.
- Summary of specifications.

- Summary of the TileCal Calibration systems in the upgrade scheme

4 complementary systems acting at various levels of the whole electronic chain + likely a 5th system for the Back end electronics not shown here.

1. At the Tile/Fiber level: **Cesium** radioactive source and p-p **Minimum Bias** events.
2. At the Light Mixer/PMT level: **Laser**.
3. At the Very Front End electronics level: **Charge Injection System**.
4. At the Front End Board digital level: **Digital tests**.

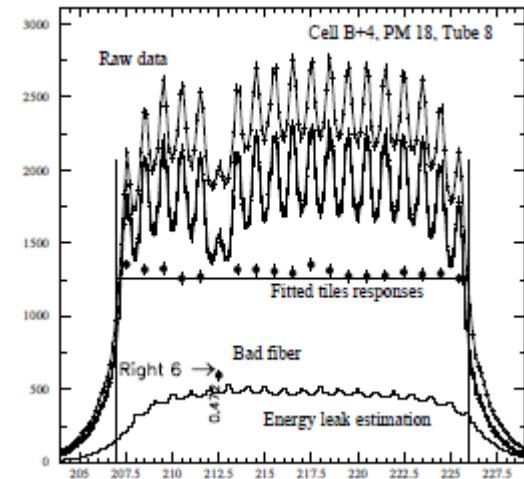
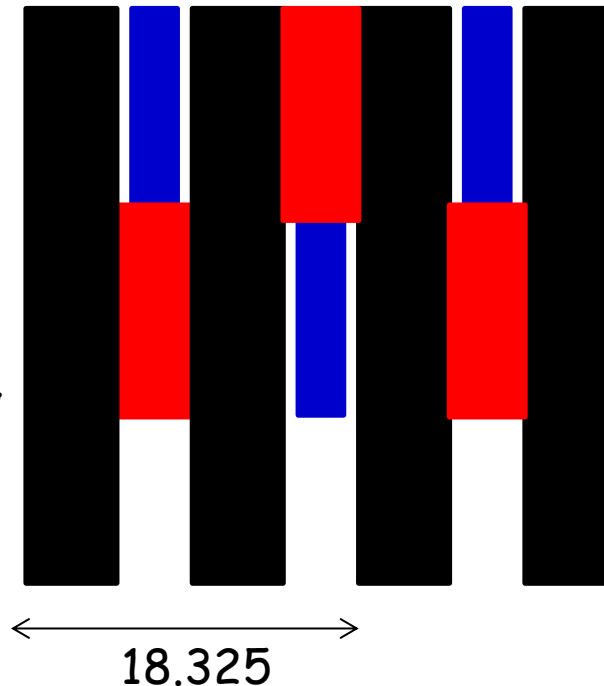
1. PMT gain adjustment/calibration and long term monitoring, plus calibration transport from the ATLAS Test Beam.
2. Short term monitoring and calibration.
3. Electronics calibration in pC.
4. Working tests of the Main Board/Daughter board communication.



• TileCal data for the Cesium source moving

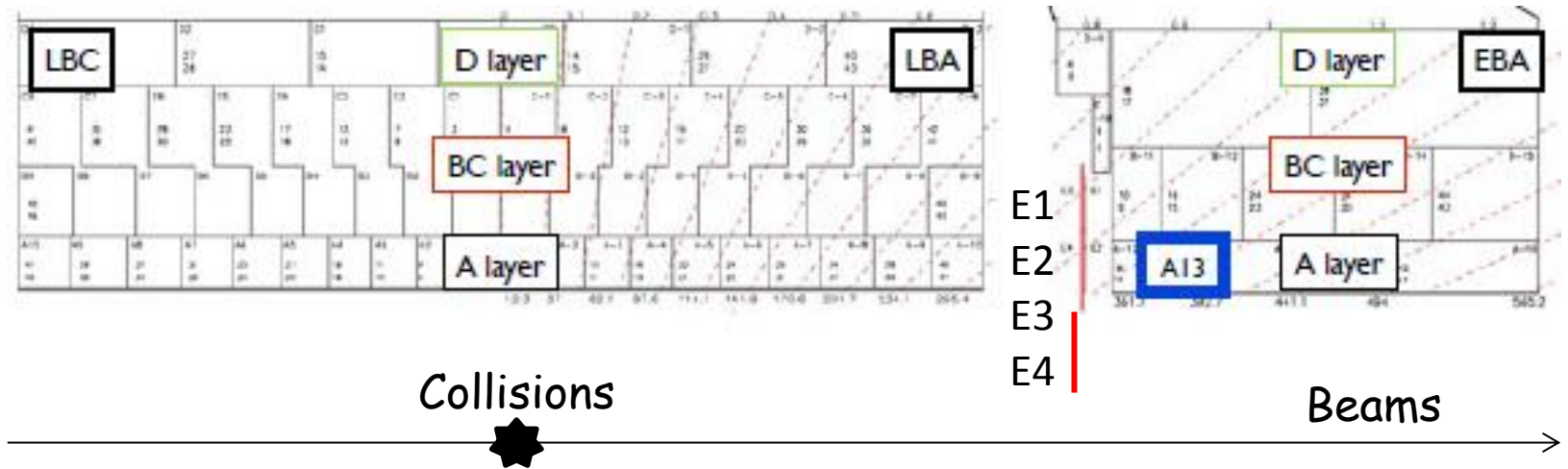
- Source speed: 30 cm/s.
- TileCal scheme

Steel Master = 5.0 mm
Steel Spacer = 4.05 mm
Plastic Tile = 3 mm
Period = 18.325 mm
= 5 + 4.05 + 5 + 4.05 + G
= 18.10 + G G = Glue



- **Transit time:**
 - In a Tile: $0.3/30 = 0.01$ s = 10 ms.
 - From a Tile to the following one: $1.8325/30 = 61.08$ ms.
- **The optimum integration time is 10 ms,** that can be increased by two means:
 - Digital sum without any problem.
 - Analog integration using different time constants.

Orders of magnitude from Ilya's talk



- By taking into account the non-replacement of the sources (Decreased activity)
- Cells A to D: 60 to 90 nA.
 - Cells E1&E2: ≤ 4 nA.
 - Cells E3&E4: ~ 0.06 nA. } Improvements of scintillators/Dividers are possible.
but no Cs in them

Comment: for the E cells, the constraint of 10 ms with respect to adjacent Tiles is no longer relevant \Rightarrow digital sums are possible, and/or use of a 20 ms time in the analog mode in order to reach these low values.

• TileCal data for the Luminosity measurements

▪ Orders of magnitude from Ilya's talk

♦ Maximum value at the highest Luminosity:

- A13 cell: $8 \mu\text{A}$.

- E cells: $100 \mu\text{A}$ \Rightarrow no saturation for Argonne and Clermont-Ferrand.

♦ Minimum value for the vdM scan at very low Luminosity:

up to 0.02 nA to cover almost all the A and E cells and part of B cells,
if not 0.05 nA .

with which accuracy?

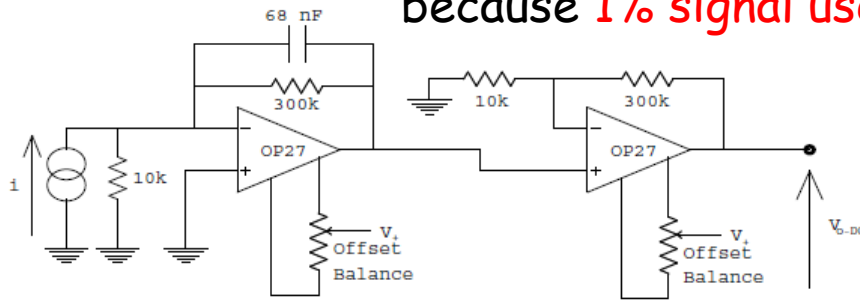
1% is impossible,

5% ? 3% ?

Chicago integrator

- Principle (Present ATLAS scheme):
in 2 steps

Amplification
because 1% signal used



Integration time

from feedback capacitance/resistor

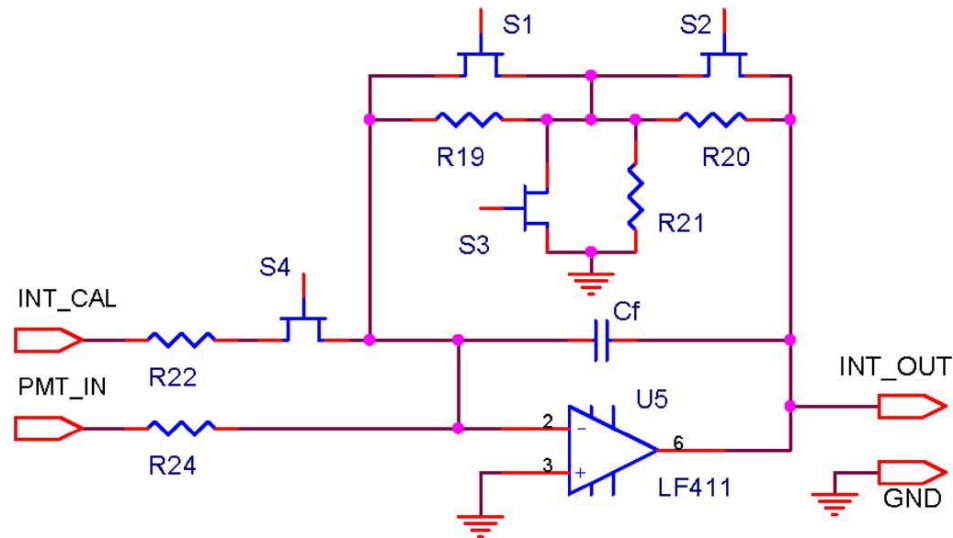
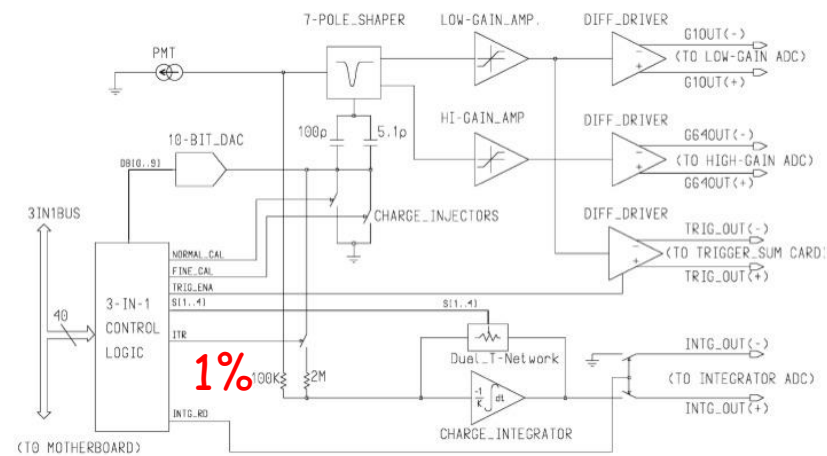
Combination of switches to control

- Timing and Gain.
- DC injection for calibration.

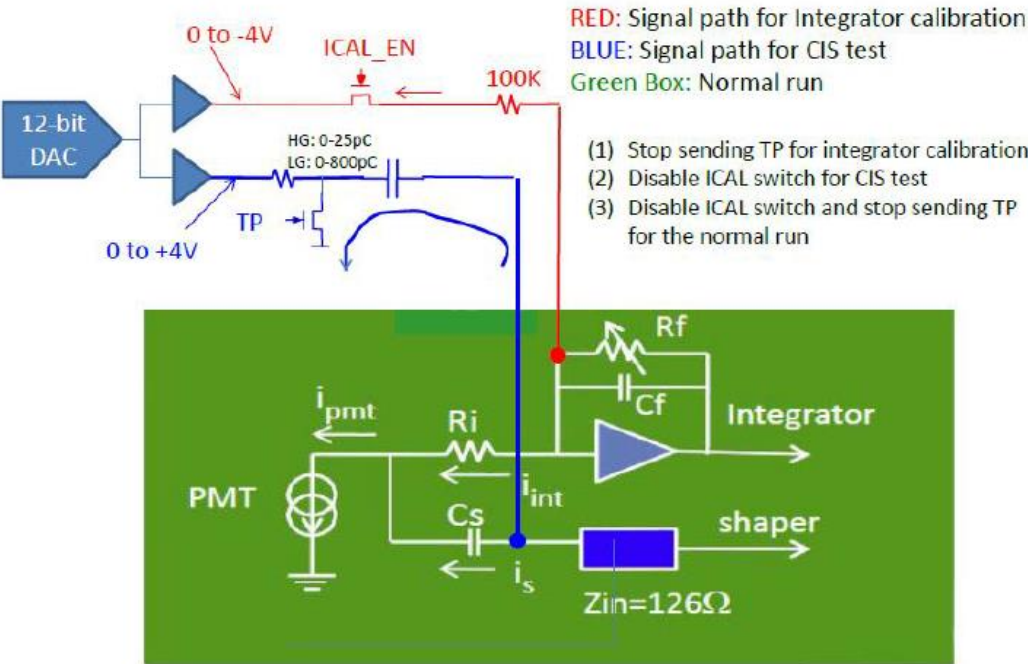
$$T = 10 + RC \text{ in ms, with } C = 0.1 \cdot 10^{-9}$$

From Ilya (Present 3-in-1): R from 2.7 to 100 MΩ

⇒ 10.27 ms to 20 ms. (Ilya said 10.3 to 20).



Integrator and CIS Calibrations and Normal Run



PMT Current Distribution over Shaper/Integrator

Case I: Cs calibration ($f < 17\text{Hz}$)

$$\omega \ll \frac{1}{(R_i + Z_{in}) \cdot C_s}$$

$$I_s \rightarrow 0$$

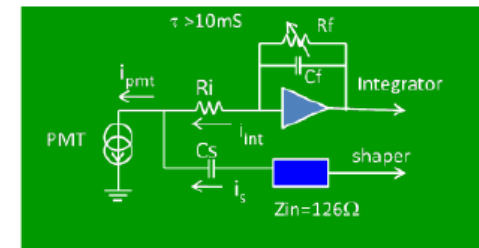
$$I_{int} \rightarrow I_{pmt}$$

Case II: Minimum current bias:

$$\omega \gg \frac{1}{(R_i + Z_{in}) \cdot C_s}$$

$$I_s = I_{pmt} \cdot \frac{R_i}{R_i + Z_{in}}$$

$$I_{int} = I_{pmt} \cdot \frac{Z_{in}}{R_i + Z_{in}}$$



R_f : sets integrator gain (6 settings).
 $R_f C_f$: suppresses output ripple.

PMT has an output capacitance of $< 40\text{pF}$, it is not shown in above schematic and formulas.

For $R_i=100\text{K}$, $C_s=0.1\mu$, $Z_{in}=126$, $\omega = 100\text{rad/s}$.
 Shaper cut-off frequency: **1.4KHz** at low end.

■ Performances

Present ATLAS scheme (from TIPP 2011 Chicago)

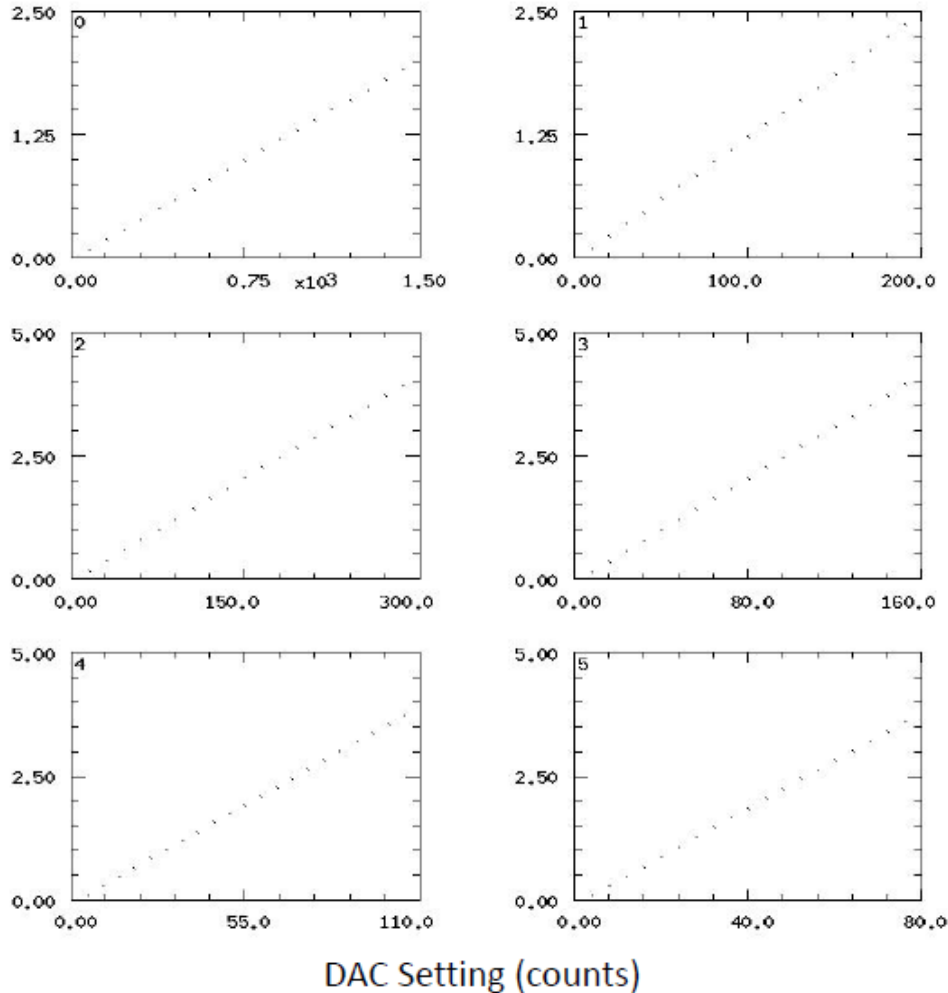
- Range **0.01 nA**-1.4 μ A.
- Non linearity < 1%.
- 12 bit ADC.
- Signal noise **0.003 nA**

Not credible
(never demonstrated)

The PMT dark current is ≤ 2 nA at 800 V, well above this noise !

Upgrade scheme

6 Integrator Gain Settings



- 6 gains ... **not given in current**
(as for the present ATLAS)

0: 0-750 } 0-2.5 V
1: 0-200 }
2: 0-300 }
3: 0-160 } 0-5.0 V
4: 0-110 }
5: 0-80 }
DAC
counts

- Does not correspond to python soft
sent by Kelby very recently
maxval = [3200,180,300,120,160,90]
minval = [64,6,4,4,4,9]

For times > 20 ms \Rightarrow summations

Example of a reply of Ilya to a question of FV about current of 0.5 nA in the current ATLAS scheme.

Hi Francois, yes, these points are averaged over about 10 measurements each having the int.time of 20ms.

So effectively the int.time is about 200ms on this plot.

Best,
Ilya

On Fri, Apr 8, 2016 at 1:20 PM, François Vazeille <vazeille@clermont.in2p3.fr> wrote:

Hello Ilya, looking at your very interesting and useful talk on the Cs system, I have a question about the VdM scan through the cell A13 (slide 6) where you measured a current of 0.5 nA.

What was the integration time of this measurement?

Did you add several measurements in order to increase the integration time?

With my best regards,
François

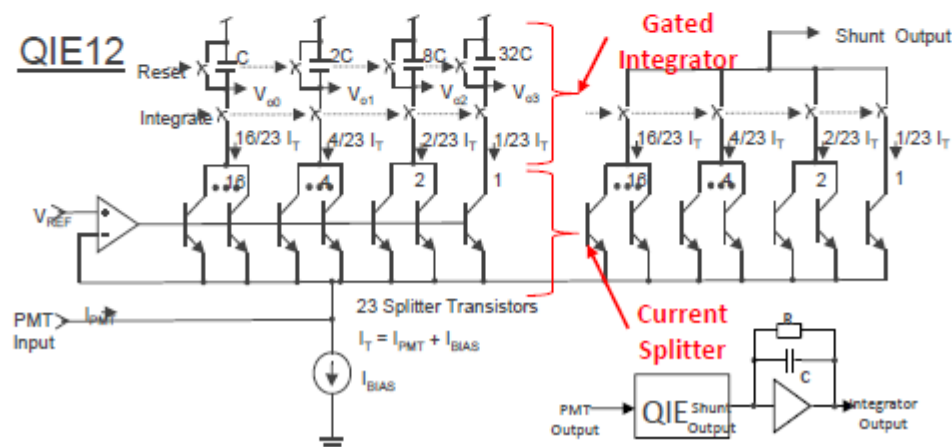
• Argonne integrator

■ Up to 8 μA : external

$\geq 40\%$ signal used

■ Current Integrator Part 1: External Circuit

- Uses the Shunt Output Circuit on the QIE
 - The Dump Circuit is another set of splitter transistors that can be switched in through the slow control interface to the chip
 - Up to 60% of the input current can be diverted to an output pin. The integrator circuit would receive as low as 40% of the collected charge.
 - The saturation of the QIE is 875 pC/25 ns when the current splitter is turned on.
 - Everything works as specified. The electronic noise with the splitter enabled is < 2 fc.
- Digitization
 - The shunt current is processed & digitized by an external integrator, 16 bits
 - The maximum range will be ~ 8 μA - \sim les than half of Range 0 Range of the QIE

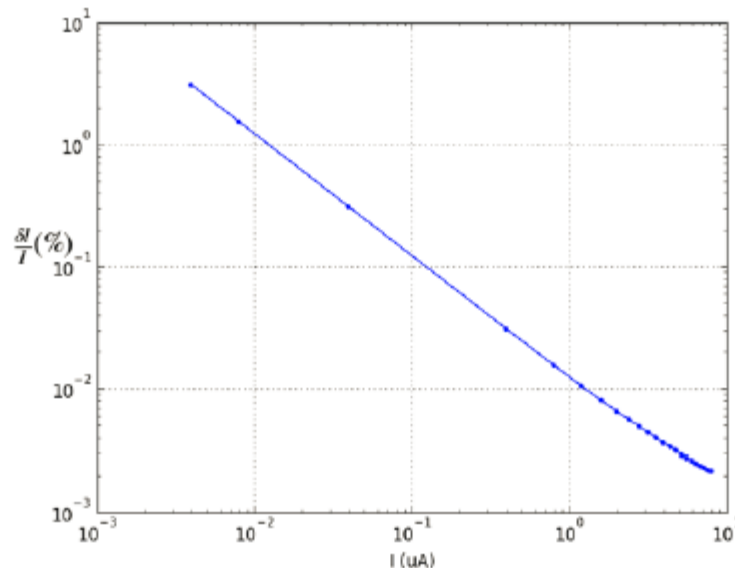


- Integration time of 2 ms, but will be fixed later at a constant value (10 ms ?).
- 16-bit ADC range, having 122 pA/count \rightarrow That does mean it is the accuracy.

■ Above 8 μA : internal from digital sum

■ Current Integrator Part 2: Digital Integration

- For currents above 8 μA , will use Digital Integration of the QIE data
 - Digital integration simplifies the design on the analog integrator (fewer ranges).
 - The fractional uncertainty for the digital is less than 0.2% for currents $> 0.1 \mu\text{A}$ ($\mu=2.5$).
 - This is easily implemented in pre-processor (along with the Look-up Table for the QIE data)



- It is a simulation.
- The integration time is not indicated, but it is 10 ms from Ilya.

- This plot goes up to 6 nA, but with an error of about 4%.
- 0.2% above 100 nA **but the noise level is very optimistic.**
- Used in fact above 8 μA .

• Clermont-Ferrand integrator

- Accuracy calculations on digital sum from the present noise performance
- Noise over the whole frequency spectra: 8 fC. (and not 7 fC HF noise only).
- For a realistic pulse shape (triangular), it corresponds to 400 nA, or 50 nA/fC.
- A "sum number" of 1 corresponds to the sum of 400 000 samples at 40 MHz.

	Cell value	Time (ms)	Sum number	Accuracy %
Cesium scan	A to D 60 nA	10	1	1.05
	A to D 90 nA	10	1	0.70
	E1-E2 < 4 nA	10	2	> 11.2
	E3-E4 ~ 0.06	Impossible, no Cs		
	Limit 1% 63 nA	10	1	1.0039
	Limit 1% 45 nA	10	2	0.9938

- For cesium scan, OK for A to D above 45 nA with an accuracy of 1% or better.
- E scintillators are likely thicker than Tiles
 ⇒ a time > 20 ms could be chosen , but not too much.

- For Luminosity scans, larger times can be used.
- We must consider two extreme case: HL-LHC ($7 \cdot 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$) and vdM scans (some 10^{30}).
- For vdM scans, we take a time of 2 minutes imposed by Luminosity blocks.

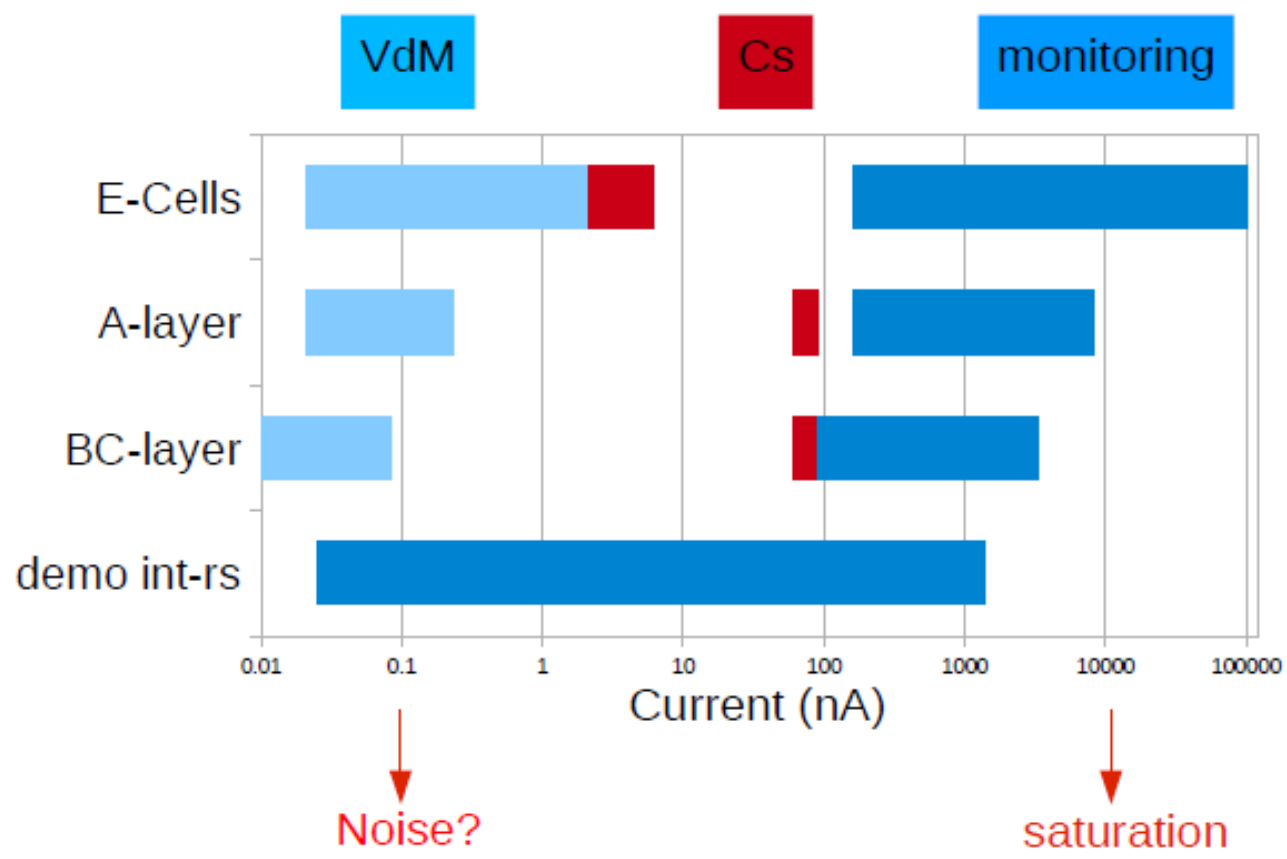
	Cell value	Time (ms)	Sum number	Accuracy %
Luminosity scan	HL minimum > 100 nA from (B-C)	10	1	< 0.63
	vdM A-B 0.02 nA	10	12000	28.9
	vdM A-B 0.05 nA	10	12000	11.5
	A, Limit 1% 0.58 nA	10	12000	0.9954
	A, 3% 0,192 nA	10	12000	3.007
	A, 5% 0.115 nA	10	12000	5.02

- No problem for HL scans, up to the 100 μA value on E cell without saturation.
- vdM scan possible for A cells with an accuracy $\geq 3\%$.

■ Requirements on Analog measurements

- ◆ For Cesium scans with times of 10 or 20 ms
 - Must overlap the Digital approach \Rightarrow Maximum value of 150 nA.
 - Must reach low values up to some nA for E1-E2.
- ◆ For Luminosity scans at Low Luminosity:
 - to reach 0.05 nA in order to scan the B cells with an accuracy of 3% over durations of 2 minutes.

Dynamics from 0.05 nA on means to 150 nA in 10 or 20 ms.



- TileCal data for the Cesium source moving

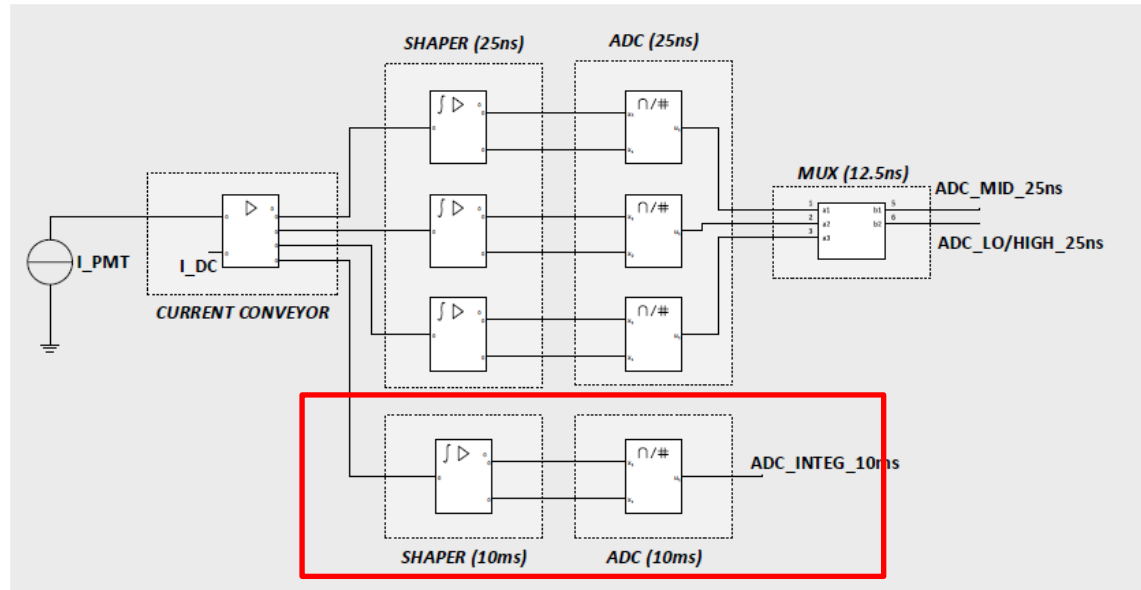
- Recommendations from Ilya's talk

- Check-List for any system to replace the current integrators**

- How do you transfer the EM scale, what would be the error?
- Do you do Cs as good as before, 1% per measurement (10ms)?
- Do you do Cs in E1&E2 to 1% accuracy on integral?
- can you measure the currents upto 8uA (in A cells) and upto 100uA in E cells?
- can you monitor the currents down to 0.02nA (w 1% per lumi block noise)?
- can you have linearity (after all the corrections) between 1nA and 8uA within 1%?

■ Our specifications for the Analog approach

- A fourth current copy with the ADC inside the chip.
- A DAC calibration via current injection.



- Possibility of 2 integration times: 10 ms and 20 ms.
- Is it possible to use the same DAC ?
- Dynamics for Cesium scans
 - Maximum: 150 nA.
 - Minimum: 0.5 nA for E1-E2 cells.
- Dynamics for Luminosity scans
 - Maximum: no constraint \Rightarrow we keep 150 nA and saturation accepted above.
 - Minimum: means are possible over 2 minutes \Rightarrow to reach 0.05 nA.