First noise measurements in the FATALIC option

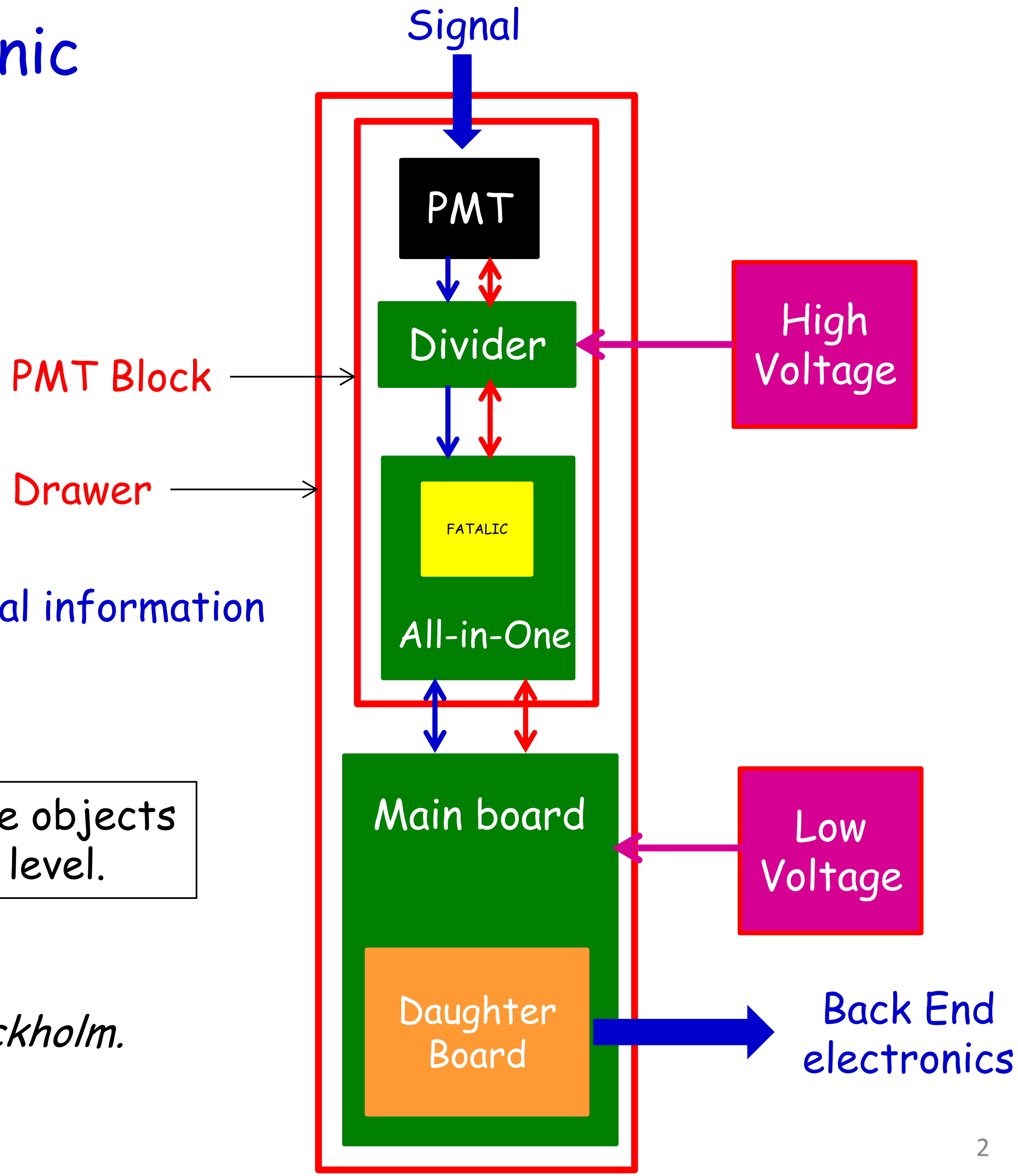
Monday ATLAS/LPC Tile meeting
Roméo Bonnefoy, Dominique Pallin and François Vazeille
on behalf of the LPC team
2016 April 4

- The main electronic components of the readout
- Performance specifications on electronic noise
- Summary of various step studies
  and present results from 3 All-in-One cards
- Conclusion and next actions

From talk given at the Wednesday Tile Upgrade meeting of March 23

Reminder: there are 2 other concurrent options to FATALIC
- Chicago: evolution of 3-in-1 cards with discrete components, linear.
- Argonne: QIE option, with evolution of CMS asic, non linear.

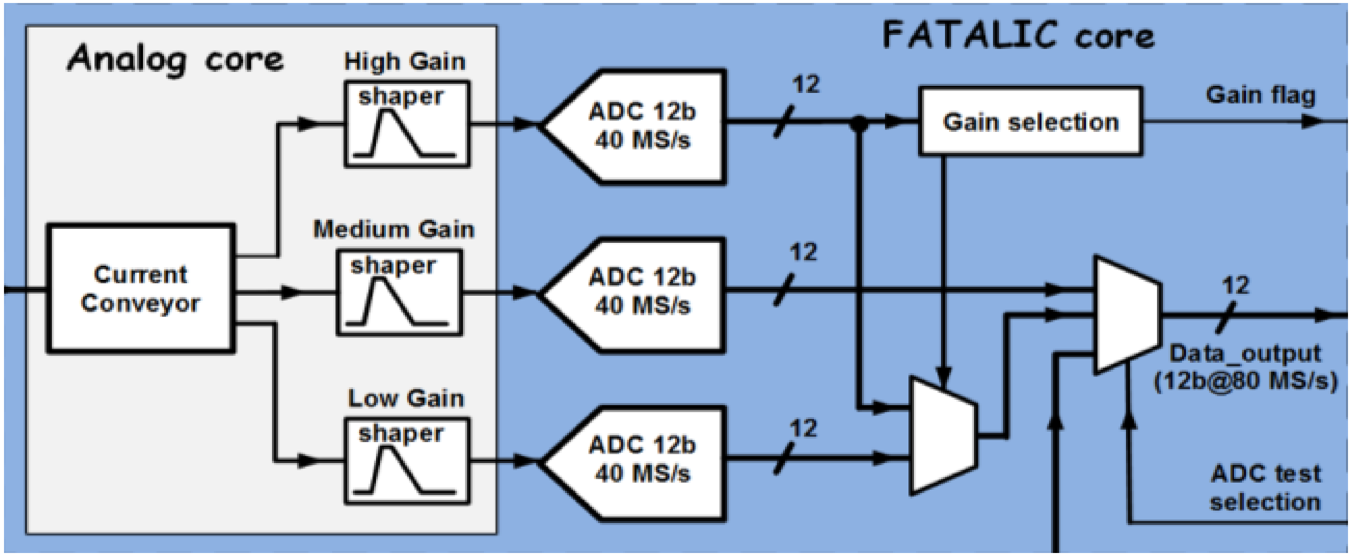
The main electronic components of the readout



In blue: Signal and/or digital information
In red : Grounding aspects

We will play with all these objects to minimize the noise level.

Daughter Board: Stockholm.
Back End: Valencia.



- *FATALIC has 3 gains (High: ~64, Medium: ~8, Low: ~1).*
- *A 12-bit ADC per Gain.*
- *Rough ranges:*

  High : "0" to 17.5 pC ← "0" means electronic noise

  Medium: 17.5 to 140 pC

  Low : 140 to 1200 pC (and even above without saturation),

with overlaps of the Medium gain with the others.

Performance specifications on electronic noise

[From Performance Specifications for the ATLAS TileCAL Front End Electronics sLHC Upgrade Environment, The TileCal group (March 24, 2009)]

"4. Electronic Noise

The intrinsic noise of the electronics, as measured through the digitization path, expressed in terms of equivalent input charge, shall not be greater than 12 fC RMS at pedestal."

It is justified by the rule of an electronic noise being half the minimum charge of interest of 24 fC corresponding to 1 photo-electron.

$\Rightarrow$ This constraint of **12 fC RMS** was a main issue in the design of FATALIC and in its implementation in the whole readout inside a Mini-Drawer.

It is impossible to find this paper on the web !

- *This paper is in the indico agenda.*
- It should be put on CDS as an official ATLAS reference.

"1. Smallest Signal to Measure

The smallest signal of interest from the detector, expressed in terms of equivalent input charge delivered to the front end electronics, is 24 fC.

Discussion: *The minimum hadronic signal of interest from the detector is a muon with energy 20 MeV, which produces 1 photo-electron delivered to the photo-multiplier tube. The photo-multiplier tubes operate at a nominal gain of ~1.5E5. The minimum charge signal of interest is thus 24 fC.*

Q_{min} *= 1 photo-electron * 1.5E5 pmt gain * 1.6E-19 Coulombs/electron = 24 fC"*

In this well documented document, the PMT gain is 1.5 10^5 instead of 10^5

WHY ?

*If we set 10^5, the electronic noise request should become **8 fC.***

ATLAS
Upgrade Workshop

A Systems Perspective of the TileCAL Electronics

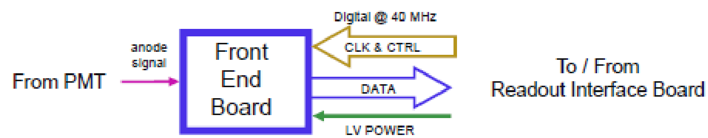
Gary Drake
Argonne National Laboratory, USA

In Collaboration with
The University of Chicago

CERN
Feb. 25, 2009

Gary Drake talk on performances

The Front End Board



- Performance Requirements (partial listing)
  - 20 MeV – 1.3 TeV (12 fC – 800 pC) → 16 bits dynamic range
  - Noise: < 24 fC (2 counts)
  - Pulse shaping – 7 points/event, 2% uniformity in transfer function
  - Integral nonlinearity: < 2 ADC counts
  - Differential nonlinearity: < 1 lsb
  - On-board charge injection – 1% uniformity, 0.1% repeatability
  - Radioactive source current monitor – 0.2% uniformity

It is no longer the same specification:
2 times more
and even 3 times above:
WHY ?
Easier to reach ?
Pure QIE approach ?

A Systems Perspective of the TileCAL Electronics
ATLAS Upgrade Workshop – G. Drake – Feb. 25, 2009 – CERN 7

Main interests of having a very low noise,
with the rule: it must be at most half the last significant physical value.

1. To fit the PMT performances: measurement of a single photo-electron
   $\Rightarrow$ 8 fC for a PMT gain of 10^5, 12 fC in the TileCal paper.

2. To measure muons in the smallest cells (350 MeV),
   with a ratio signal/noise > 10 on a single PMT.
   - 1 PMT   350/(10x2) MeV = 17.5 MeV.
   - 1.15 pC/GeV for muons $\rightarrow$ 20.125 fC.

   If we take larger cells (D cells), the energy (the charge) will be bigger.

3. To perform Cs calibrations of every cell ($\rightarrow$ current measurement in 10 ms),
   to contribute to the LHC Luminosity measurements ($\sim 10^{34}$ $cm^{-2}s^{-1}$),
   and even better to the vDM (van der Meer) low Luminosity calibrations (10^{30} $cm^{-2}s^{-1}$),
   via pulse mode or current measurements, at least on A and B cells.
   $\rightarrow$ Signals at a level of 1 photoelectron $\Rightarrow$ noise of 8 fC.

Lower currents

Main objectives of the FATALIC readout

1. An electronic noise $\leq$ 12 fC on the High Gain.
2. An external RMS noise < intrinsic noise.
3. A noise practically independent from the environment.

From the point 1 to the point 3,
these goals will be more and more difficult to reach.

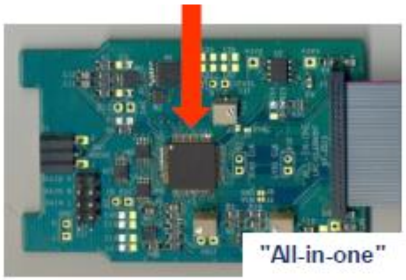
… and why not to be better than 12 fC.

Noise study started **beginning of January** while first results were **disturbing**
→ Empirical and systematic studies of trouble sources.

Summary of various step studies and present results from 3 All-in-One cards

- Long systematic study, step by step, with improvements

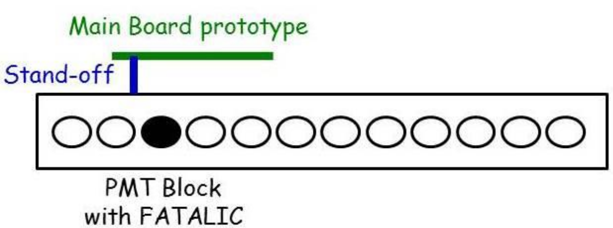
FATALIC



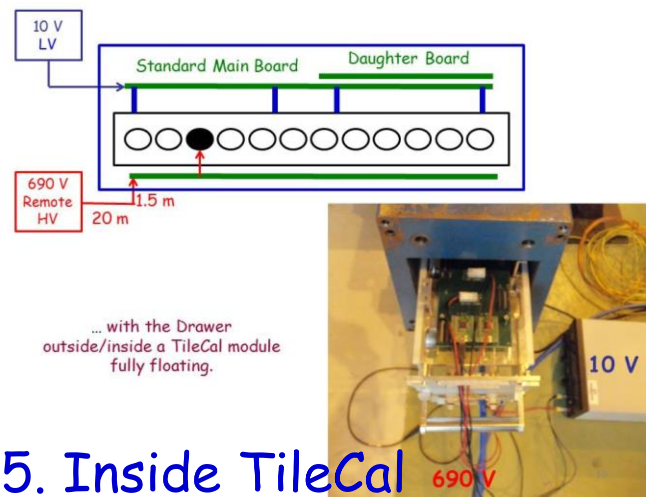
1. Alone

2. Inside PMT Block

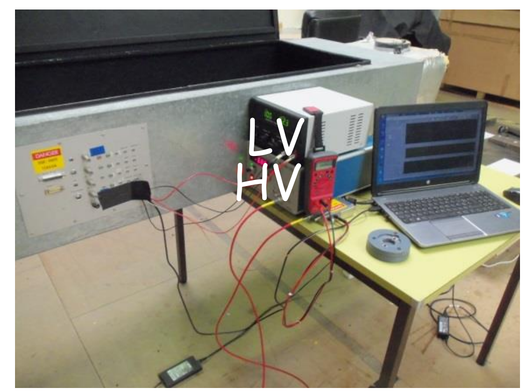
3. Inside FATALIC Test Bench



4. Inside Drawer
+ Main Board proto



5. Inside TileCal at CERN
+ Main Board
+ Daughter Board

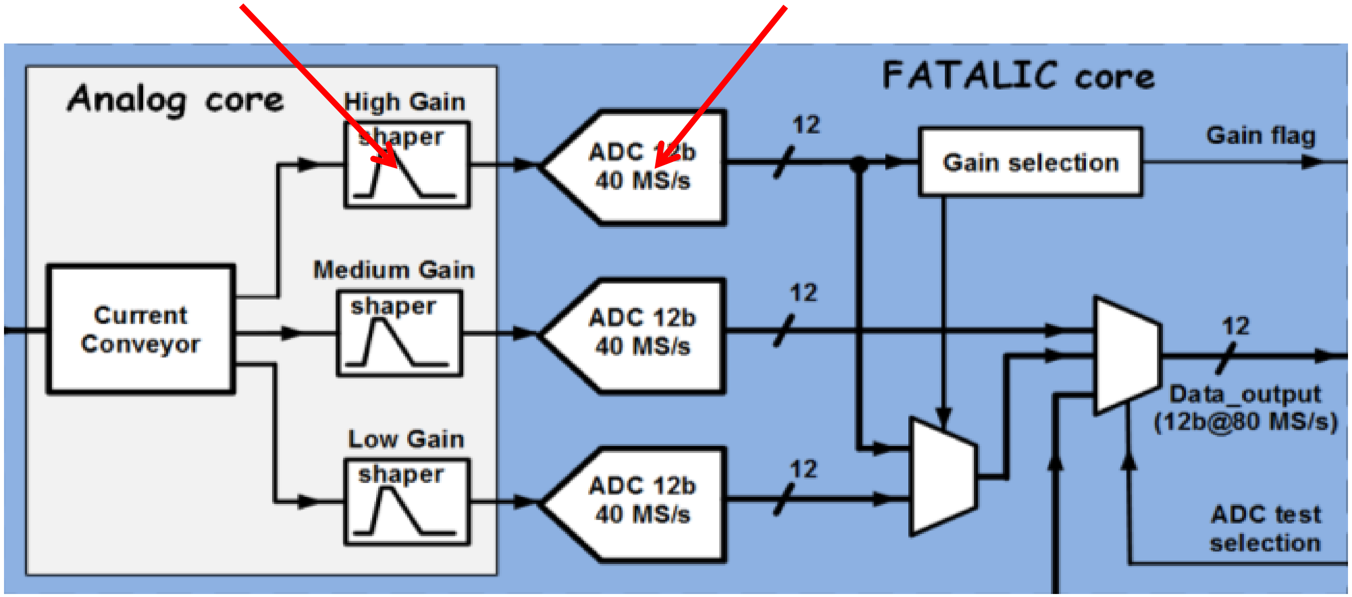


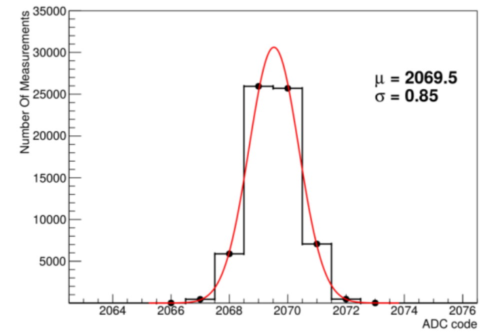
6. Inside Large box at LPC
+ Main Board
+ Daughter Board

- There was a step 0 (Laurent Royer, TWEPP 2015 Lisbon) intrinsic noise estimates from simulations of FATALIC alone.

High Gain noise:
2 ADC counts

ADC noise:
0.85 ADC count





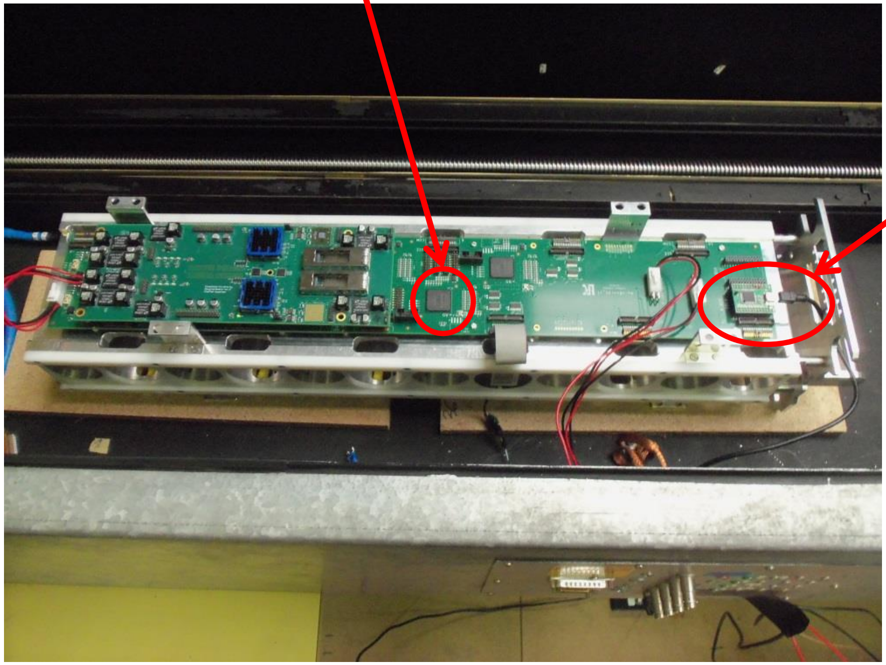
ADC noise

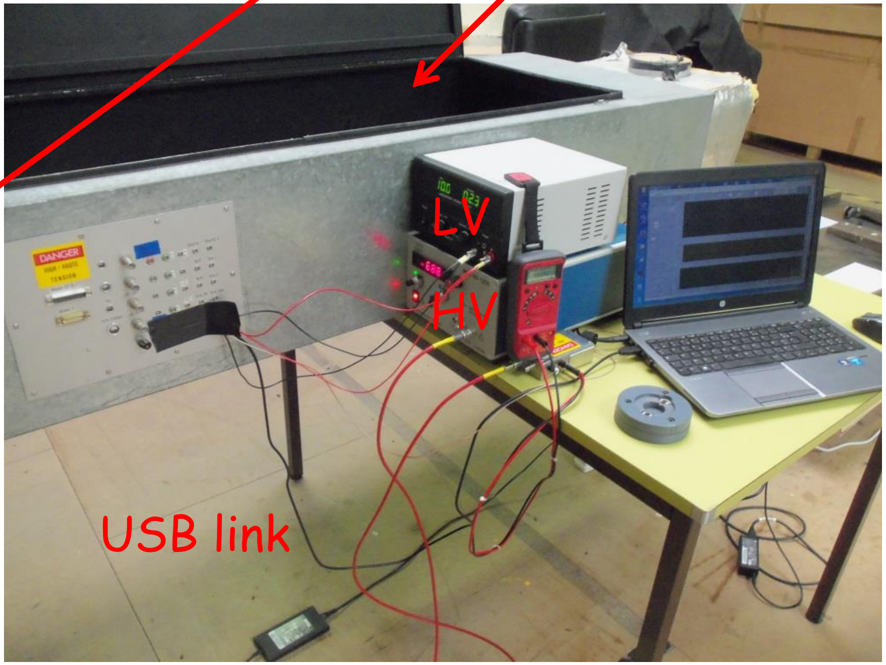
Total noise (quadratic sum) = **2.2 ADC counts** for the High Gain or **5.5 fC**.

• Experimental set-up (Example of Step 6):

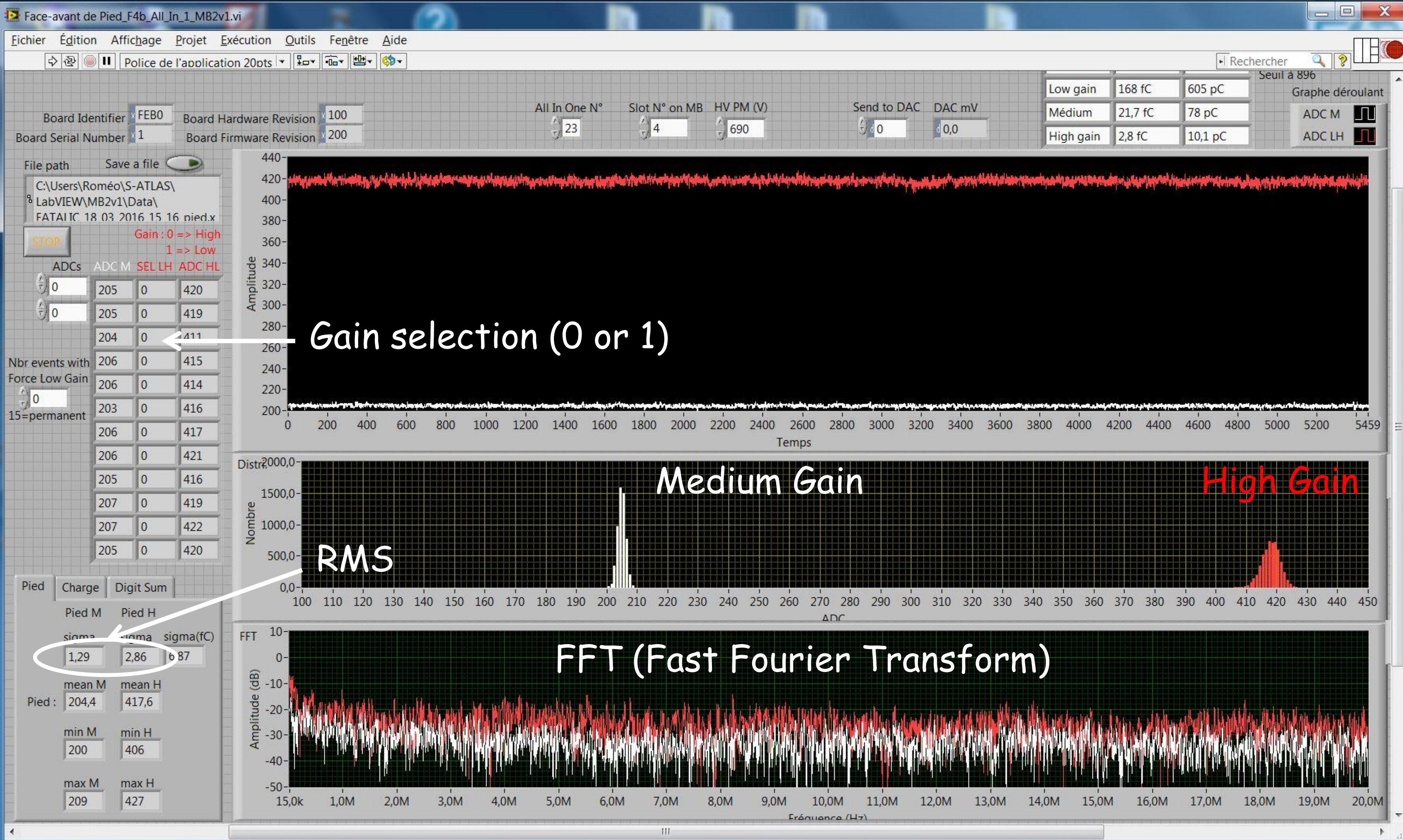
PMT Block-Drawer-Main Board-Daughter Board inside a Big Test Box + LV/HV powers + laptop

FPGA memory of Main Board read out by USB interface





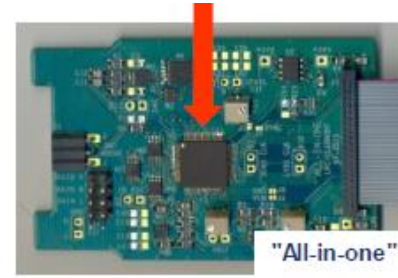
Monitoring and data recording by LabVIEW on laptop



- Data: 5460 samples at 40 MHz.
- Frequency spectra: 136.5 μs range $\rightarrow$ 15 kHz to 20 MHz (Shannon theorem).
- RMS accuracy: ~ 0.15 to 0.20 ADC count.
- Charge calibration: 1 ADC count = (2.40±0.05) fC.

- Step 1: All-in-One alone

FATALIC



All-in-One#	13	15	23	21	Mean
Noise (ADC counts)	2.7	3.0	3.0	2.7	2.85±0.17

- Measured intrinsic noise not far from simulation of 2.2 ADC counts.
- Equivalent noise in charge units: 6.84±0.43 fC

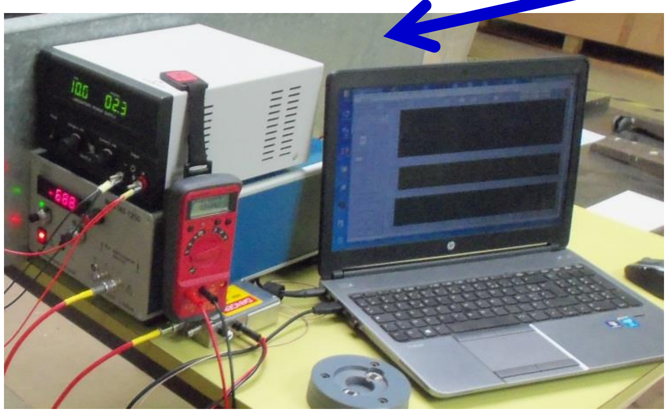
Comments:
- The USB link can manage only 3 channels.
- Cards #13, 15 and 23 were used up to Step 5,
but in Step 6, #23 was killed … and replaced by #21.

Grounding aspects: what will be the effect of the environment and how to cure the noises coming from it ?

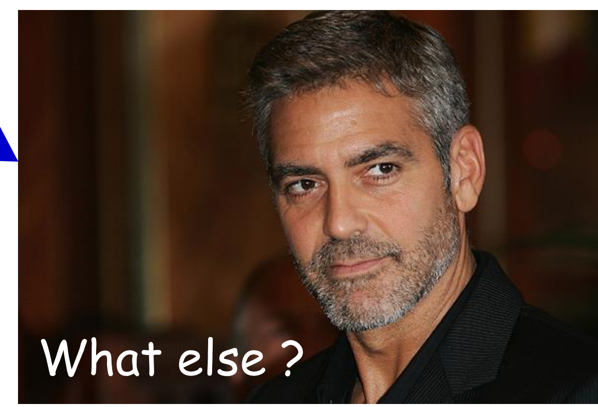
PMT Block+Drawer+Main Board+Daughter Board

Test Box

LV+HV+Laptop



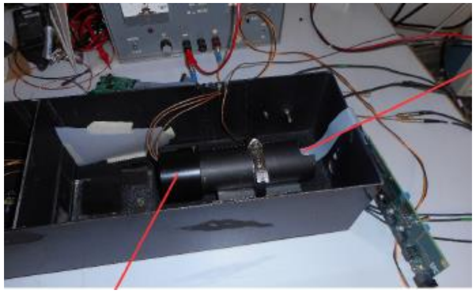
The operator



Many "things" around FATALIC

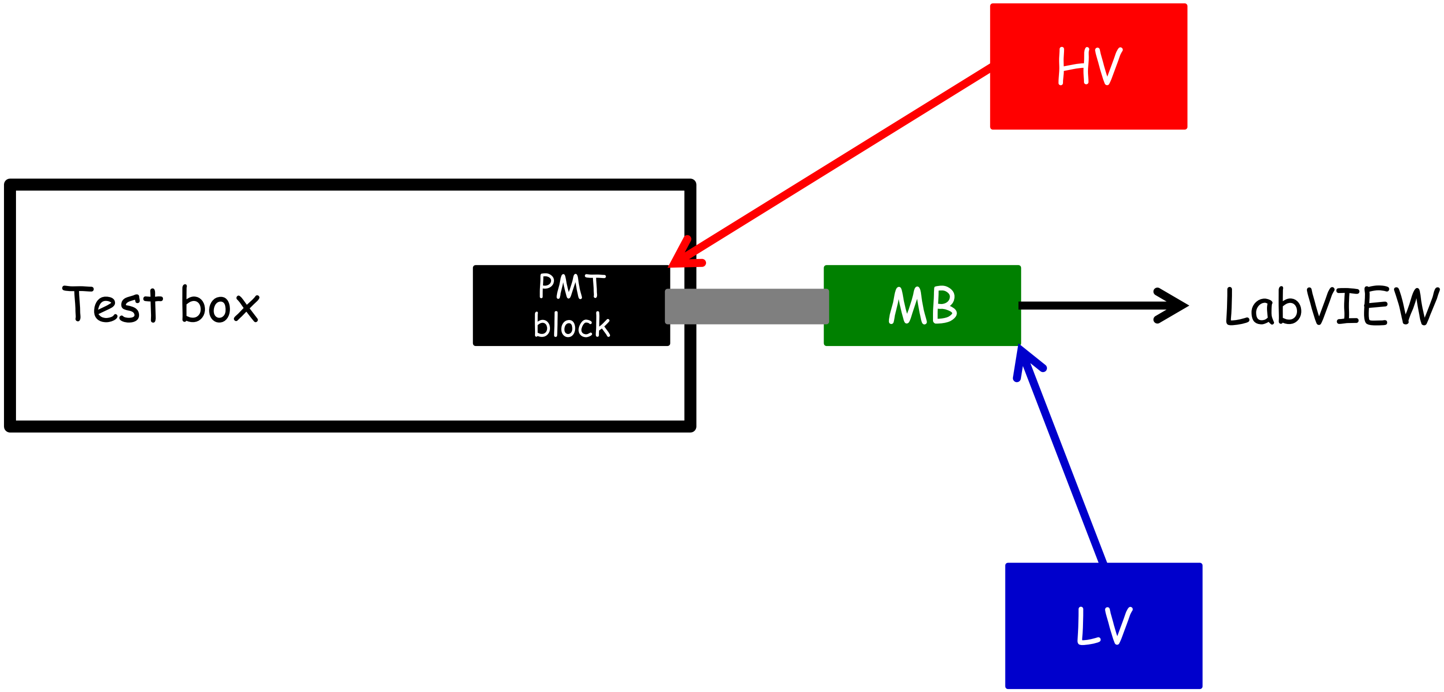
- Steps 2 and 3:
  PMT Block alone
  and inside FATALIC test box

PMT Block

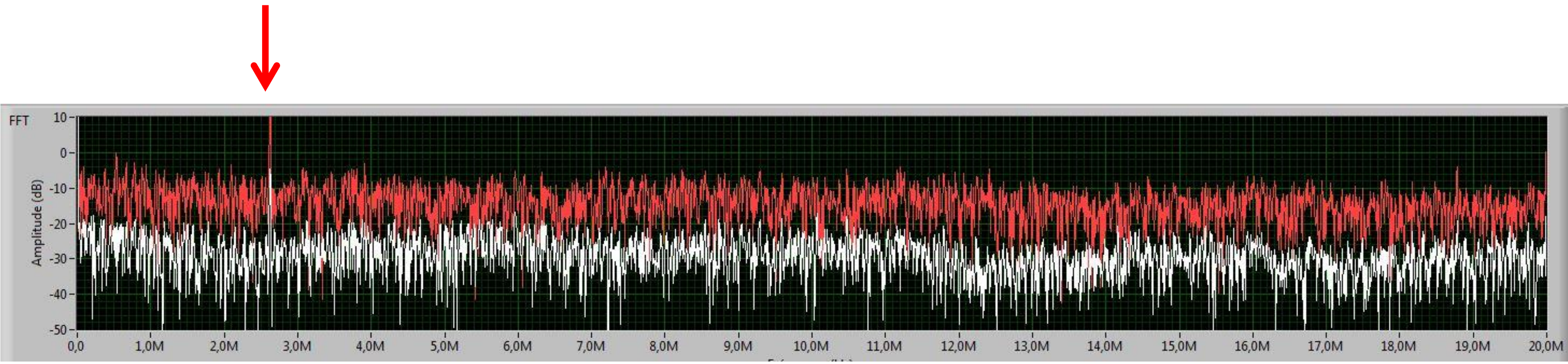


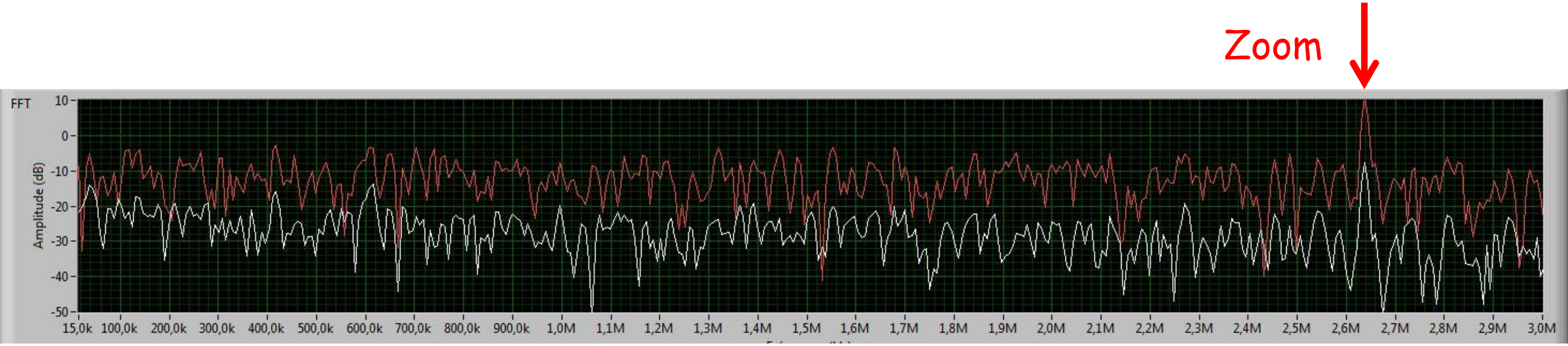
Test Bench

- Dramatic:
- Intrinsic noise increased about 4-5 times when connecting the PMT/Divider.
  + Noise peak at 2.6-2.7 MHz.
- Big sensitivity to the environment: position in the Test Box, cover or not…



Peak at 2.6-2.7 MHz

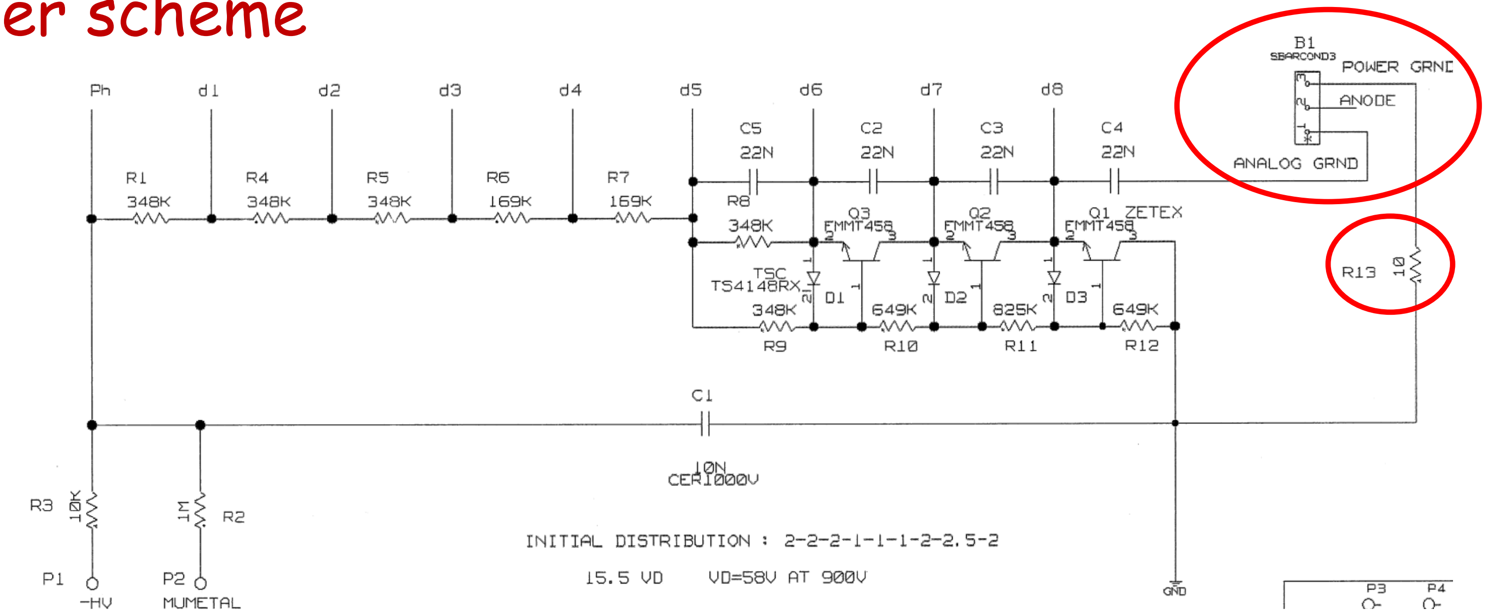




Other peaks arose also at any moment

Theoretical approach

Divider scheme



2 different grounds:

- Analog ground → FATALIC ground
- Power ground → HV ground

} With a 10 Ω resistor connection

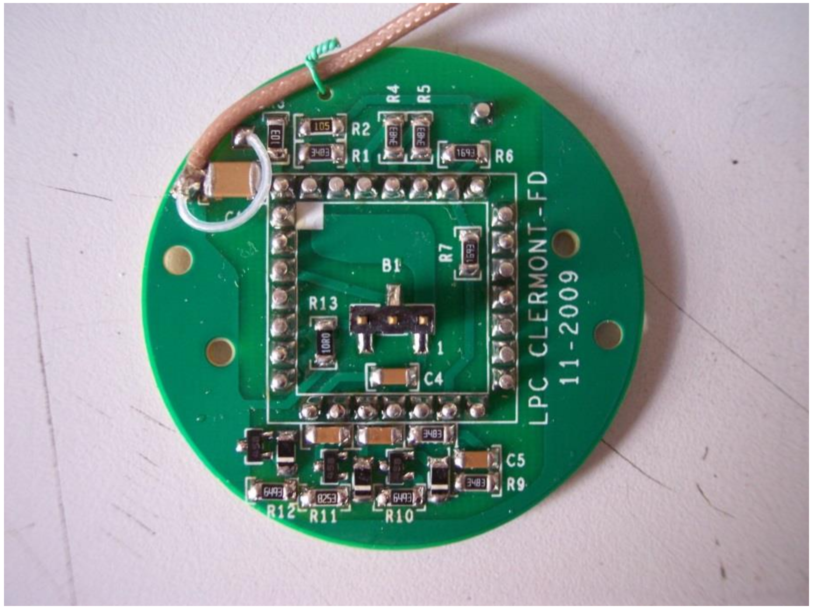
- Official ATLAS divider scheme.
- Not suited to a current readout: case of FATALIC with current conveyors.

Comments:

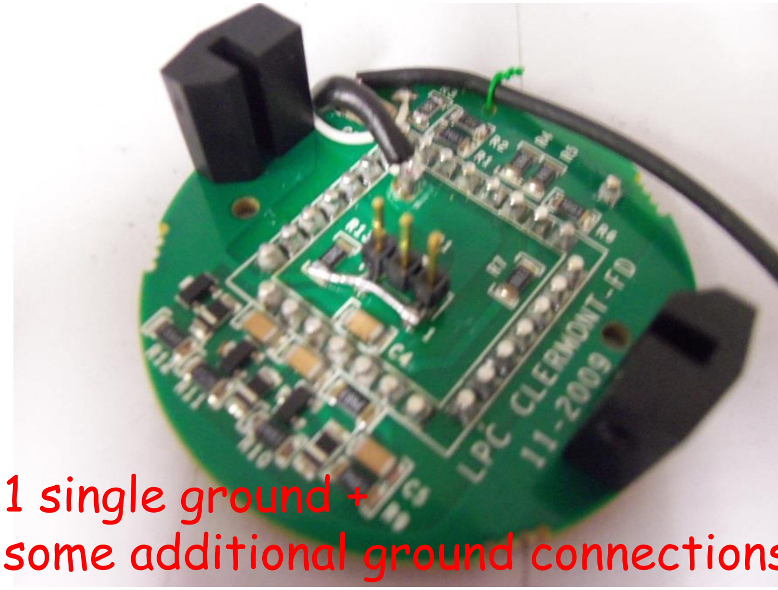
- These 2 grounds resulted from long studies in the Test Beam, in order to mitigate the noise increase from channel 1 to channel 48 (close to patch panel).
- We have just discovered that the present Chicago 3-in-1 cards connected these grounds, whereas the 11 000 produced passive Dividers had the 2 grounds.
- I do not remember when this change was performed.

- We decided to connect these 2 grounds (to suppress the 10 Ω resistor) then to compare 3 kinds of active Dividers, with more or less additional grounds.
- We implemented the usual "Noise killers" (Filter with 1 kΩ resistor on the HV power and on the return).

1. Standard Divider



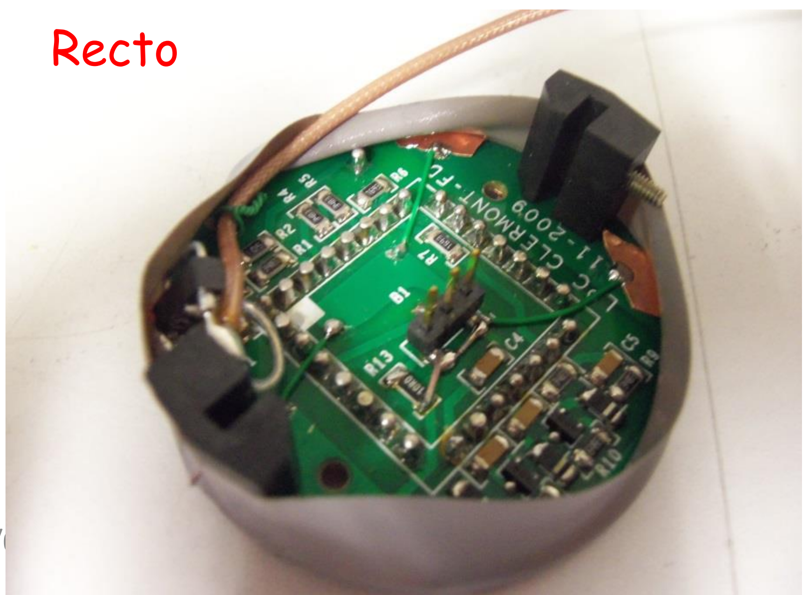
2. Modified Divider



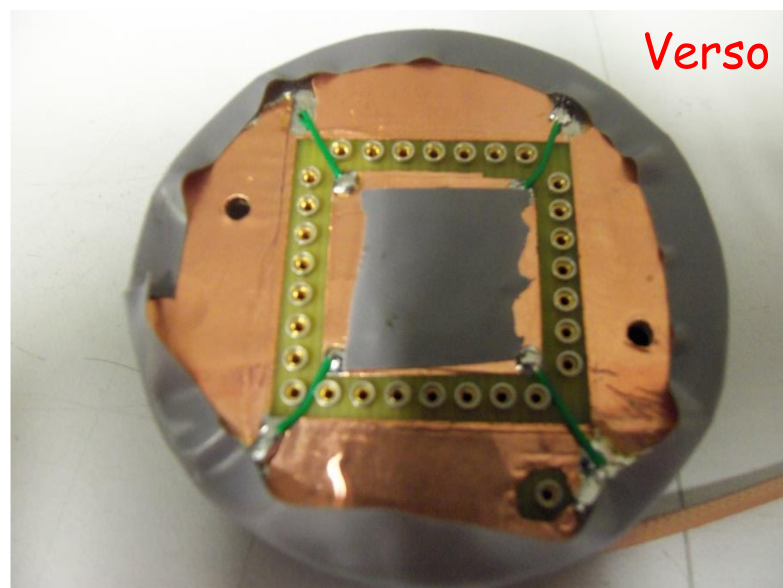
1 single ground +
some additional ground connections

3. Modified Divider + new grounds

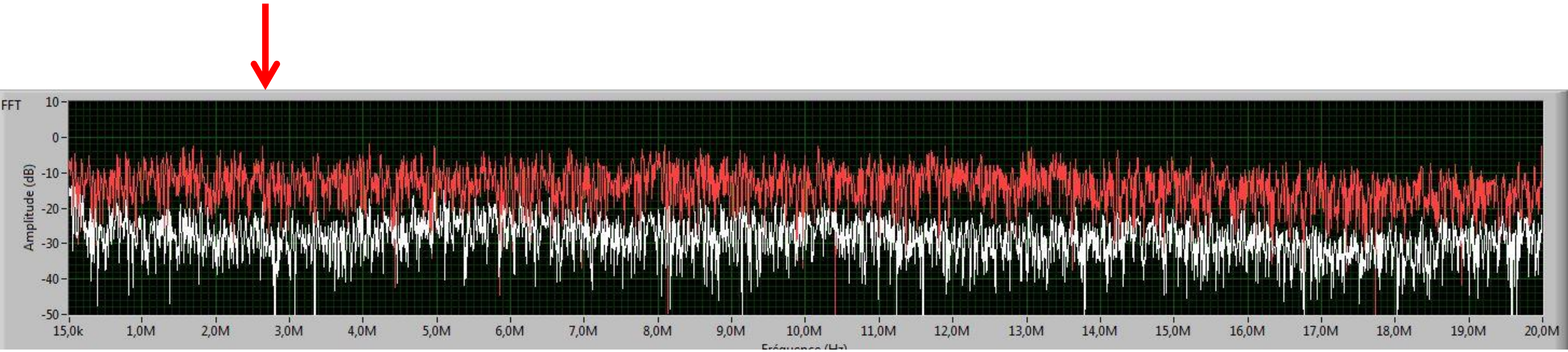
Recto



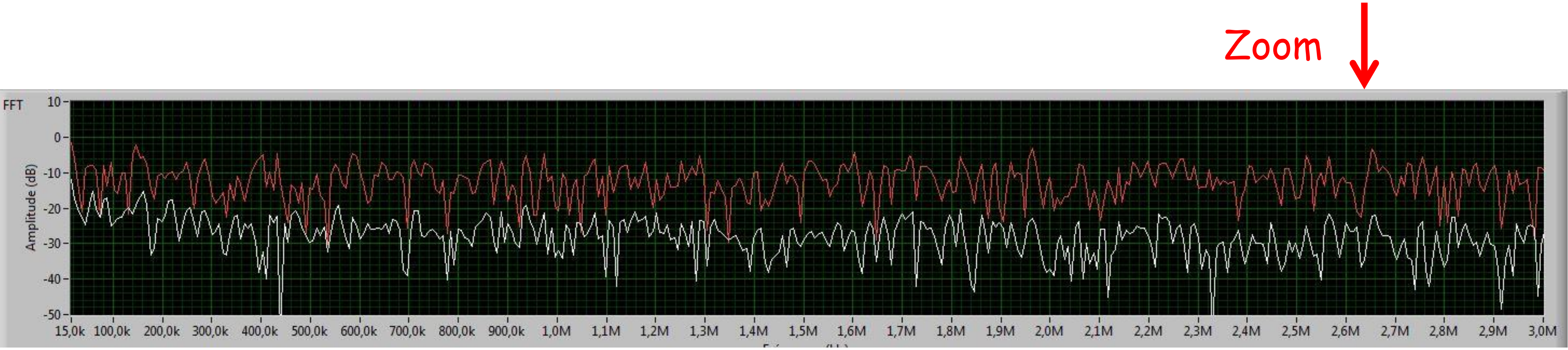
Verso



Effect of Noise killer: kills Peak at 2.6-2.7 MHz



Zoom



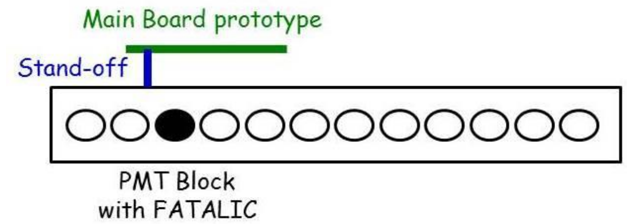
- Tests with All-in-One # 13, 15 and 23.
- Results in ADC counts.

Divider			Standard	Modified	More grounds
PMT block outside	Body floating		13.52 ± 3.44	3.77 ± 0.40	3.75 ± 0.25
	Body grounded		5.67 ± 0.74	4,75 ± 1.04	4.88 ± 1.66
PMT block inside test box	Body floating	Close wall	16.35 ± 1.96	4.47 ± 0.47	4.32 ± 0.24
		Far wall	17,17 ± 5.02	4.67 ± 0.42	4.15 ± 0.22
	Body grounded	Close wall	5.05 ± 0.62	6.50 ± 1.60	5.83 ± 1.01
		Far wall	7.63 ± 1.57	6.02 ± 1.63	5.60 ± 1.23

- **Obvious** effect of a single Divider ground.
- **No clear difference** in between modified and more grounded Dividers.
- **Worst** in the Test box, with **sensitivity** to the PMT Block location.
- **Best results in box** with Body floating, with noise at a level of 10-11 fC

… but very uncomplete set-up !

- Step 4: inside Drawer with Main Board proto and a single Stand-off (Only 1 Drawer thread in front)



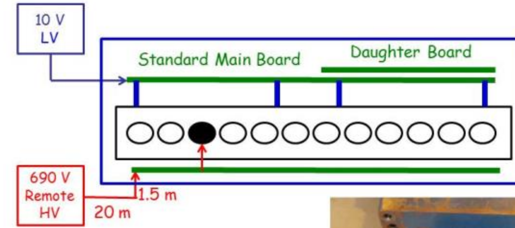
- Tests with All-in-One # 13, 15 and 23.
- Results in ADC counts.

Divider		Modified	+ More
Metallic stand off 20 mm	HV off	12.63±1.66	14.52±2.21
	HV on	13.25±1.84	14.45±2.66
Plastic stand off 10 mm	HV off	5.00±0.92	6.37±1.95
	HV on	5.02±1.04	6.40±2.00
Plastic stand-off 30 mm	HV off	3.88±0.58	4.57±0.95
	HV on	3.93±0.52	4.67±1.95

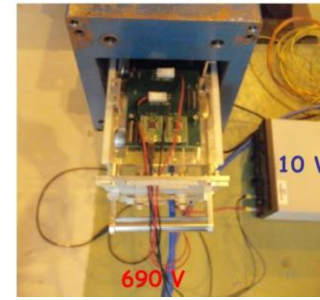
- A **unique** stand-off: ground loops in the case of a **metallic** stand-off ?
- **Increased** ground loops with the modified Divider with more grounds ?
- **Better** results with plastic stand-off',
  and better **far away** Drawer body: decrease of a **capacitive effect** ?
- **Low** effect of HV supply.

⇒ Must be **redone** with the complete Main Board and more stand-off's.

• Step 5: Whole set-up with Drawer inside a TileCal module at CERN



... with the Drawer
outside/inside a TileCal module
fully floating.



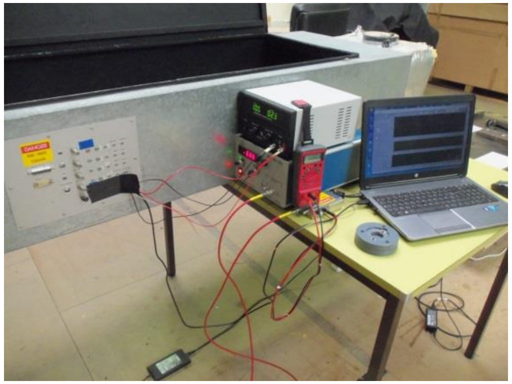
- During the February expert week.
- More stand-off's, but some are missing because of the Drawer thread locations.
- Test with only the All-in-One card #13.
- Remote HV with 20 m long cable.

Set-up			Inside Module	Outside Module
Plastic 10 mm	Modified Base + additional	HV off	6.5	5.9
	Modified Base	HV off	5.6/6.0	4.7/4.8
Plastic 20 mm*	Modified Base	HV off	5.3	4.6
Metallic 12 mm	Modified Base	HV off	4.8/4.6	7.8/6.8
		HV on	4.8/5.0	

- Results in ADC counts.
- / separates repeated measurements.
- * Drawer partially outside Module.

- **Better** results with **metallic** stand-off's: noise slightly below 12 fC.
- Drawer body/PMT Block/ MB/DB grounds at the **same potential**.
- **HV effect** within uncertainties.
- **Better** results with **modified Base** with not too much grounds.
- **Sensitivity to the environment**: inside/outside TileCal module.

- Step 6: Whole set-up with large Test box at LPC



- Goals:
  - To reproduce the CERN set-up.
  - To perform systematic studies with 3 All-in-One cards.

→ To bring new improvements if possible.

- Is it possible to reproduce at home what we had at CERN using the All-in-One #13 ? One example of the results:

Site	CERN	LPC
Daughter Board OFF	4.8/4.6	5.1-5.3
Daughter Board ON	4.8/4.6	5.3

Slightly better at CERN, but not far if we consider uncertainties of 0.15 to 0.20 ADC count and fatigue wear of connectors.

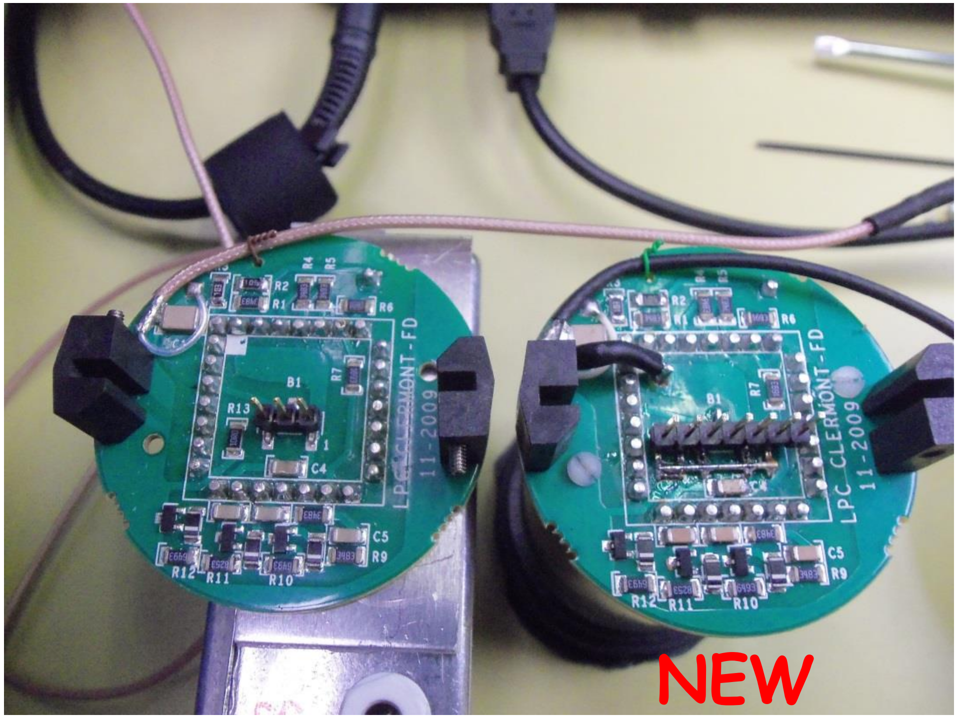
- Mounting/dismounting a lot of times the connectors damage the performance
  - ⇒ Suddenly, the noise reached 35 ADC counts !
  - ⇒ Can we find safer connectors ?
- During the tests, a bad mounting of the PMT Block destroyed the All-in-One #23
  - ⇒ Replaced by a new card #21.

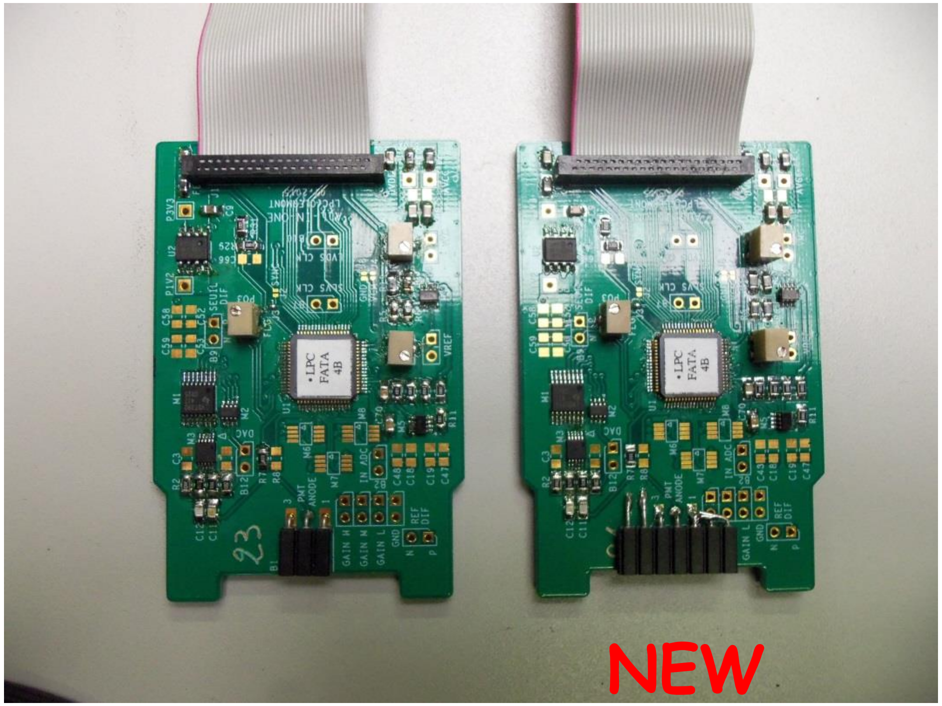
- New connectors on Divider/All-in-One cards

  - Previous scheme: 3 pin connectors (Central: anode signal, Sides: ground).
  - Changes: 7 pin connectors (Central: anode signal, Others: ground).

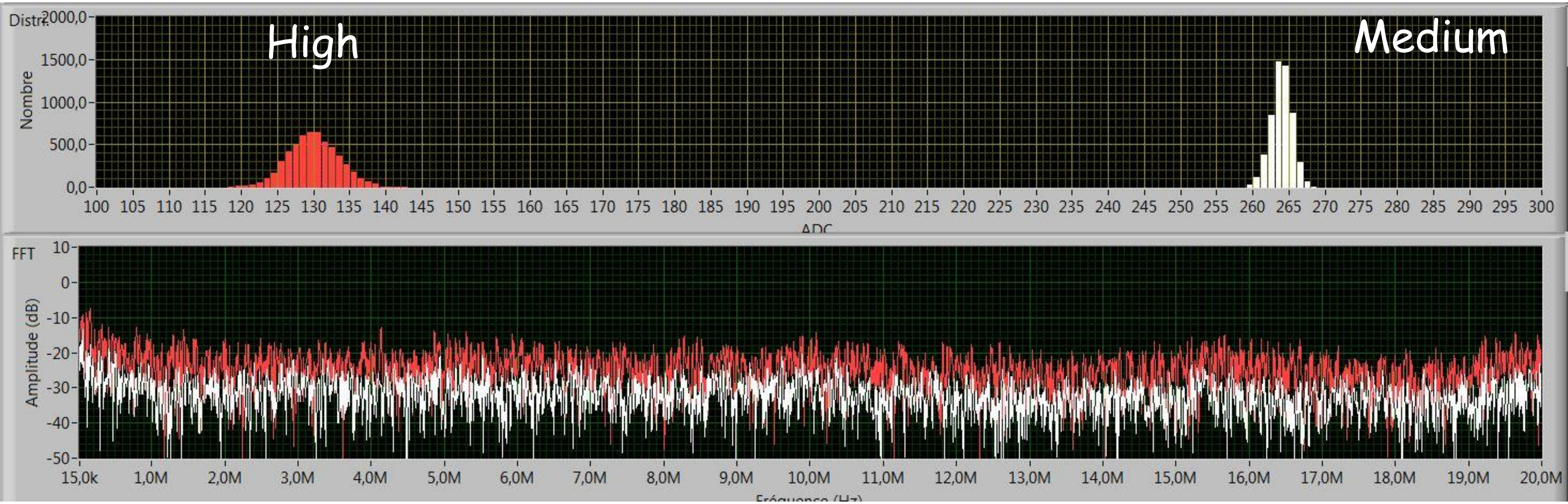
Comments:

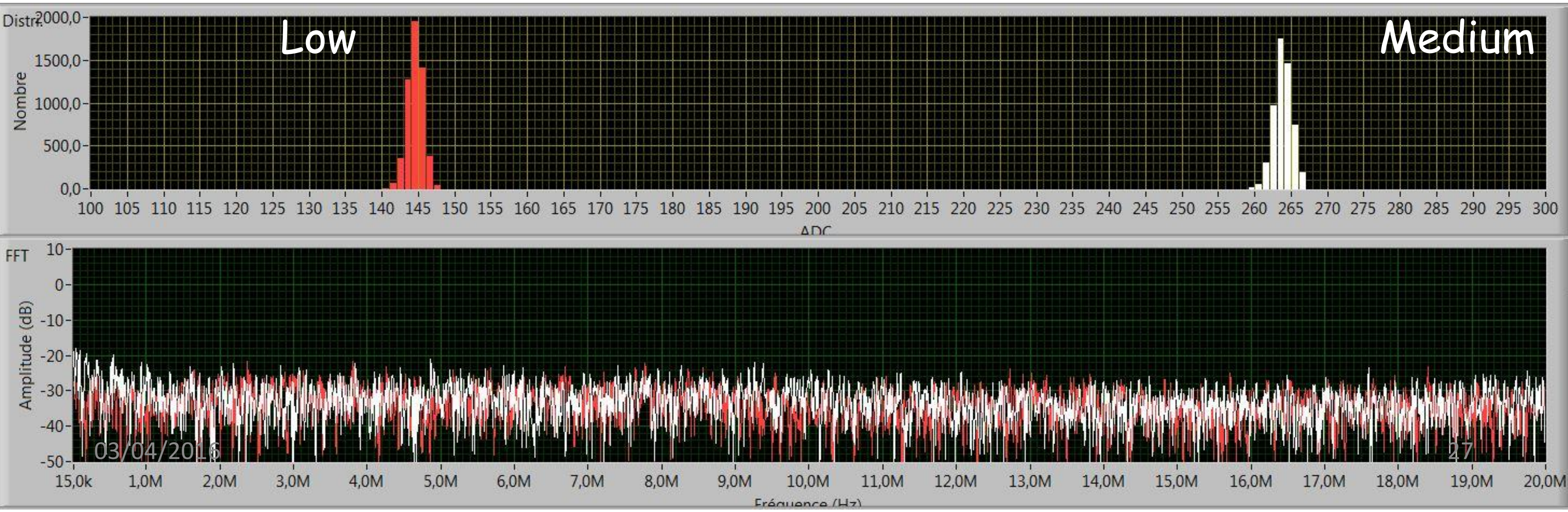
- *The Divider type is this one with common ground + additional wires, that gave the best results till now.*
- *The ground distribution is not perfect on the All-in-One board.*





Distribution and frequency spectra for the 3 gains





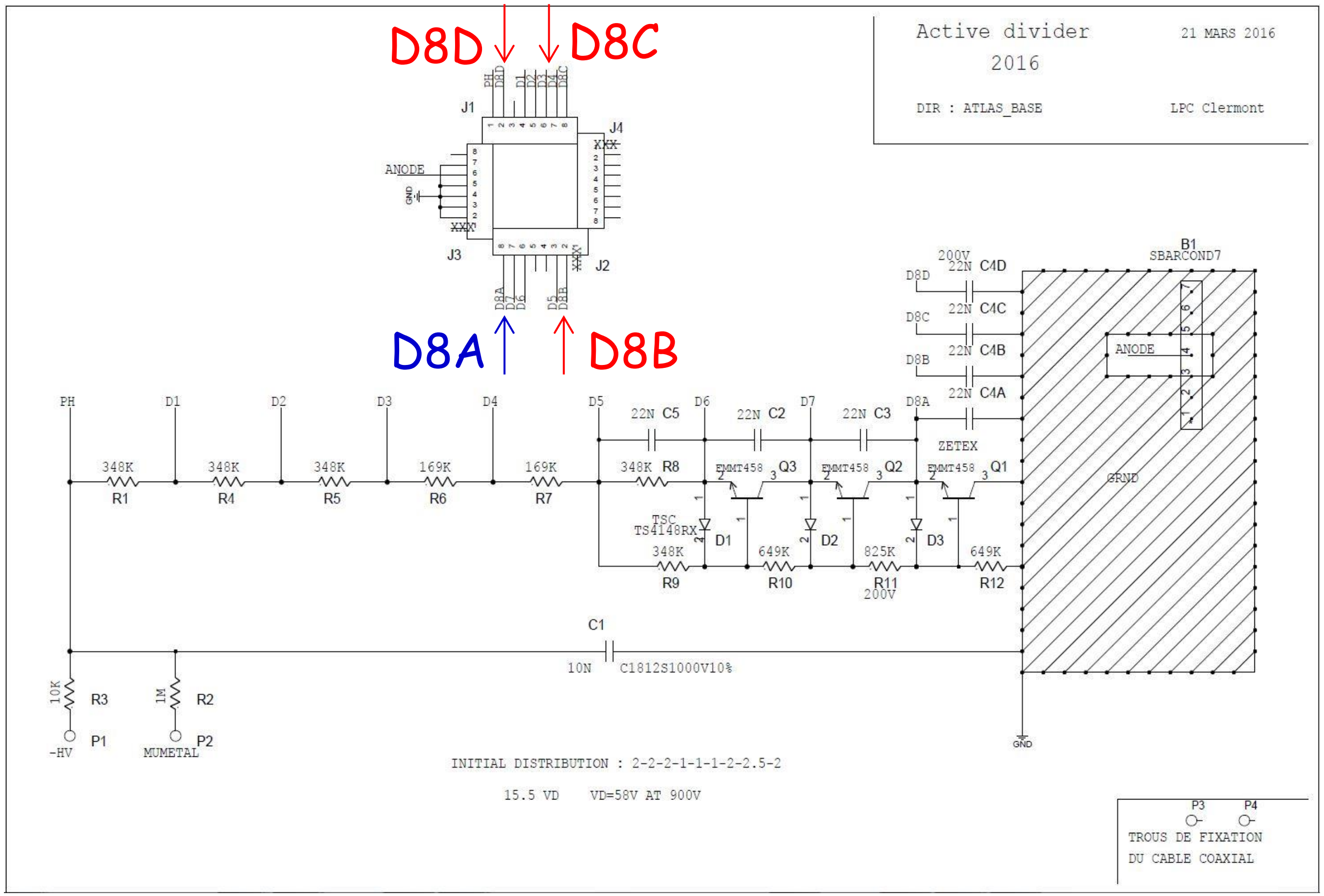
In/out Box		Average
High Gain	In	3.60±0.26
	Out	3.62±0.32
Med. Gain	In	1.32±0.06
	Out	1.32±0.08
Low Gain	In	1.16±0.08
	Out	1.17±0.07

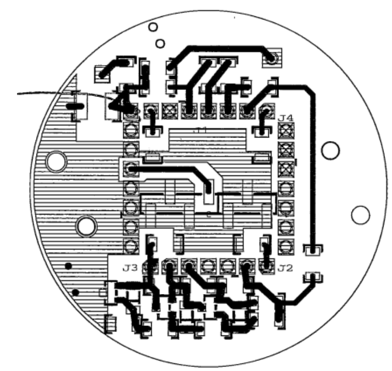
- All-in-One #13, 15 and 21.
- Results in ADC counts.

- The noise is very low : 3.6 counts for the High Gain without HV.
  By taking into account the uncertainty + this one on scale factor of 2.40±0.05
  ⇒ Noise of 8.64±0.65 fC.
- There is no difference inside and outside test box
  ⇒ very low sensitivity to the environment.
- The noise levels of other gains are small also.

- New "discovery": the last dynode (D8) is connected to 4 pins of socket, but till now in ATLAS, only 1 (D8A) is used (Decoupled/ground.) (D8 is roughly a dynamic ground/anode).

  ⇒ Modification: use of the 4 pins with 22 nF capacitors to the ground.





New active Divider with:

- single ground,
- more grounds,
- 4 D8 pins.

- Results in ADC counts.

Gain	HV	Mean ± RMS
High	Off	3.35±0.30
	On	3.47±0.51
Medium	Off	1.36±0.12
	On	1.37±0.11
Low	Off	1.17±0.03
	On	1.17±0.03

Means over cards# 13, 15,21

In/out Test Box	Gain	HV off	HV on
In	High	3.00	2.90
	Medium	1.25	1.26
	Low	1.14	1.15
Out	High	2.8	2.9
	Medium	1.28	1.26
	Low	1.15	1.15

Card# 21

PMT Block outside Drawer	High	3.00
	Medium	1.27
	Low	1.14

PMT Block alone Card# 21

- **High gain noise** in fC with HV off (On): **8.04±0.74 fC** (8.33±1.24 fC).
- **External noise: 1.76 ADC counts** < intrinsic noise of 2.85 ADC counts.
- Noise **independent** from the environment.
- Rough estimates (from the noise levels of the 3 gains) of the analog (Shaping) and digital (ADC) noise parts for HV off:

  Analog: 3.3 ADC counts (Simulation: 2 ADC counts).

  Digital : 1.1 ADC count (Simulation: 0.8 ADC count).

  $\Rightarrow$ Perhaps some margin of improvement of the analog noise.

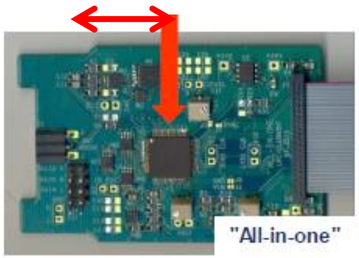
Conclusion and next actions

- The 3 main noise objectives of the FATALIC read out are reached:
  1. A High Gain electronic noise of 8.04±0.74 fC < 12 fC.
     It fits even the noise level of 8 fC: crucial for the Luminosity calibrations.
  2. An external RMS noise 1.76 ADC count < intrinsic noise 2.85 ADC counts.
  3. The noise levels of the 3 Gains are independent of the environment.

- The HV induced noise is negligible, within the uncertainties.

- Ground improvements are identified on the Dividers/All-in-One boards.

- Is it possible to improve again the electronic noise ?
  Difficult because the noise is already very low,
  but not impossible because of 3 reasons:
  - The RMS values are calculated over the whole frequency spectra, while only the high frequency noise should be considered. (5.7 to 20 MHz).
  - Cleaner modifications will be made on the new Dividers and All-in-One cards.
  - A reduction of the analog noise could come from the following change on All-in-One: to reduce the distance in between FATALIC and connector.



- And the 2 other options ?

  - Chicago 3-in-1: 15 to 20 fC, in realistic conditions (Test Beam).

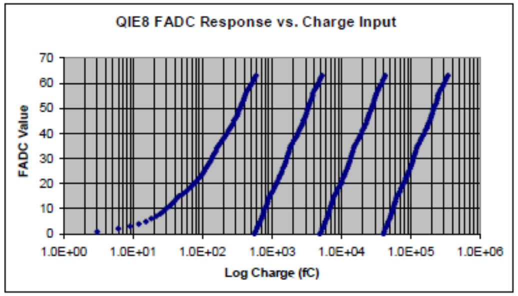
  - Argonne QIE: not very clear.

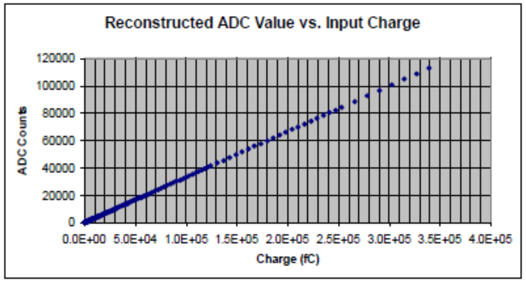
    ◊ Intrinsic noise :
    - No input current, no capacitance: ~ 2.0 fC.
    - DC current injector noise: ~ 3.3 fC.

    ◊ In realistic conditions, with PMT/Divider and other electronics: no number.

    ◊ Moreover, they must add the quantization error coming from the "linearization" of the readout (logarithmic response).

QIE quantization error = Q_{Bin} /Sqrt(12)





- Next actions
  - To produce modified active Dividers and All-in-One cards for new noise tests and the next test beam in June.
  - To perform the second phase of the noise study at LPC/CERN on a complete Drawer through the MB-DB communication (and switching LV power supply)
    - ⇒ Better statistics (12 channels).
    - ⇒ Same measurements + High frequency noise measurements.