Détecteurs CMOS

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Journée Thématique – Electronique Front-End associée aux détecteurs semi-conducteurs

Contents

1. Overview of silicon pixel detector technologies
2. Recent advancements in CMOS sensors
3. Physics motivations to use CMOS sensors
4. ALPIDE, the CMOS sensor for the ALICE ITS upgrade
5. Outlook

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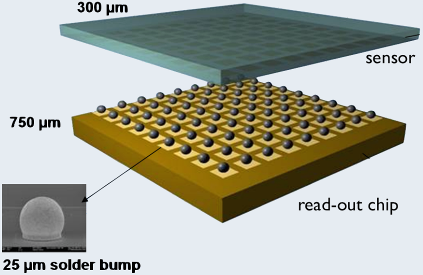
Silicon pixel detector technologies

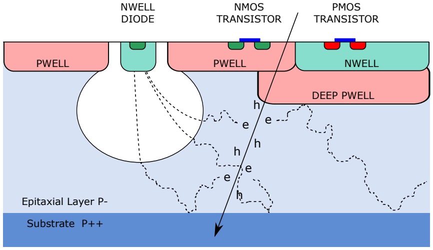
Hybrid



[current ALICE Silicon Pixel Detector]

- Two layers/chips assembly:
  - sensor chip
  - read-out chip
- They are interconnected using solder balls

CMOS (or MAPS)

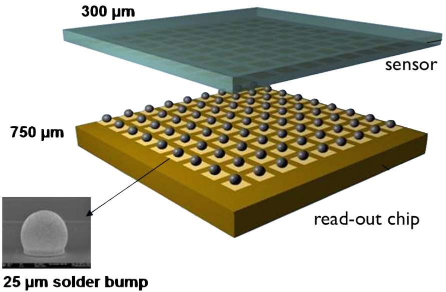


[Technology for ALICE upgrade]

- Single chip
- Read-out circuitry shares space with collection electrode

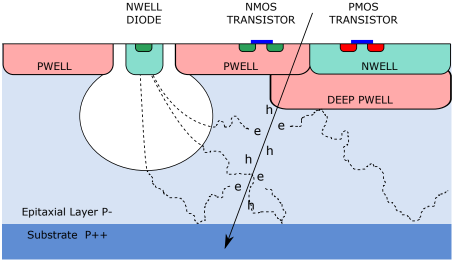
Hybrid pixels

- **Pro's**
  - Sensor and read-out may use technologies optimised for each purpose
    - Higher radiation hardness
    - Faster read-out
    - Very high signal/noise
- **Con's**
  - Larger material budget
  - Larger pitch ($\in \mathcal{O}(100\,\mu m)$)
  - ⇝ Worse performance at low momenta
  - More processing steps
  - ⇝ Higher cost



CMOS pixels

- **Pro's**
  - Minimal material
  - Small pitch ($\in \mathcal{O}(20\,\mu m)$)
  - ⇝ Better performance at low momenta
  - Single chip, no extra processing steps
  - ⇝ Lowest cost
- **Con's**
  - Lower signal/noise
  - Lower radiation tolerance
  - Lower read-out speed
  - ⇝ Not suitable for "ATLAS/CMS/ILC" *(at least as of today and for the inner layers)*



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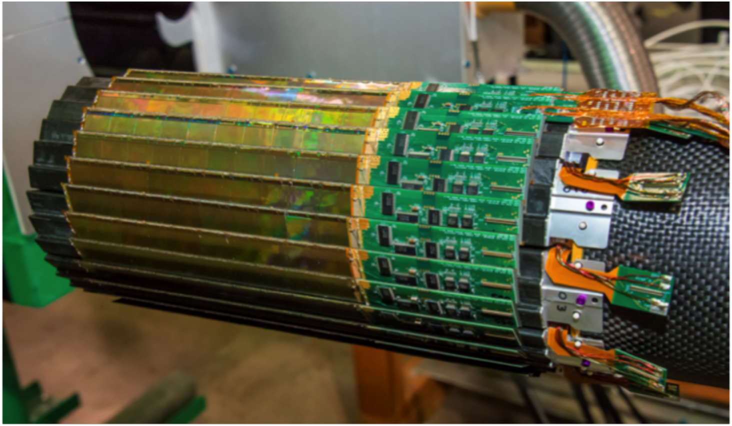
STAR's Heavy Flavor Tracker (HFT)



- STAR is the first large scale HEP application of CMOS sensors, using the ULTIMATE (IPHC Strasbourg) chip:
  - AMS 0.35 µm imaging process
  - tailored to STAR

STAR → ALICE

Increasing requirements on the sensor (selection):

STAR

- **radiation hardness:**
  >150 krad (TID),
  $>3 \times 10^{12} n_{\text{eq}}/\text{cm}^2$ (NIEL)
- **integration time:**
  <200 µs
- **power consumption:**
  $<160\,\text{mW}\,\text{cm}^{-2}$

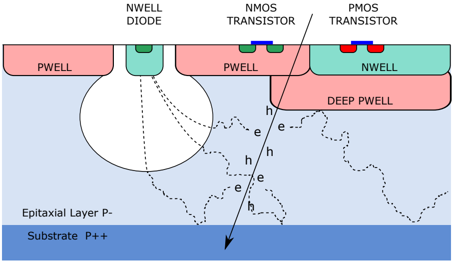
ALICE

- **radiation hardness:**
  >2.7 Mrad (TID),
  $>1.7 \times 10^{13} n_{\text{eq}}/\text{cm}^2$ (NIEL)
- **integration time:**
  <30 µs
- **power consumption:**
  $<100\,\text{mW}\,\text{cm}^{-2}$

With respect to STAR, three technology features allowed to meet the tighter requirements of ALICE:

- Inclusion of a deep p-well
- Smaller structure sizes
- Availability of high-resistivity epitaxial layers

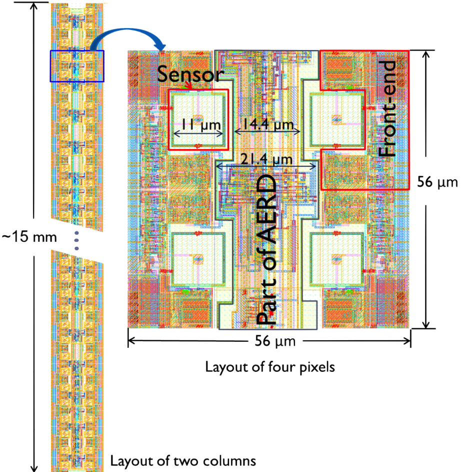
Deep p-well



- Traditionally, only one kind of transistor (PMOS or NMOS) was possible inside the active area
- In a p-type epitaxial layer, all n-wells (i. e. also those of PMOS transistors) compete for ionisation electrons
- By introducing a protective layer, the deep p-well, underneath, these can be shielded
- This allows the usage of NMOS and PMOS simultaneously, i. e. CMOS *inside the pixel matrix*

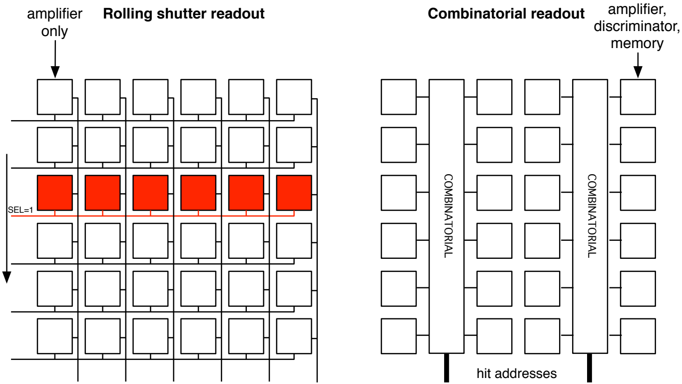
Smaller structure size

- Originally CMOS sensors were read out by 3T or 4T in-pixel circuits
- Nowadays, CMOS imaging processes allow much more, e. g. for ALPIDE:
  - 0.18 µm structure size
  - 6 metal layers
  - ⇝ around **150** transistors in a 28 µm × 28 µm pixel



[P. Yang et. al., NIM **A785** 61–85]

New read-out concepts



- New read-out concepts become possible due to high integration
- Power consumption can be reduced by:
  - not distributing a clock over the matrix
  - transferring only digital information
  - not transferring any information of not-hit pixels

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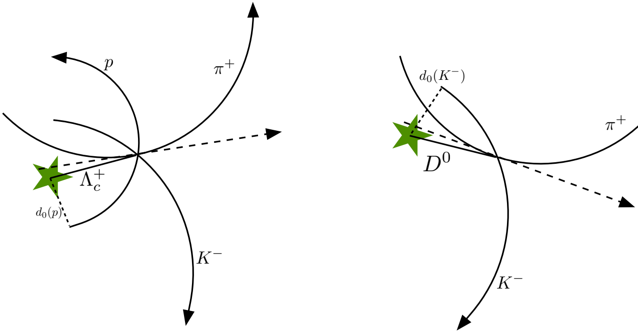
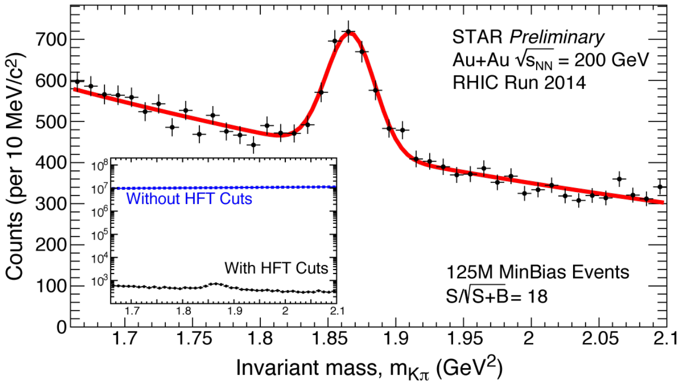
Measurements of open charm



- Decay lengths of charm particles are very short: $c\tau \in \mathcal{O}(100\,\mu\text{m})$
- Heavy-ion collisions have a huge combinatorial background: $\mathcal{O}(10\,000)$ tracks in central collisions at LHC
- Topological identification, i. e. separation of primary and secondary vertices, is key for these analyses

Measurements of open charm – D^0 at STAR



- STAR's HFT reduces background by several orders of magnitude
- 10 % of data, first physics expected for Quark Matter 2015

Impact parameter resolution

Simplified model with only two tracking planes

$$\sigma_{d_0} \approx \sigma \sqrt{\frac{r_2^2 + r_1^2}{(r_2 - r_1)^2}} \oplus \frac{r_1}{p \sin^{3/2}\theta} 13.6\,\mathrm{MeV}\sqrt{X/X_0} \quad (1)$$

with:

r_i: radii of tracking planes

σ: detector plane resolution

X/X_0: material budget

[see P. Welles, EDIT 2011 for details]

- Especially at low momenta, second term dominates

⇝ Go close, be light, have good intrinsic resolution!

Momentum resolution

Limiting factors

$$\frac{\sigma_p}{p^2} \sim \frac{\sigma}{BL^2} \tag{2}$$

with:

L: lever arm

B: magnetic field

σ: spatial resolution

[see F. Ragusa, Italo-Hellenic School of Physics 2006, for details]

- Free parameter: spatial resolution

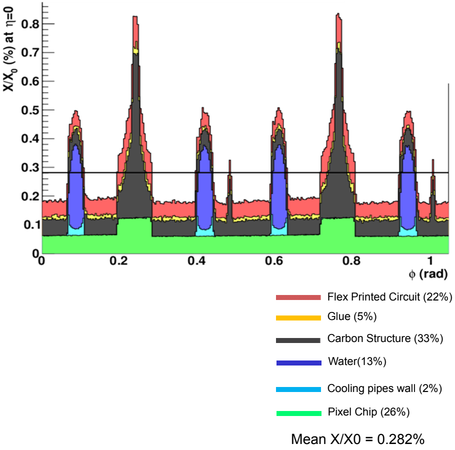
⇝ same considerations as before apply

- NB: high momentum tracks will typically be precisely tracked by outer detectors
- Key for low momentum measurements: low material

Material budget

- Reduction of material budget is key for low momentum particle measurements
- Material is composed of:
  - sensor
  - power distribution
  - cooling
  - mechanical support

⇝ Lower power consumption can reduce this significantly



[ALICE ITS upgrade Inner Barrel]

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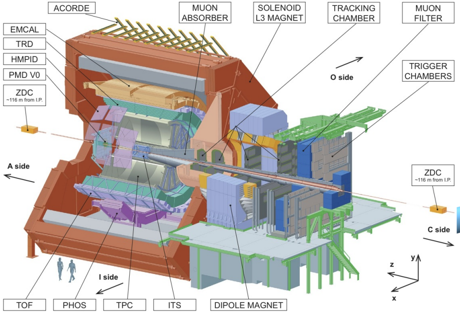
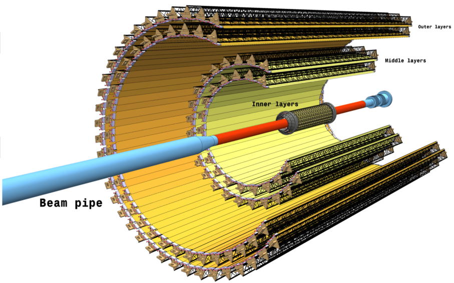
ALICE ITS upgrade

- Main goal: replacement of ALICE Inner Tracking System (ITS) during LHC long shutdown II in 2018–2019
- Design objectives:
  - **Increased spatial resolution:**
    - $\lesssim 5\,\mu\text{m}$ in longitudinal and transverse directions
  - **Closer to interaction point:**
    - move to $r = 23\,\text{mm}$
  - **Reduced material:**
    - aiming at $\lesssim 0.3\,\%\ X_0$ for innermost layers
    - additional benefit from thinner beam pipe
  - **Increased read-out speed:**
    - Record 50 kHz Pb–Pb collisions (minimum bias)

J. Phys. G **41** 087002

Detector design





- 7 layers of monolithic active pixel sensors (MAPS)
  - 3 layers in inner barrel with $X/X_0 \approx 0.3\,\%$ from $r = 23\,\mathrm{mm}$
  - 2+2 layers in outer barrel with $X/X_0 \approx 1\,\%$ to $R = 400\,\mathrm{mm}$
  - Total area of about $10\,\mathrm{m}^2$
- Coverage: $2\pi \times (|\eta| \leq 1.22)$ for $90\,\%$ most luminous region

Sensor requirements

Parameter	**Inner Barrel**	**Outer Barrel**
Sensor thickness	50 µm	50 µm
Spatial resolution	5 µm	10 µm
Dimensions	15 mm × 30 mm	15 mm × 30 mm
Power density	$300\,\mathrm{mW\,cm^{-2}}$	$100\,\mathrm{mW\,cm^{-2}}$
Time resolution	30 µs	30 µs
Detection efficiency	99 %	99 %
Fake hit rate*	10^{-5}	10^{-5}
TID radiation hardness**	2700 krad	100 krad
NIEL radiation hardness**	$1.7 \times 10^{13}\ 1\,\mathrm{MeV}\,n_{eq}/\mathrm{cm}^2$	$10^{12}\ 1\,\mathrm{MeV}\,n_{eq}/\mathrm{cm}^2$

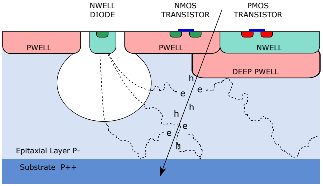
* per pixel and read-out
** including a safety factor of 10, revised numbers wrt. TDR

⇝ Perfect match for CMOS pixel sensors

- Two (pin-)compatible sensors are being developed:
  - ALPIDE (project baseline; more details here)
  - MISTRAL-O (more classical approach, optimised for outer barrel)

ALPIDE's principle of operation

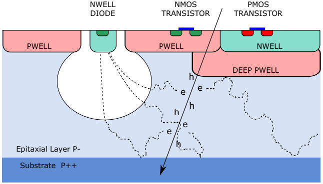
Charge creation & collection



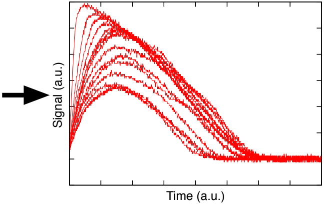
- Charge is created in the epitaxial layer

ALPIDE's principle of operation

Charge creation & collection

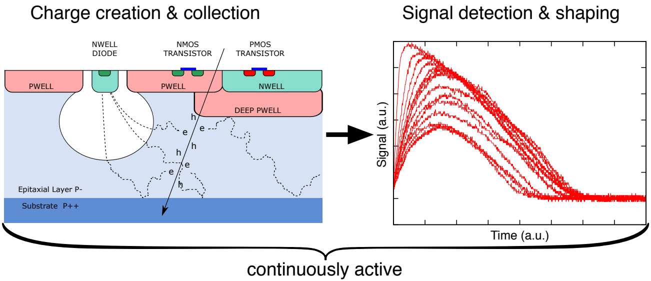


Signal detection & shaping



- Charge is created in the epitaxial layer
- Signal is shaped:
  - rise-time: $<2\,\mu s$ (defines timing resolution)
  - total pulse length: $10\,\mu s$ to $20\,\mu s$

ALPIDE's principle of operation



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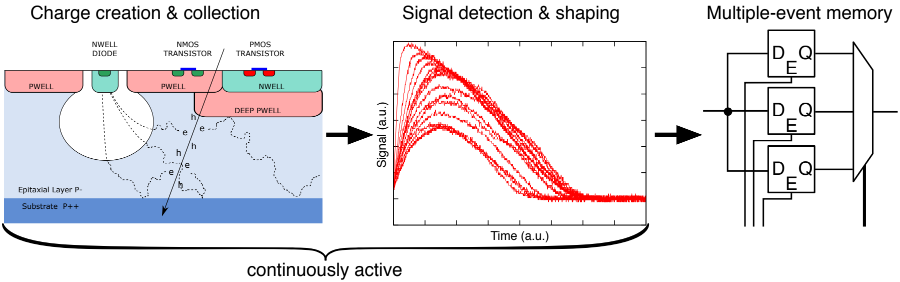

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- Signal is strobed into memory
  - either upon trigger
  - or with constant frequency (continuous/"trigger-less" operation)

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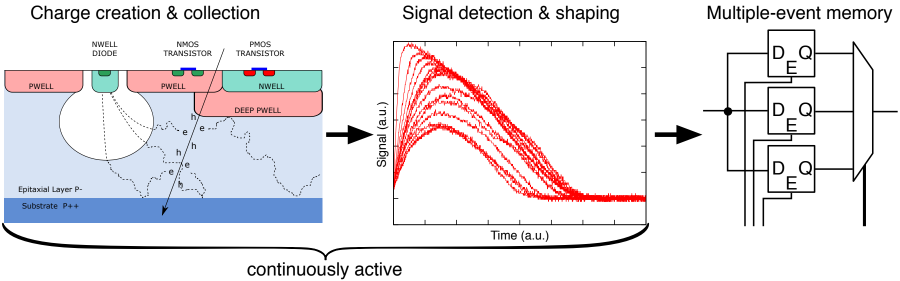

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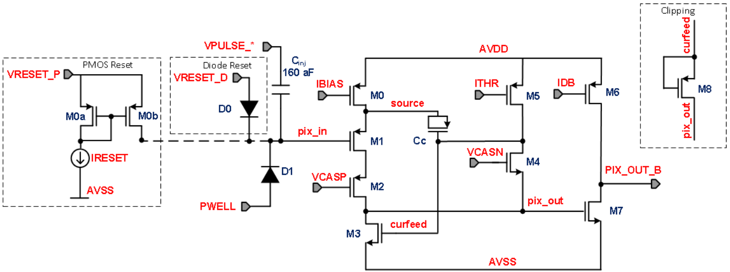
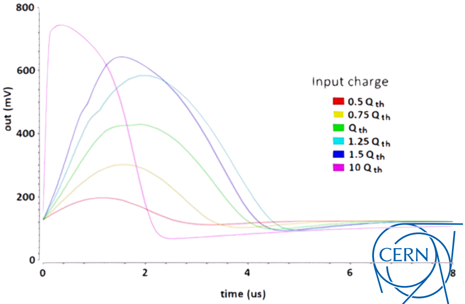
- Front-end acts as delay line
- Signal is strobed into memory
  - either upon trigger
  - or with constant frequency (continuous/"trigger-less" operation)
- Hit pixels are read out asynchronously

In-pixel front-end circuit

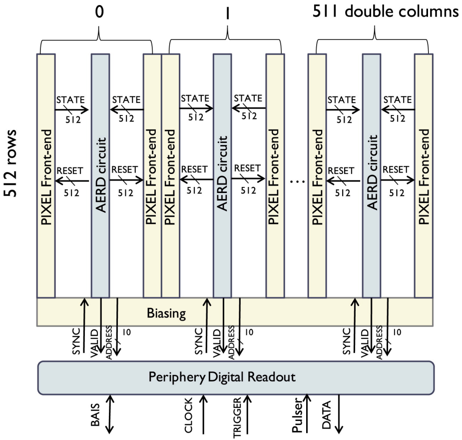


- One main current branch
- AC sensitive to negative charge input
- Non-linear dependence on input charge

⇝ Very low power consumption: $I_{\text{bias}} = 20\,\text{nA}$, $I_{\text{thr}} = 500\,\text{pA}$ (or: $\approx 40\,\text{nW}$ per pixel)



- The matrix is read out asynchronously and sparsely by use of 512 priority encoders
- High speed serial point-to-point link with up to 1.2 Gb/s (8b/10b) for data read-out
- Serial bus for configuration and triggering (≈40 MHz)



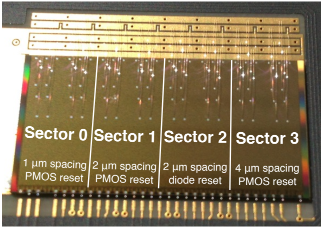
[P. Yang et. al., NIM **A785** 61–85]

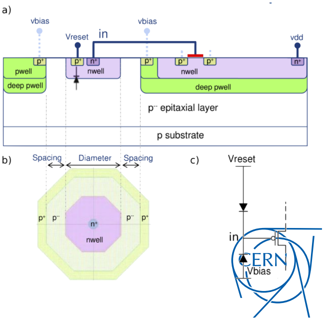
Full-scale prototype: pALPIDE-1

ALPIDE

- Pixel pitch: 28 µm × 28 µm
- Power consumption: $<40\,\mathrm{mW\,cm^{-2}}$
- Diode: 4 different flavours
- Multiple-event memory: 1 register (ALPIDE: 3)
- Read-out: 8-bit 40 MHz parallel interface (ALPIDE: high-speed serial link)

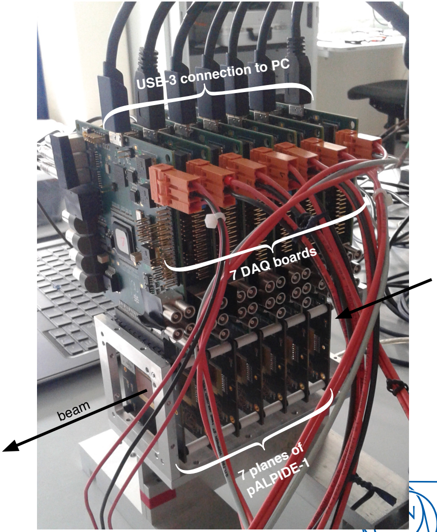
- Peaking time: 2 µs
- Pulse length: 10 µs to 20 µs
- Fake-hit rate: $\ll 10^{-5}$ per pixel and event
- Detection efficiency: $\gg 99\,\%$





pALPIDE-1: test beams

- Test beams are carried out using a telescope made entirely of pALPIDE-1
- Extensive campaign with beams at PS, SPS, PAL (Korea), BTF (Italy), DESY (Germany)
- In the following: results with 6 GeV/c π^- from CERN PS
- Tests before and after neutron irradiation



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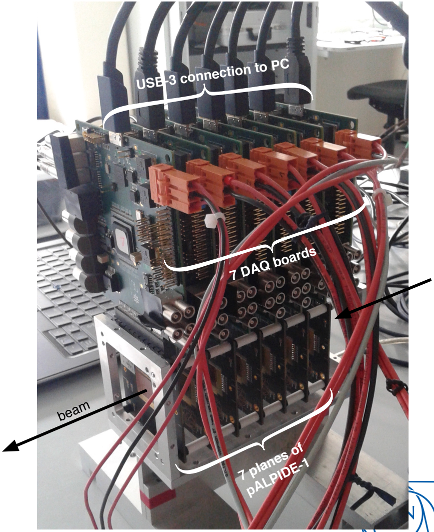
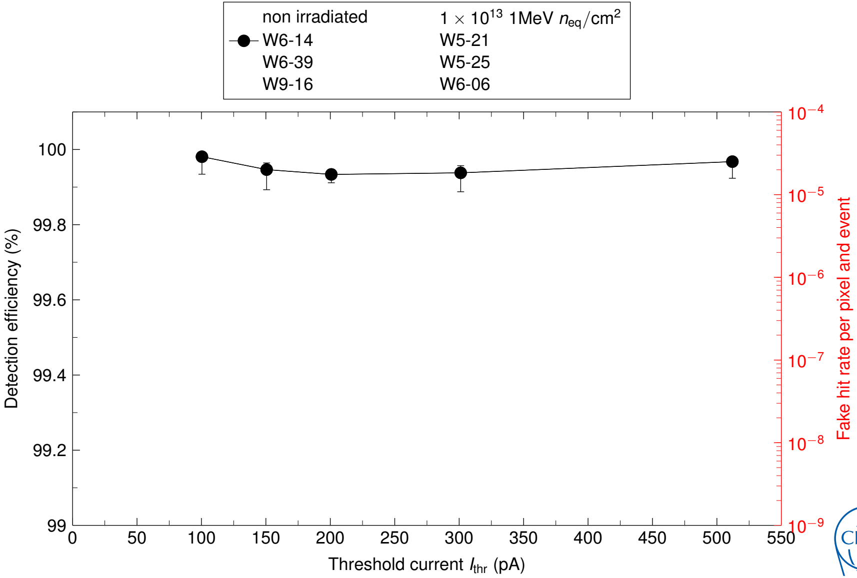
- **Many thanks to our colleagues from the host institutes for their excellent support!**



pALPIDE-1: detection efficiency



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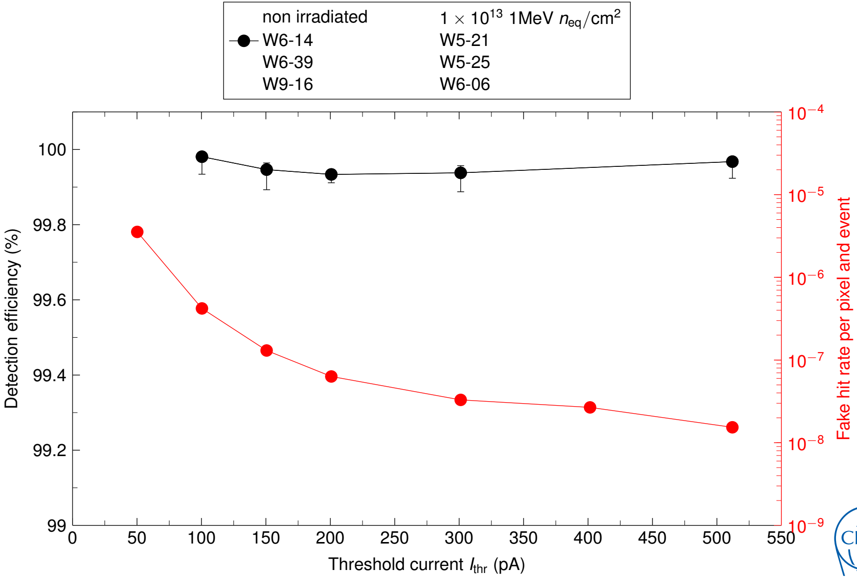

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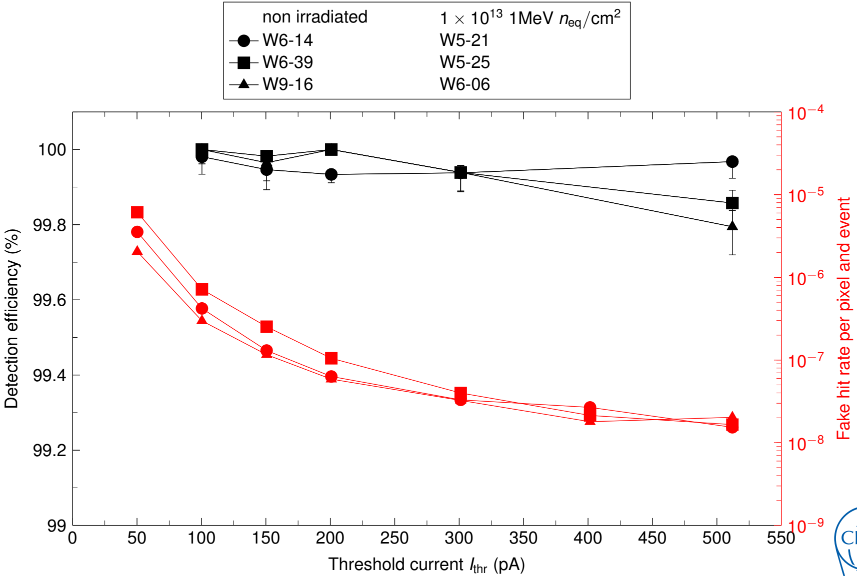
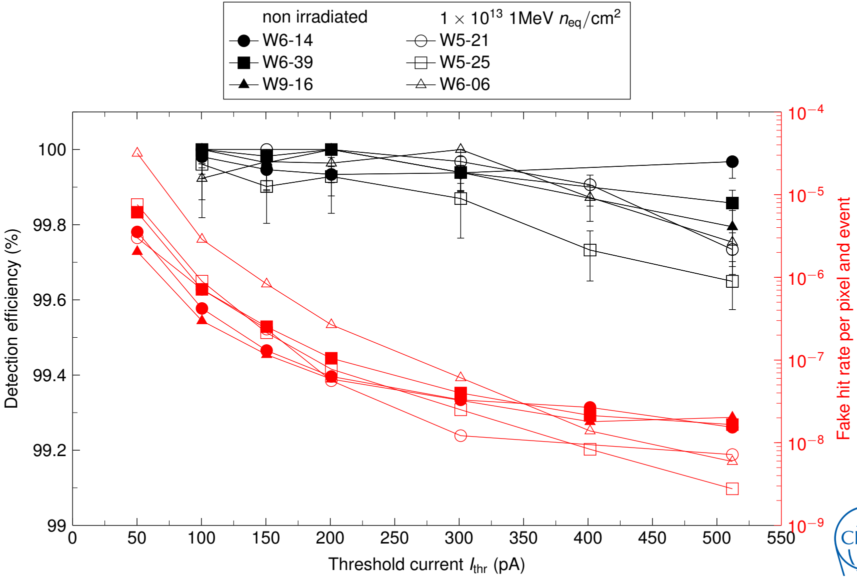
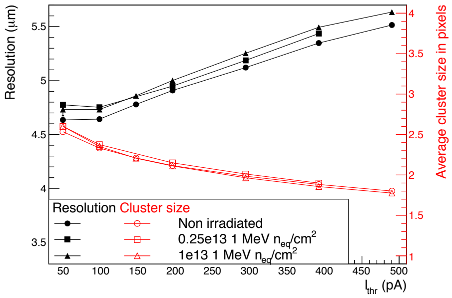


pALPIDE-1: detection efficiency



pAL PIDE-1: spatial resolution

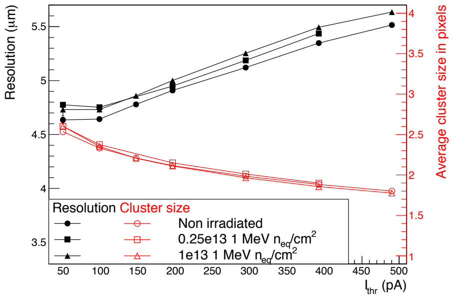
Spatial resolution



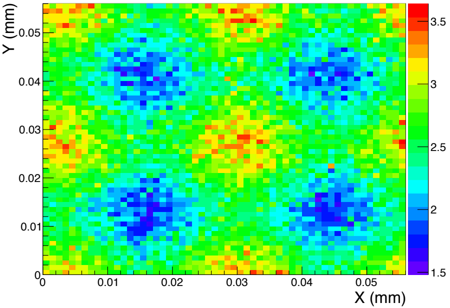
- Average cluster sizes of 1.5–3 pixels
- Spatial resolution of around 4.5 µm to 5.5 µm

pALPIDE-1: spatial resolution

Spatial resolution



Cluster size



- Average cluster sizes of 1.5–3 pixels
- Spatial resolution of around 4.5 μm to 5.5 μm

⇝ Can use telescope tracking to study properties differential in track impinging point

- Cluster size varies nicely leading to good intrinsic resolution

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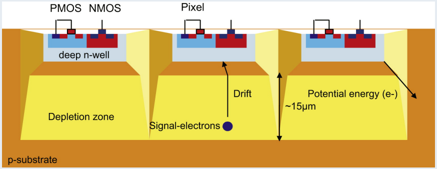
Preparing for ATLAS/CMS/ILC

- Future HEP collider experiments are more demanding, especially in terms of
  - radiation hardness ($\approx 10^{15}\ 1\,\text{MeV}\,n_{\text{eq}}/\text{cm}^2$)
  - speed (LHC: 25 ns bunch crossing)
- Several techniques are investigated to harden the detector against radiation
  - common goal: application of electric field to reach full depletion
- Besides the inner-most detection layers, there are other fields of applications:
  - Particle densities (and radiation levels) at layers further out is lower
  - Currently these areas are equipped with strip detectors
  - CMOS becomes an attractive alternative

Ways to increase radiation tolerance

- Essentially boils down to apply high electrical fields

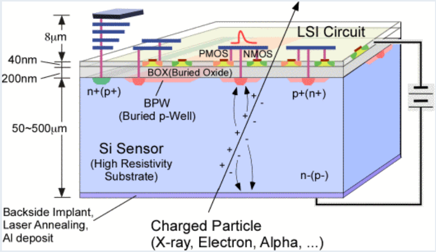
High Voltage CMOS



[I. Perić et. al., NIM **A765** 172–176]

- Deep n-well shields electronics
- This well also collects the charge
- Apply high voltage

Silicon on Isolator



[http://rd.kek.jp/project/soi/research.html]

- Oxide layer isolates electronics
- Apply high voltage

⇝ R&D also in the field of high-resistivity MAPS (like ALPIDE) to reach full depletion ongoing. . .

Summary and Outlook

Summary

- CMOS sensors are becoming attractive for certain HEP applications, due to their
  - minimal material budget
  - high granularity
  - moderate radiation tolerance
  - moderate speed
  - very low power consumption
  - low cost
- With STAR's HFT, CMOS sensors enter large scale HEP experiments

Outlook

- ALICE will replace its complete inner tracker with some $10\,m^2$ CMOS in 2018–2019
- Many R&D projects are on their way to make CMOS radiation hard enough for "ALTAS/CMS/ILC-type" applications