OMEGAPIX2

Journées VLSI – FPGA – PCB de l'IN2P3
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Outline

- The ATLAS experiment
- The OMEGAPIX2 integrated circuit
  - The 3D process
  - The analog tier
  - The digital tier
- Circular memory measurements
- Analog performances
- Future work
  - Irradiation, bump bonding
  - New OMEGAPIX chip in 65 nm
- Conclusion

The ATLAS inner tracker @ HL-LHC

44m
25m
Tile calorimeters
LAr hadronic end-cap and forward calorimeters
Pixel detector
LAr electromagnetic calorimeters
Toroid magnets
Muon chambers
Solenoid magnet
Transition radiation tracker
Semiconductor tracker

Pixel Detector

Operated from 2009 to 2012

- Installation from 2013 to 2014
- Operation from 2015 to 2020

Second upgrade: High-Luminosity LHC

- 14 TeV centre-of-mass energy
- L = 10^{35} $cm^{-2}s^{-1}$ => need new FE design
- Pixel damage due to neutrons and pions, exposure up to 10^{16} neq/cm^2 (1 Grad) => need new rad-hard technology
- New technology
  - 3D 130 nm techno
  - 65 nm techno
  - …

Pixel detector's first upgrade

- service upgrade and repairs
- Resolution: 10 µm (rϕ) 115 µm (z) with FE-I3 (50x400 µm²)

Insertable b-layer

- Compensate inefficiency, radiation damage and losses of pixels/modules
- Improve precision measurement with an additional point closer to the interaction point, improve vertexing, tracking and b-tagging performance
- FE-I4 (50x250 µm²), plannar sensor and 3D sensor
- Resolution < 10 µm (rϕ) 80 µm (z)

The OMEGAPIX2 chip

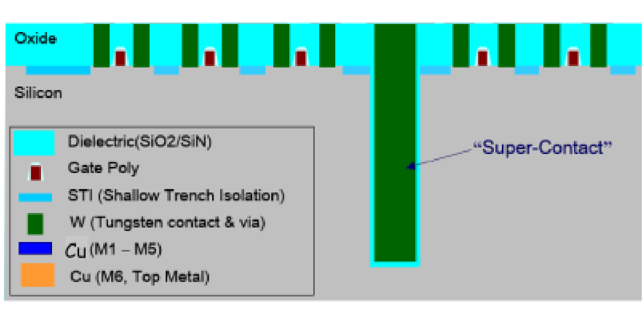
- 3D OMEGAPIX2 chip received in January 2014
  - Submitted in October 2011
- Goals
  - Study and validate the Global Foundries techno and the 3D process of Tezzaron
    - Tier isolation, GF techno characterization (T typical, low Vt), yield, electrical and mechanical connections
  - Explore new solutions for a pixel readout chip for the ATLAS upgrade phase II
    - Low power, small pitch (35x200 µm), low signal
    - High luminosity: keep all data before L1 trigger by storing in a circular memory the whole history of the pixel activity during a L1 latency
    - Very hard radiation level
- Future work
  - Sensor bump bonded
  - Irradiation tests
- A new OMEGAPIX chip in 65 nm techno as an alternative to the 3D chip
  - Same pixel form factor: 35x200 µm
  - TSMC 65 nm techno
  - Common PDK provided by CERN

The 3D process from Tezzaron

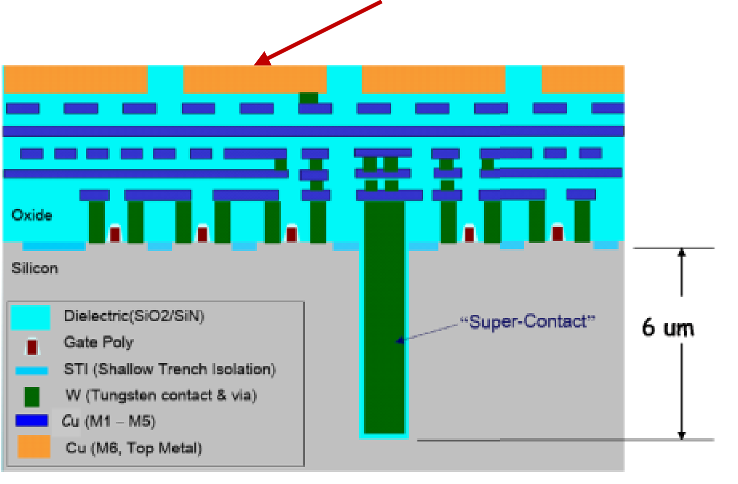
- (1) Via first approach. Tungsten through silicon vias (TSV) are fabricated as a part of the foundry process
  - Fabricate transistors (FEOL)
  - Form via (6 micron deep)
  - Passivate vias
  - Fill vias and connect to transistors at same time

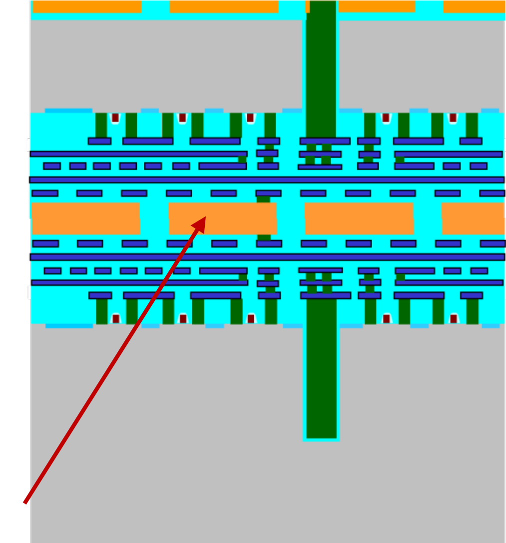
- (2) Complete BEOL processing
  - Add 6 metal layers
  - 6th metal layer is used as a bond interface for Cu-Cu thermo compression

- (3) Stack a second wafer
  - Alignment better than 1 micron
  - Thermo compression bond is formed between wafers
- (4) Thin the top wafer down to 12 microns to expose TSVs
- (5) Metal pads added for wire or bump bonding



Pads for bond interface





The bond interface is critical for good yield
- Makes electrical and mechanical connections from one wafer to the other wafer
- Bond interface must be strong enough to withstand subsequent thinning process

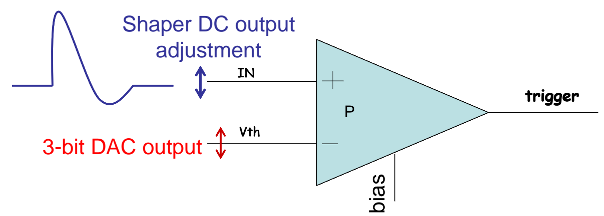
Analog tier (1)

Ωmega

- Targets
  - Dynamic range: 0 to 40 000 electrons
  - Low threshold (~1000 electrons), low noise (<100 electrons)
  - Power dissipation : ~6 µA
  - Leakage current compensation: up to 100 nA
  - Time over Threshold (ToT) capability
- Preamplifier
  - Regulated followed cascode NMOS common source
  - Leakage current compensation based on an OTA circuit in feedback: 0 to 100 nA
  - Constant current in feedback to discharge the gain capacitance: ToT purpose
  - Low noise: < 200 e- with Cd
  - Detector capacitance: 200 – 300 fF
- Second gain stage
  - Regulated followed cascode PMOS common source
  - Capacitive coupling: parallel noise independent
  - Gain = ~1
  - Feedback structure based on an OTA to tune the DC level at the shaper output: 5-bit DAC
- Comparator
  - Classical structure
  - 3-bit DAC to fix the threshold
- Slow control DFlipFlops
  - Injection capacitance, 8-bit DAC, External Trigger
  - Triple voting, interleaved layout
- Layout
  - 96 rows, 24 columns
  - Pitch = 35x200 µm
  - Macropixel = 2 pixels with staggered analog inputs: bump bond pitch = 70 µm
  - Match with the last sensor submission

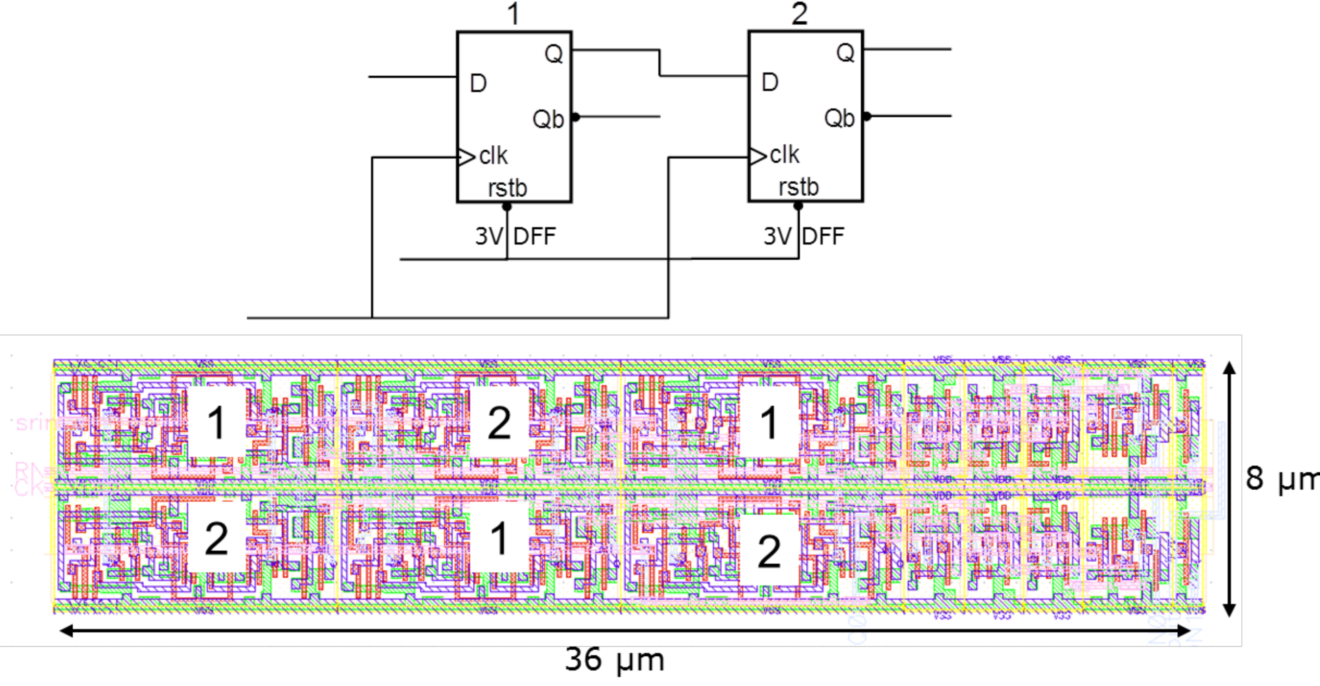
Constant current feedback
5-bit DAC
Input bounded to the sensor pixel
Signal comes from Through Silicon Via (TSV)
Preamplifier
Shaper
Comparator
Trigger goes up to the second digital tier
Leakage Current Compensation
3-bit DAC

Pixel	35x200 µm² in omegapix2
Pixel Capacitance	200 – 300 fF
Threshold	1000 electrons (0.16 fC)
Rms noise	< 200 electrons
Charge measurement	ToT (3 bits,)
Leakage current max.	100 nA
Power dissipation	6 µW/pixel



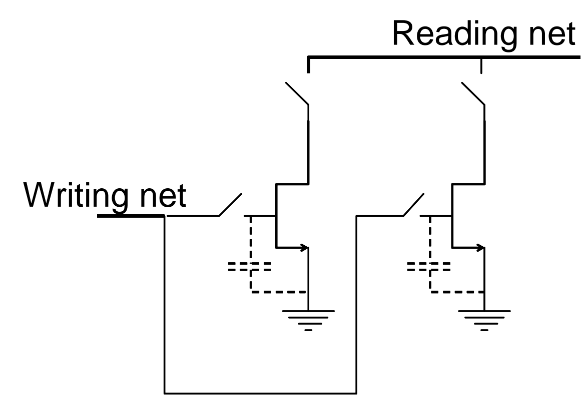
Analog tier (2)

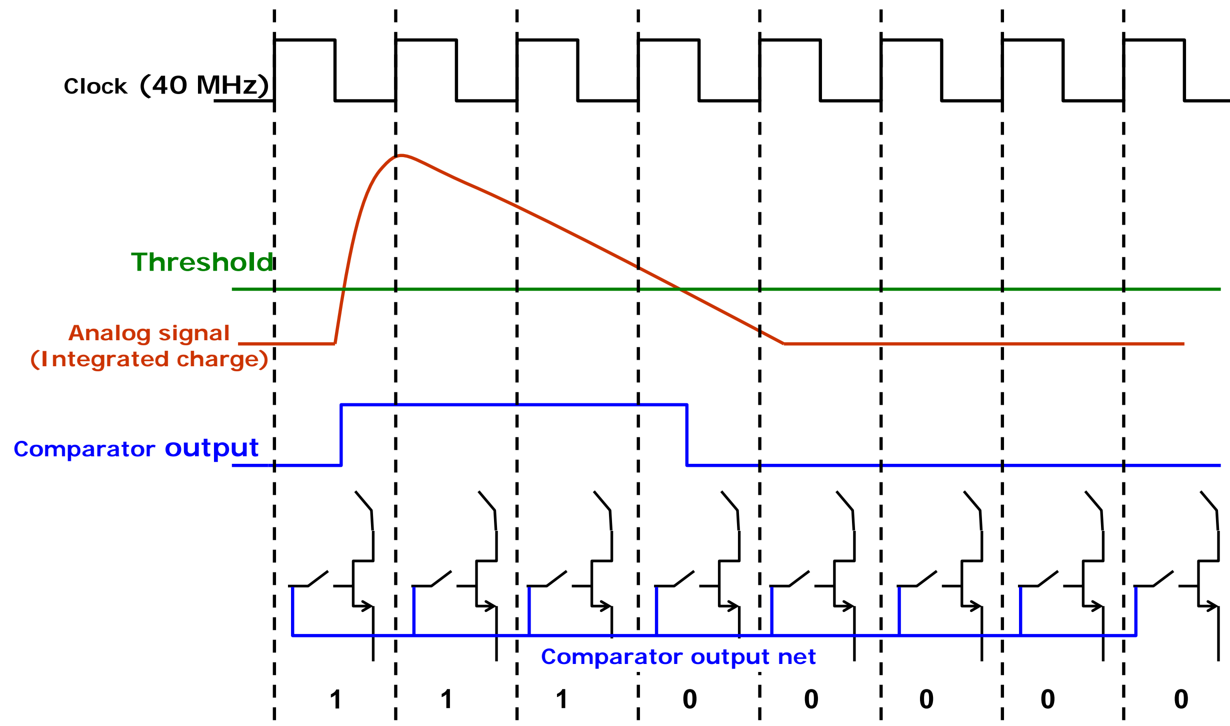
- Slow control shift register
  - Injection capacitance
  - 5-bit shaper DAC and 3-bit local DAC
  - 4-bit preamplifier feedback current
- Rad_hard shift register
  - SEU immune: triple voting and interleaved layout



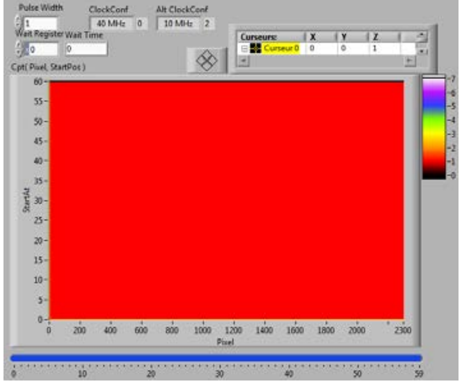
Digital tier

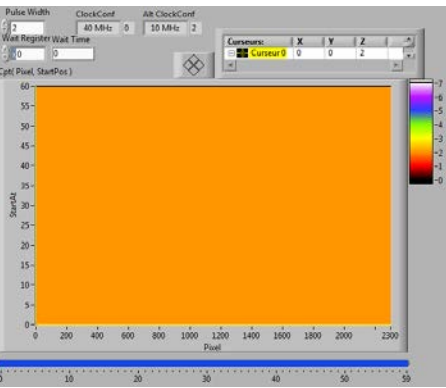
- Circular memory
  - 60-deep circular memory: keep an image of the pixel activity for 3 µs (BC period = 50 ns) or 1,5 µs (BC period = 25 ns)
  - Memorizing cell performed by the parasitic Cgs capacitance of NMOS
  - 6 different types of memory cell: 5/1 typ, 15/1 typ, 5/1 3P3, 15/1 low Vt, 5/1 typ + capa
  - Output data after L1: 3-bit ToT in gray

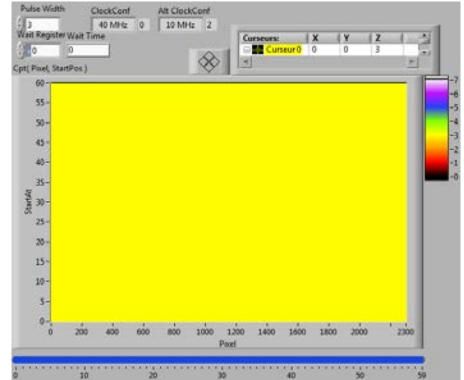


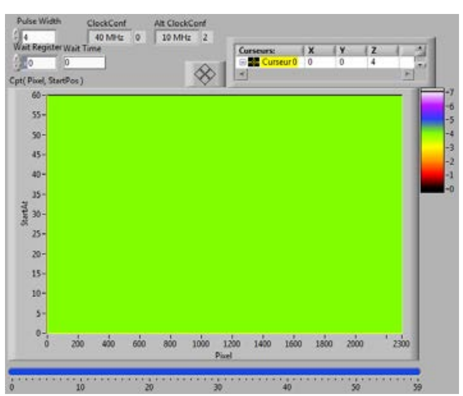


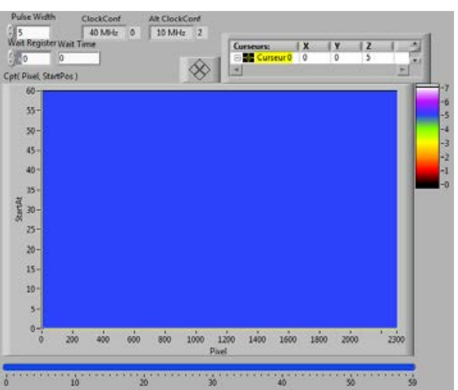
Digital measurements (1)

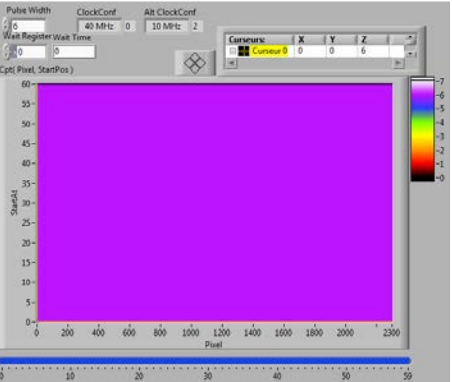


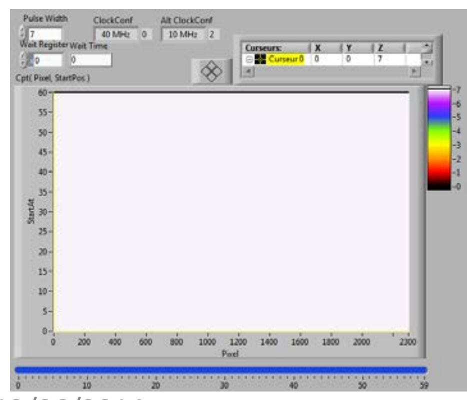


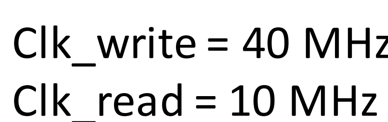






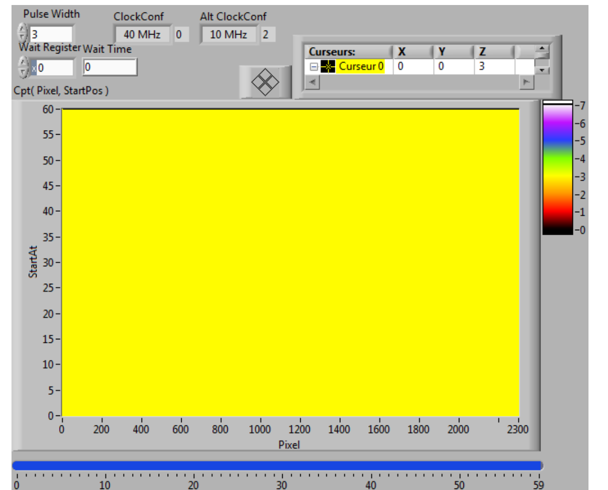




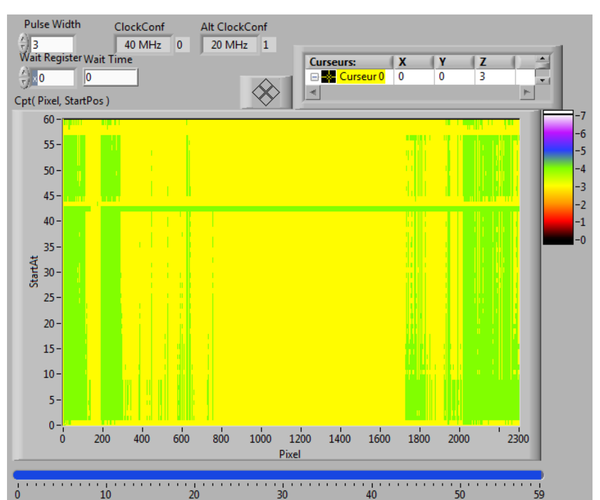


Firmware and software designed by O. Le Dortz (LPNHE Paris)
Measurements done by M. Cohen-Solal and C. Sylvia (LAL Orsay)

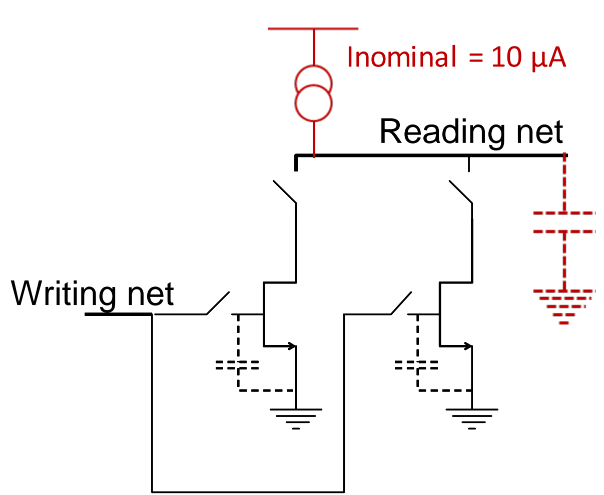
Digital measurements (2)

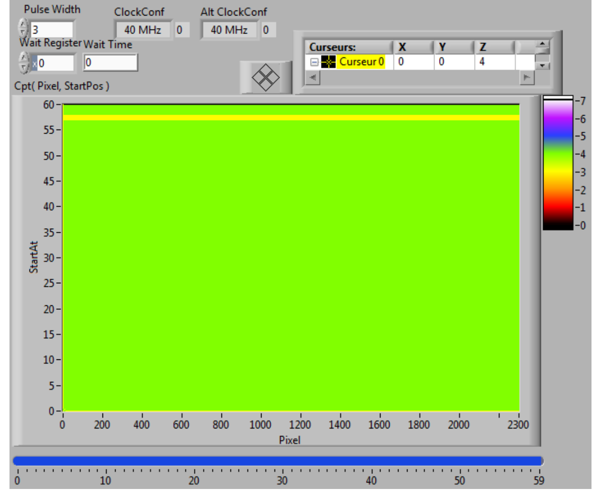


clk_write = 40 MHz, clk_read = 10 MHz



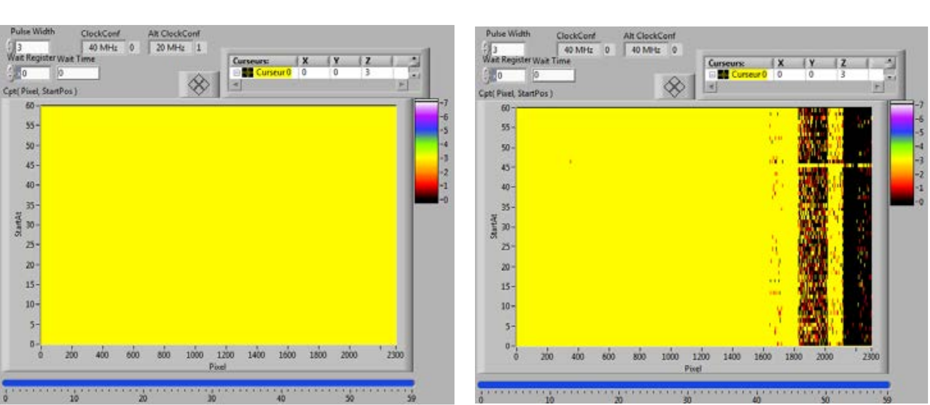
clk_write = 40 MHz, clk_read = 20 MHz





clk_write = 40 MHz, clk_read = 40 MHz

15/1 typ 5/1 + capa 15/1 lvt 5/1 lvt 3p3 typ 5/1 typ



R bias memdyn = 22k => ibias x3,5 = ~ 35 µA

Digital measurements (3)

	BC0	BC1	BC2	BC3
Data in circular memory	0	1	0	0

Digital measurements (4)

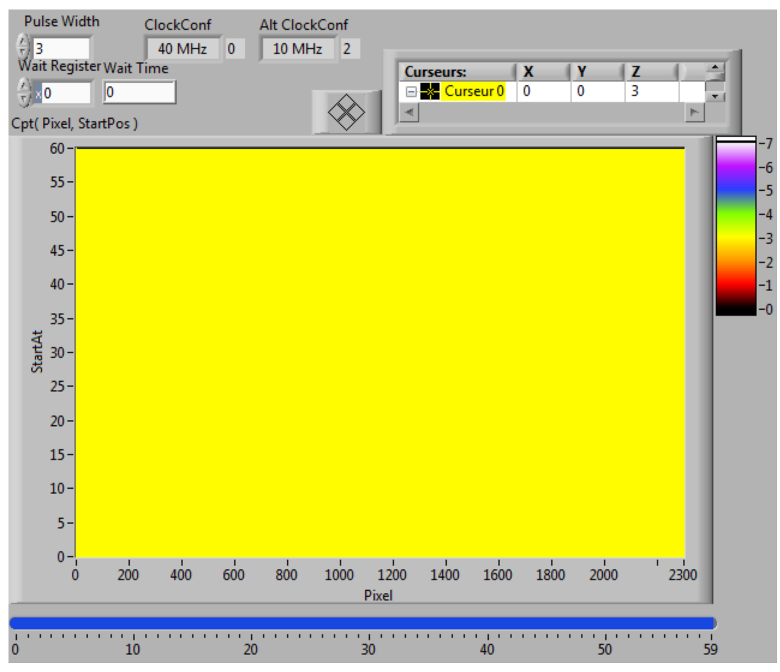
15/1 typ   5/1 + capa   15/1 lvt   5/1 lvt   3p3 typ   5/1 typ

Sans R bias memdyn

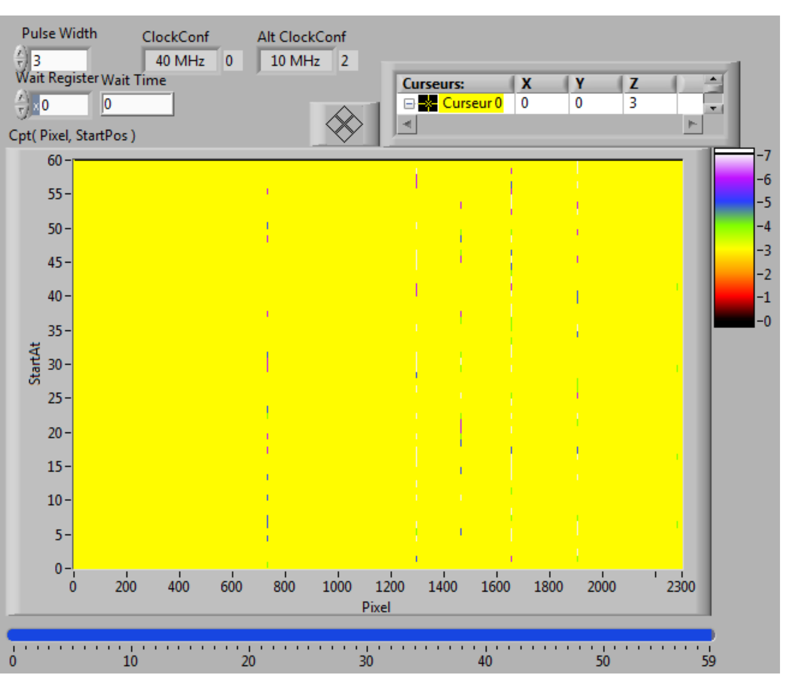
Avec R bias memdyn

5/1 typ
5/1 typ
5/1 typ
15/1 typ
15/1 typ
15/1 typ
Clk_write = 10 MHz
Ib_memdyn nominal
5/1 lvt
Clk_write = 10 MHz
Ib_memdyn nominal
Inj. Via Analog tier
5/1 lvt
5/1 lvt
Clk_write = 40 MHz
Ib_memdyn x3,5
15/1 lvt
15/1 lvt
15/1 lvt
5/1 + capa
5/1 + capa
5/1 + capa
3p3 typ
3p3 typ
3p3 typ
memorization time (ms)
Occurences

Digital measurements (5)



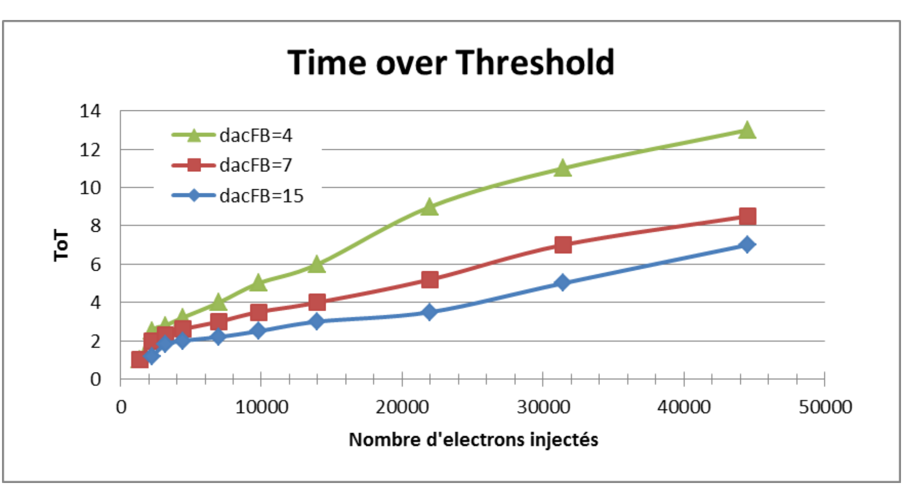
Injection via digital tier

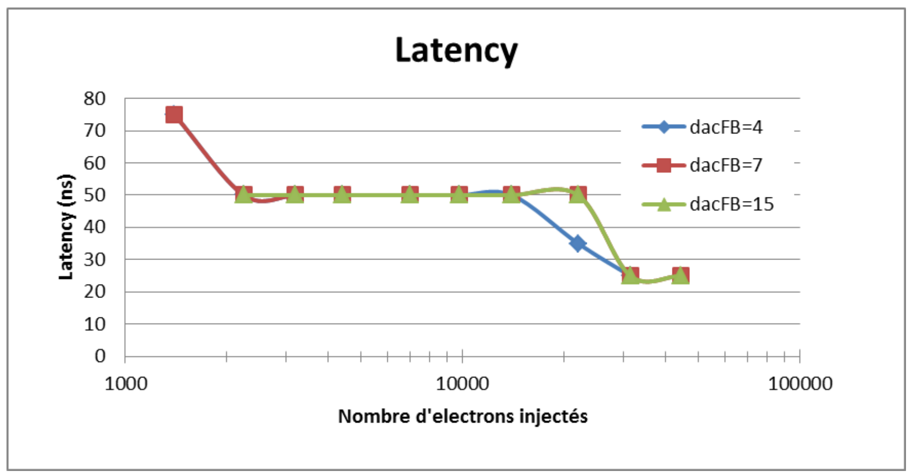


Injection vi analog tier

Analog performances (1)

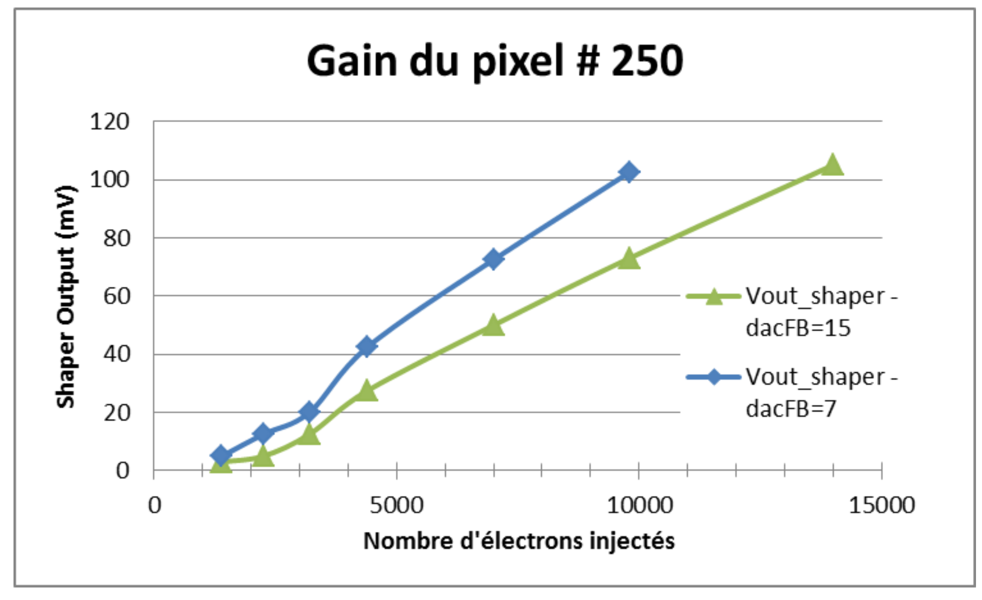
- Premières mesures analogiques
  - Réalisée sur une seule voie
  - Time over Threshold
    - Réglable par dacFB<0:3>
  - Latence
    - Plus grande que prévue, peut-être due à la façon d'injecter
    - Deuxième coude problématique
- Difficultés
  - Capa d'injection mal connue car faite avec un transistor et non une vraie capa (estimée à 15 fF)
  - Beaucoup de dispersion du gain est attendue





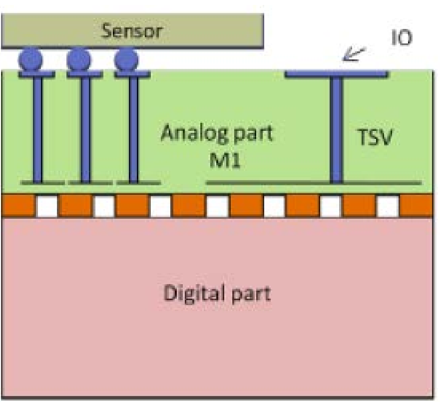
Analog performances (2)

- Gain: ~ 50 – 70 mV/fC
  - Mesuré par le trigger (S curve) et non par probe
  - Plus faible que prévu (130 mV/fC)
    - Mesure faite sur une voie
    - Les Dacs doivent être mieux caractérisés
    - Valeurs des capas (en fait des transistors) peut-être mal modélisés
- Enveloppe du bruit
  - ~ 10 mV => ~ 100 électrons rms



Bump bonding

- Sensor
  - CIS slimedge, VTT slimedge and edgeless
  - 35x200 µm, compatible with OMEGAPIX2 chip
- Interconnection with the CEA LETI
  - Pitch 70 µm 35 µm
  - Post-process, die to wafer
  - I/Os



    - Sensor side: wire bonding as described in figure

    - Back side: via last process from LETI to reach pads from digital tier (all the I/O pads of OMEGAPIX2 pass through the 2 tiers)

Irradiation

- New dedicated boards designed @ LPNHE (O. Le Dortz)
  - Monitoring board based on the Kit Altera Nios II Stratix II
  - Custom irradiated board

Salle d'irradiation

Extérieur

Faisceau

Zone « tiède »

ZONE CONTROLEE ACCES REGLEMENTE

ASIC

Logique I/O

Carte Irradiée à fabriquer

Câble à définir qques mètres

~30 I/O + Alim

Carte Pilote à définir

FPGA+Interface

ETHERNET ~10 m

PC de monitoring

Conclusion

- Circular memory works well
  - Writing operation at 40 MHz
  - Memorization time is very good
  - But limitation to read at 40 MHz
    - Increase bias current leads to decrease the memorization time => trade-off
- Analog performances
  - Time over Threshold OK
  - Slightly too long latency
    - Injection has to be checked
    - Preamp and shaper bias can be increased
  - Gain smaller than expected: to be understood
  - Noise higher than expected: to be understood
- Irradiation
  - Board, firmware : on going
- Bump bond: project on going with the CEA-LETI
- Future
  - 3D or 65 nm ?

Backup

New OMEGAPIX in 65 nm (1)

- Due to very long fabrication delay of the 3D chips, we plan to submit a new 2D prototype in 65 nm

out_pa Tue Jun 25 10:03:29 2013

out_pa
out_sh
Vth
out_discri

time (us)

rmsNoise:Vmax_pa:Vmax_sh:VDC(out_pa):VDC(out_sh):Threshold:SNratio:ENC:Qinj

Vmax_pa
Vmax_sh

N (k)

Q (electrons)	1000	10 000	30 000
Preamp gain	11 mV	110 mV	300 mV
Shaper gain	16 mV	190 mV	450 mV
ToT (ns)	60	350	770
ToT (BC)	3	14	31

New OMEGAPIX in 65 nm (2)

- Typical Low Power transistor
  - Cf = 15 fF => 66 mV/fC
  - With Cd = 300 fF, ENC from 80 to 120 electrons when leakage current varies from 0 to 100 nA
  - Preamplifier open loop gain = 90 dB
  - Global power consumption: vdd = 1,2 V and i + 8 uA => 9,6 uW
  - Dynamic range: 450 mV max.
- Local 5-bit DAC
  - Low power => relatively high resistor value in each pixel

	Vdd (V)	DC gain (dB_{20})	GBWP	Consomption
Preampli	1.2	90	250M	3.4uA
Shaper	1.2	77	90M	2.5uA
Discri	1.2	NA	NA	2.2uA