



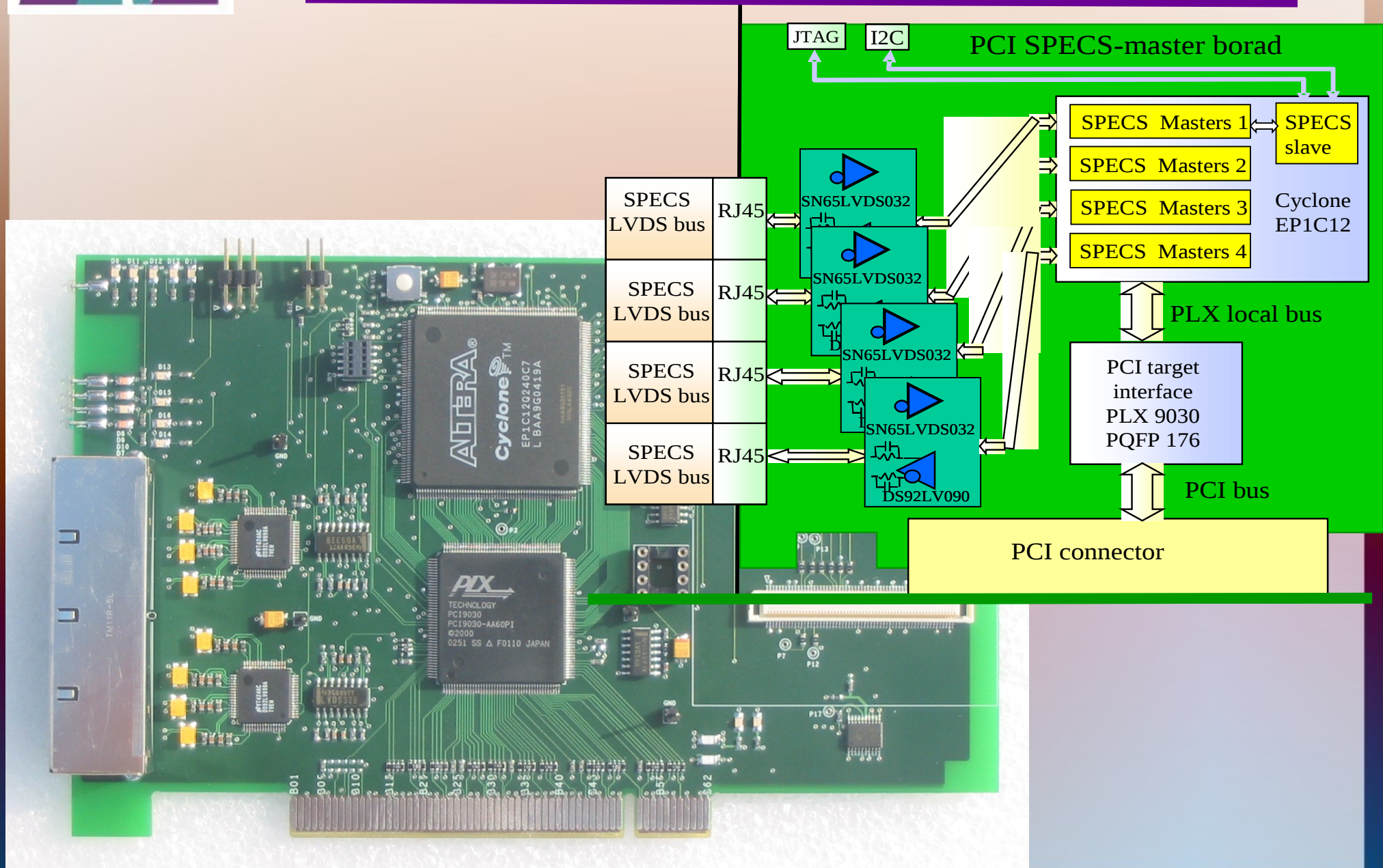
SPECS -Master_PCIE_xTCA

- L'histoire ancienne
- SPECS_Master_V2
- Les outils de développement

Jean-Pierre Cachemiche, Daniel Charlet, Jean-Pierre Marolleau,
Claude Pailler, Monique Taurignat, Jean-Luc Socha

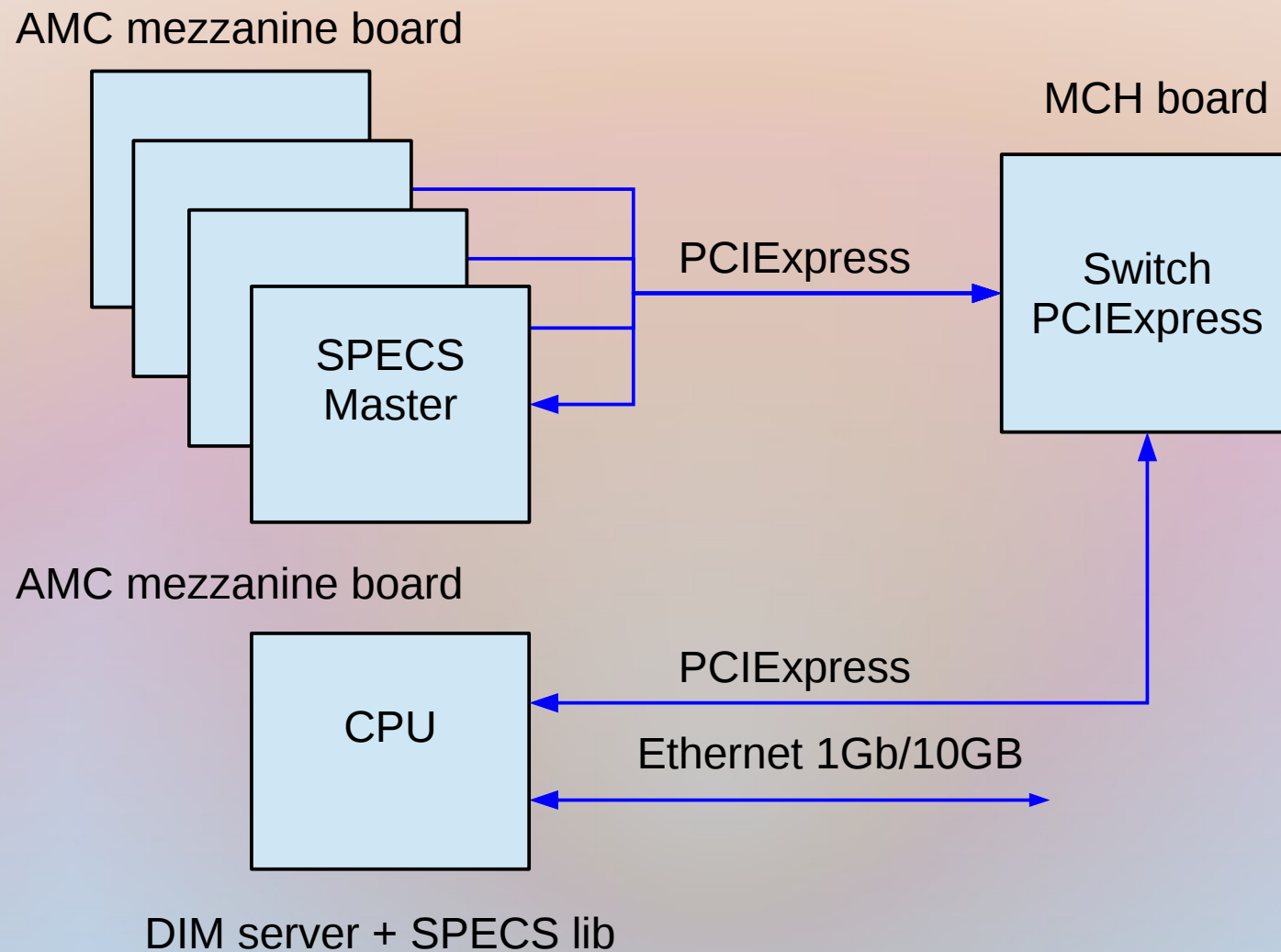


SPECS master version 1



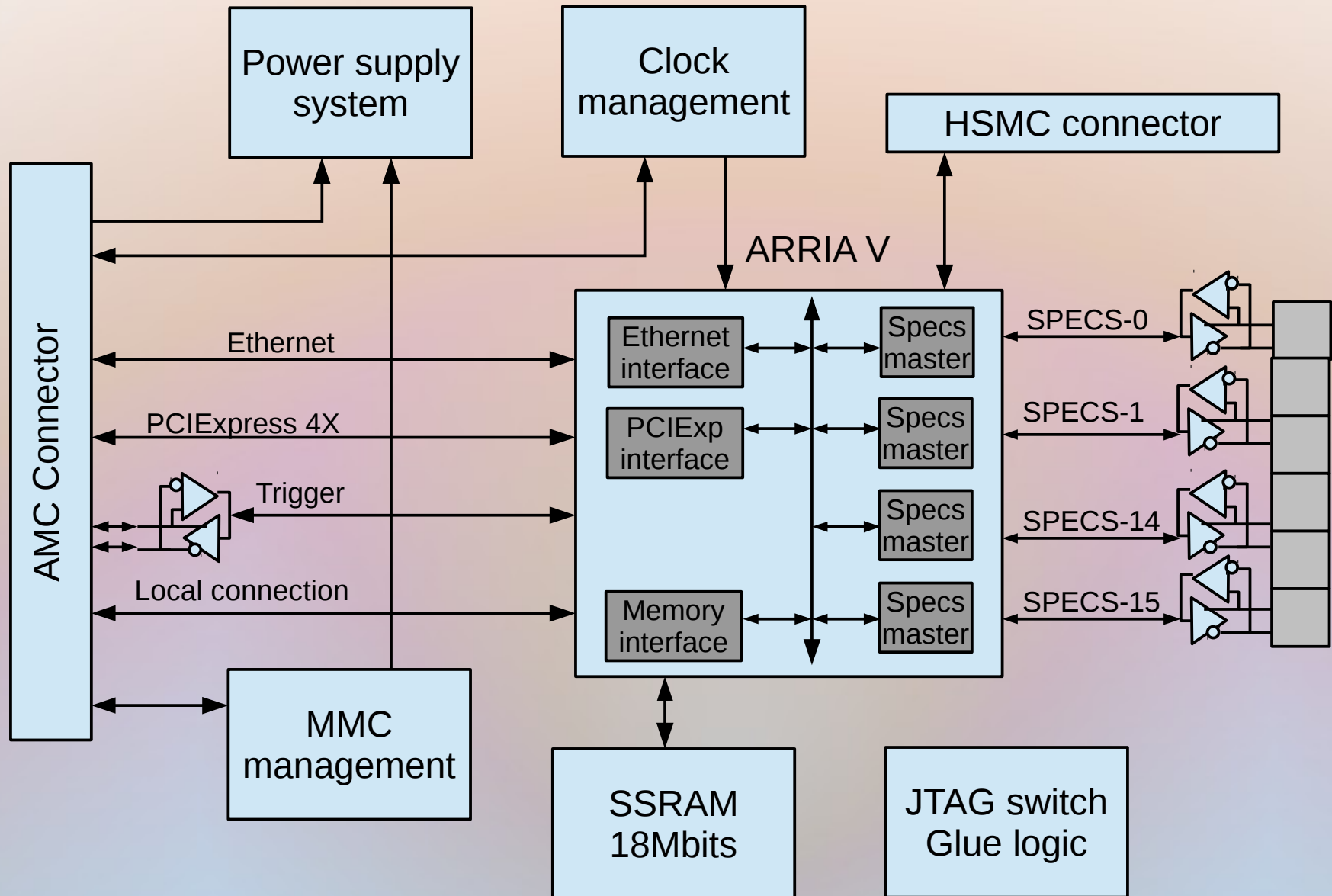


SPECS master version 2





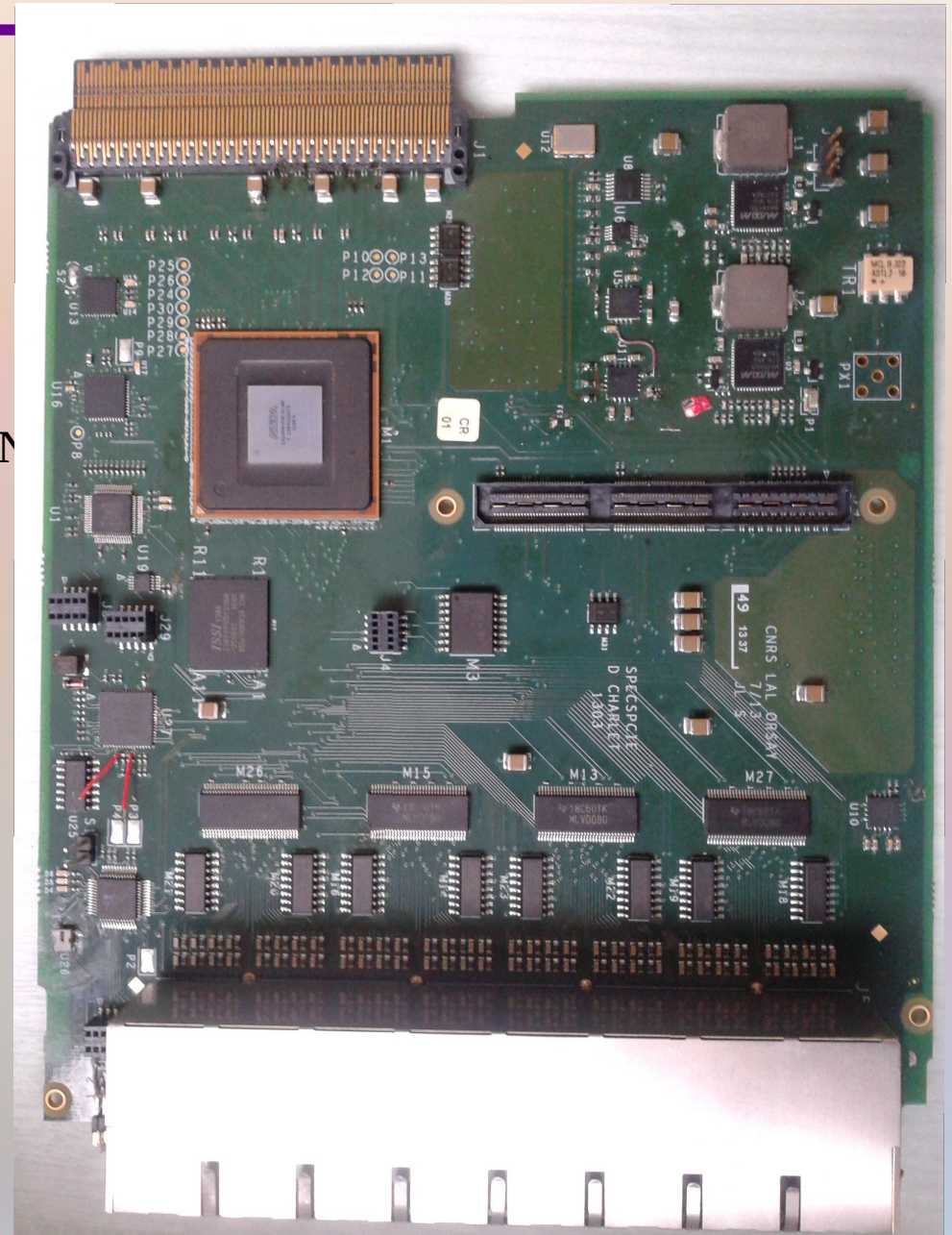
AMC SPECS master V2





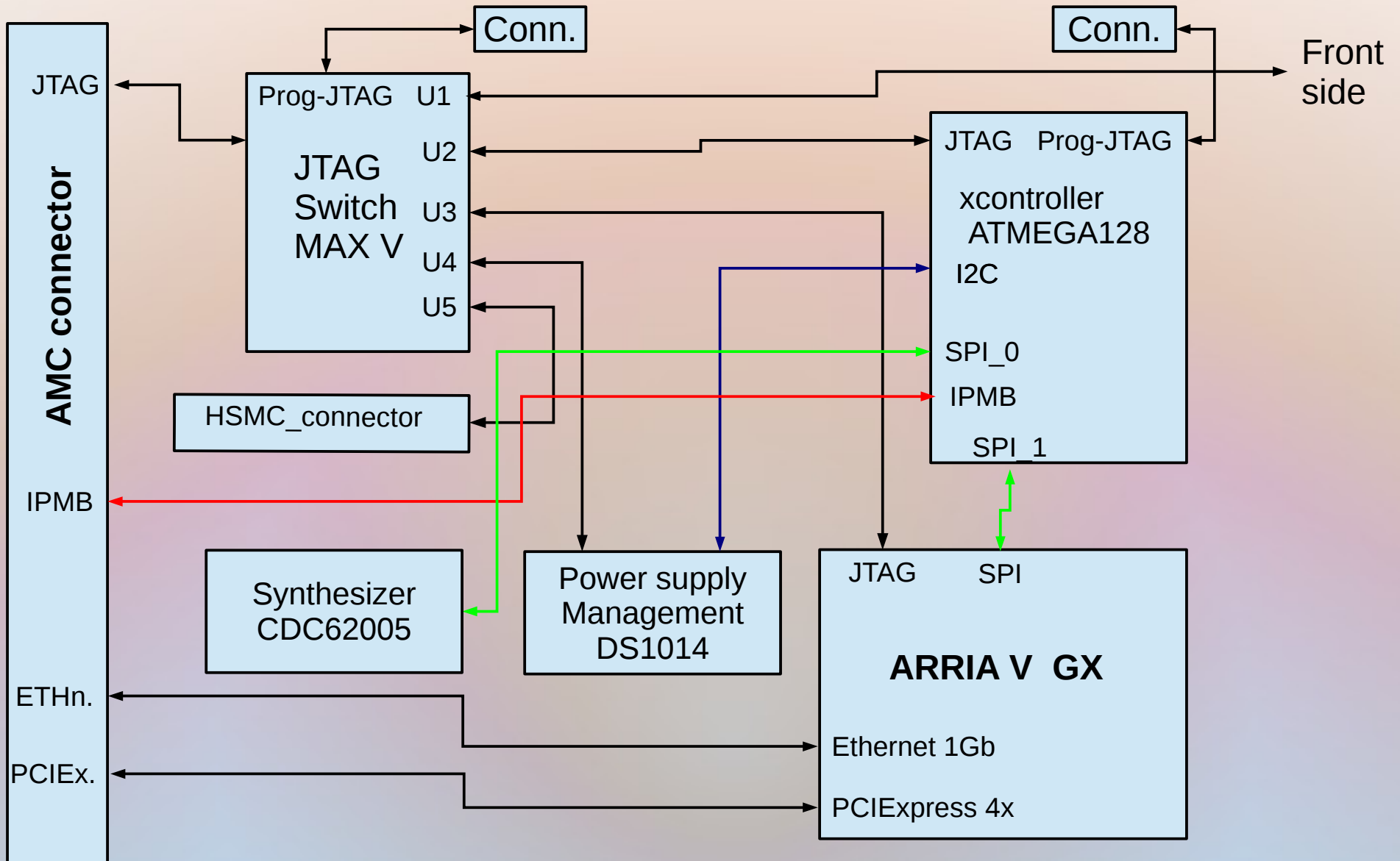
Caractéristique principale

- MicroTCA 4.x double-width full size
- Interface
 - PCIExpress Gen 2 4x (hard IP)
 - Ethernet (custom made)
- FPGA ARRIA V GX (5AGXMA3D4F31C5M)
- Configuration
 - Active serial (Quad SPI 128 Mbits)
 - JTAG
 - Partial configuration (Ethernet)
 - CvP (configuration via protocol)
- SSRAM 18Mbits
- HSMC connector

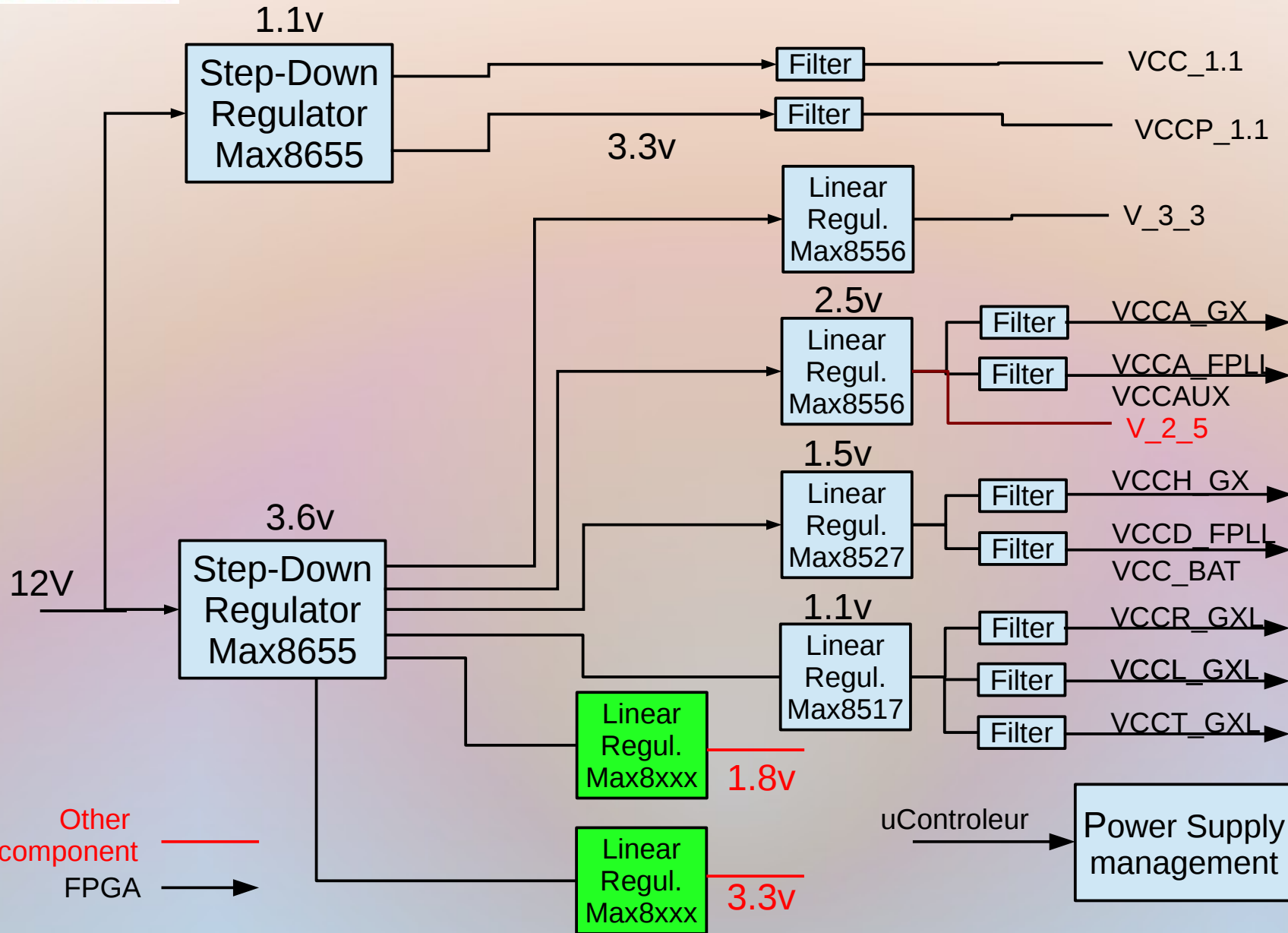




Bus tree

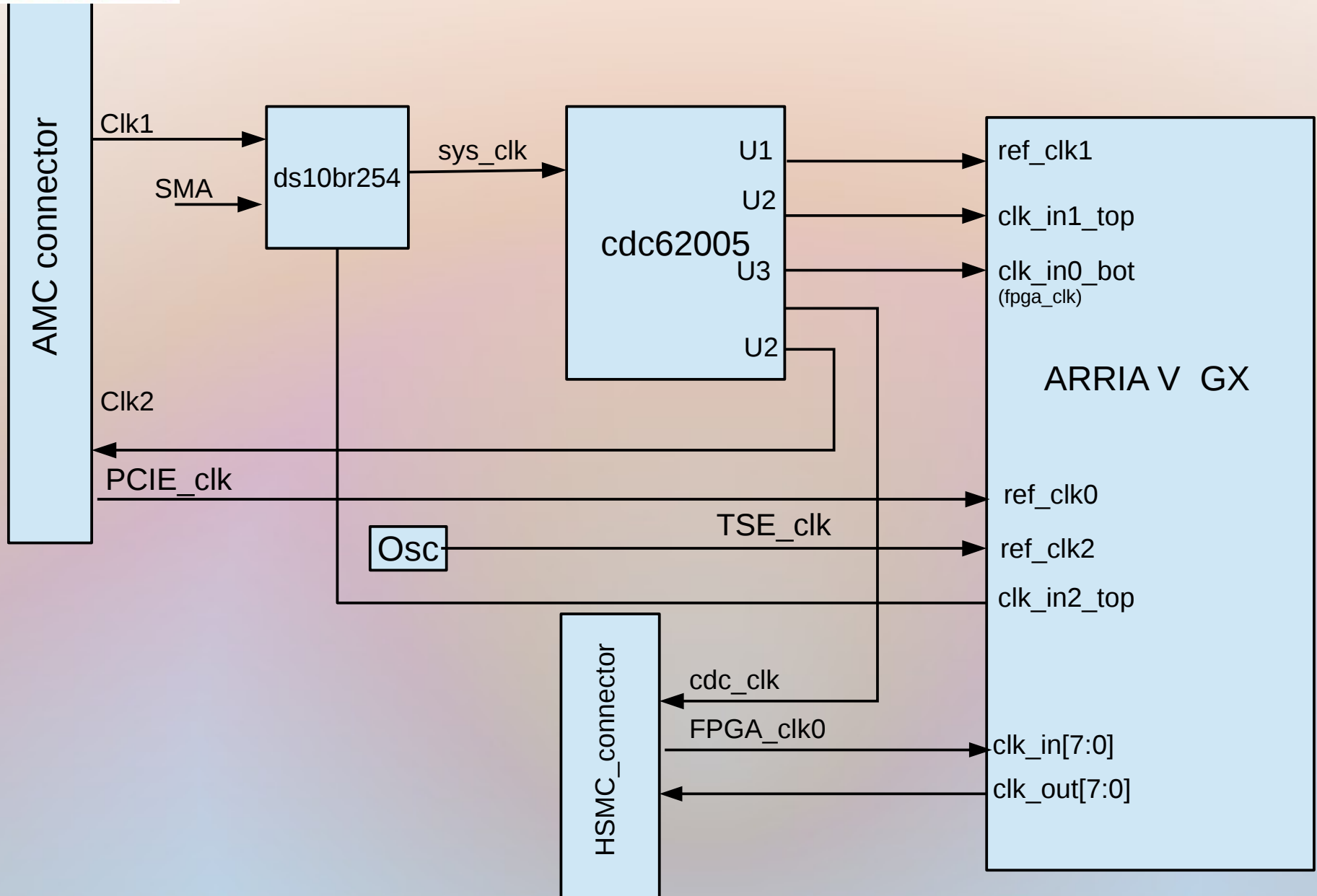


Power supply





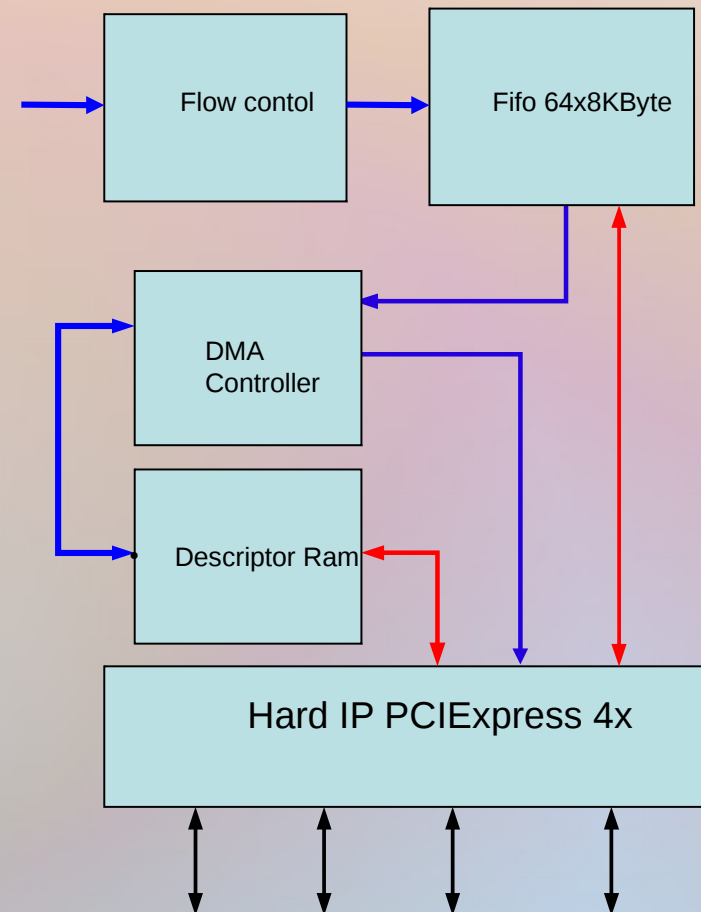
Clock tree





PCIExpress interface

The screenshot shows the Altera SOPC Builder interface. The 'System Contents' pane on the left lists various components like MM_interface, Nios II Processor, serial32_R, streaming_io_interface, streaming_pattern, Bridges and Adapters, Interface Protocols, Legacy Components, Memories and Memory Controllers, Peripherals, PLL, USB, and Video and Image Processing. The 'Connections' pane shows a detailed view of the system's internal connections, with a central clock source 'cal_clk' connected to numerous modules. The 'Module Name' and 'Description' columns provide details for each component, such as 'pci_express_compiler' (PCI Express Compiler), 'onchip_mem' (On-Chip Memory), and 'fifo' (Avalon-ST Single Clock FIFO). The 'Clock' column indicates the clock source for each module, and the 'Base' and 'End' columns show the memory addresses. The 'PIO' column indicates the Peripheral Interconnect (PIO) inputs and outputs for each module.





FPGASYSPLANNER

Allegro 4 FPGA System Planner Option - [/exp/elec/charlet/LHCb/SpecsPCIE/sfp/specsv2a5/specsv2a5.fsp* : Design Board] (sur iao.lal.in2p3.fr)

Custom Projects Window Help

Files Abstract

Canvas Navigation

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To highlight the entries listed in order to auto on canvas, turn Auto Zoom

```
./Hcb/SpecsPCIE/sfp/specsv2a5.  
/sfp/specsv2a5/specsv2a5.fsp for editing.  
  
tch required voltage 3.3 for pin WCCPD3 ( Y21 ) in instance M1.  
  
) at x=53.07912 mm, y=92.61553 mm.  
at x=53.75519 mm, y=104.29509 mm.  
t x=55.27595 mm, y=115.45114 mm.  
iver ) at x=56.29156 mm, y=131.32166 mm.
```

Allegro Design Entry HDL XL : Allegro ... [Allegro Design Entry HDL XL : Allegro... dialcprt.dat (sur iao.lal.in2p3.fr) (sur iao.lal.in2p3.fr) Démarrage de Prendre une captur



FPGASYSPLANNER decoupling capacitor

Allegro 4.1.10A System Planner - Options

Custom Projects Window Help

tics Abstract

U1_refclk

M1

U1_conf

M1_SPI

M17

Define Decoupling Capacitors (sur iao.lal.in2p3.fr)

Decoupling capacitor for power signals connected to the instances

Decap Symbol	Pin Count	Decap Value	Decap Count
J1	8	132uf	6
V_12	8	132uf	6
inpassive:capacsym_1		22u	6
J4	1	1	0
V_3_3	161	5176uf	202
M1	40	1240uf	34
V_2_5		10u	4
inpassive:capacsym_1		1u	4
inpassive:capacsym_1		100n	8
inpassive:capacsym_1		22n	18
VCC_1_1	39	2057.6uf	56
inpassive:capacsym_1		100u	4
inpassive:capacsym_1		10u	8
inpassive:capacsym_1		2.2n	8
inpassive:capacsym_1		1u	8
inpassive:capacsym_1		100n	12
inpassive:capacsym_1		22n	16
VCCP_1_1	10	2084uf	23
inpassive:capacsym_1		100u	2
inpassive:capacsym_1		10u	2
inpassive:capacsym_1		1u	2
inpassive:capacsym_1		220p	4
inpassive:capacsym_1		100n	7
inpassive:capacsym_1		47n	6
V_3_3	40	870uf	39
inpassive:capacsym_1		100u	4
inpassive:capacsym_1		10u	4
inpassive:capacsym_1		1.0u	12
inpassive:capacsym_1		22n	19
VCC_LGX_1_1	3	56uf	5
inpassive:capacsym_1		10u	1
inpassive:capacsym_1		1u	2
inpassive:capacsym_1		22n	2
VCCF_GX_1_1	3	375.4uf	8
inpassive:capacsym_1		4.7u	2
inpassive:capacsym_1		22n	3
inpassive:capacsym_1		100n	3
VCCR_GX_1_1	5	123uf	9
inpassive:capacsym_1		10u	1
inpassive:capacsym_1		1u	3
inpassive:capacsym_1		22n	5
VCC_HGX_1_5	2	202uf	4
inpassive:capacsym_1		1.0u	2
inpassive:capacsym_1		100n	2
VCCA_FPLL_2_5	10	543.4uf	17
inpassive:capacsym_1		10u	2
inpassive:capacsym_1		4.7u	2
inpassive:capacsym_1		1u	4
inpassive:capacsym_1		100n	4
inpassive:capacsym_1		22n	5
VCCA_GX_2_5	2	201uf	3
inpassive:capacsym_1		1u	1
inpassive:capacsym_1		100n	2
VCCD_FPLL_BAT_1_5	7	400uf	4
inpassive:capacsym_1		100n	4
M10	1	122uf	2
V_3_3	1	122uf	1
inpassive:capacsym_1		100n	1
inpassive:capacsym_1		22n	1

Note: Ensure that power regulators are defined and mapped in the design before defining decoupling capacitors.

OK

```

Hcb/SpecsPCIe/sfp/specsv2a5.
/sfp/specsv2a5/specsv2a5.fsp for editing.

ch required voltage 3.3 for pin VCCPD3 ( Y21 ) in instance M1.

) at x=53.07312 mm, y=92.61553 mm.
at x=53.75513 mm, y=104.29503 mm.
: x=55.27595 mm, y=115.45114 mm.
iver ) at x=56.29156 mm, y=131.32166 mm.

```

[Allegro Design Entry HDL XL : Allegro... [Allegro Design Entry HDL XL : Allegro... [dialcprt.dat (sur iao.lal.in2p3.fr)] (sur iao.lal.in2p3.fr) Démarrage de Pre



FPGASYSPLANNER Power supply

Power Mapping Editor (sur iao.lal.in2p3.fr)

Collapse Sort Ascending Sort Descending Filter Find Cut Copy Paste Show/Hide Columns Reset Width Clear Highlight Refresh Update From CSV Export To CSV Define Regulators Auto Map Regulators Map Regulators Check Connection Reset All Import Reg.

Pin Number	Signal Name	Voltage Level	Regulator Voltage	Regulator Name	Power Filter	External Port	External Net Name
V18	VCC	1.1	1.1	VCC_1_1		<input type="checkbox"/>	
V20	VCC	1.1	1.1	VCC_1_1		<input type="checkbox"/>	
M16	VCCA_FPLL	2.5	2.5	VCCA_FPLL_2_5		<input type="checkbox"/>	
P9	VCCA_FPLL	2.5	2.5	VCCA_FPLL_2_5		<input type="checkbox"/>	
P22	VCCA_FPLL	2.5	2.5	VCCA_FPLL_2_5		<input type="checkbox"/>	
T9	VCCA_FPLL	2.5	2.5	VCCA_FPLL_2_5		<input type="checkbox"/>	
T22	VCCA_FPLL	2.5	2.5	VCCA_FPLL_2_5		<input type="checkbox"/>	
W16	VCCA_FPLL	2.5	2.5	VCCA_FPLL_2_5		<input type="checkbox"/>	
V24	VCCA_GXBL0	2.5	2.5	VCCA_GX_2_5		<input type="checkbox"/>	
P24	VCCA_GXBL1	2.5	2.5	VCCA_GX_2_5		<input type="checkbox"/>	
K26	VCCBAT	1.5	1.5	VCCD_FPLL_BAT_1_5		<input type="checkbox"/>	
M8	VCCD_FPLL	1.5	1.5	VCCD_FPLL_BAT_1_5		<input type="checkbox"/>	
M15	VCCD_FPLL	1.5	1.5	VCCD_FPLL_BAT_1_5		<input type="checkbox"/>	
N22	VCCD_FPLL	1.5	1.5	VCCD_FPLL_BAT_1_5		<input type="checkbox"/>	
V9	VCCD_FPLL	1.5	1.5	VCCD_FPLL_BAT_1_5		<input type="checkbox"/>	
V22	VCCD_FPLL	1.5	1.5	VCCD_FPLL_BAT_1_5		<input type="checkbox"/>	
W15	VCCD_FPLL	1.5	1.5	VCCD_FPLL_BAT_1_5		<input type="checkbox"/>	
T24	VCCD_GXBL0	1.5	1.5	VCCD_GX_1_5		<input type="checkbox"/>	
N25	VCCD_GXBL1	1.5	1.5	VCCD_GX_1_5		<input type="checkbox"/>	
T25	VCCD_GXBL0	1.1	1.1	VCCD_GX_1_1		<input type="checkbox"/>	
T26	VCCD_GXBL0	1.1	1.1	VCCD_GX_1_1		<input type="checkbox"/>	
M25	VCCD_GXBL1	1.1	1.1	VCCD_GX_1_1		<input type="checkbox"/>	
L9	VCCP	1.1	1.1	VCCP_1_1		<input type="checkbox"/>	
L11	VCCP	1.1	1.1	VCCP_1_1		<input type="checkbox"/>	
L15	VCCP	1.1	1.1	VCCP_1_1		<input type="checkbox"/>	
L19	VCCP	1.1	1.1	VCCP_1_1		<input type="checkbox"/>	

OK Cancel Apply

M17

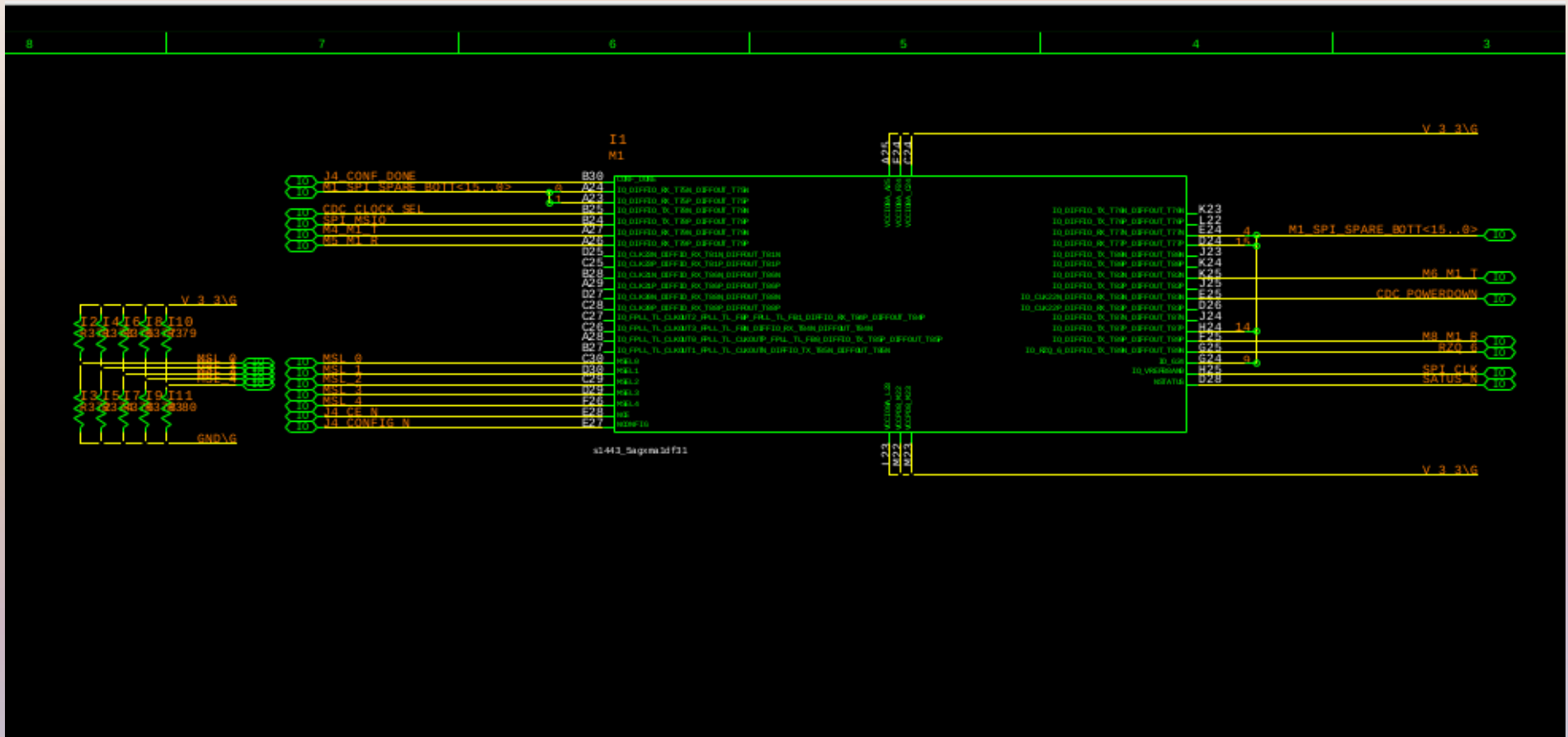
Error

```
successfully.  
c path set to /exp/elec/charlet/LHcb/SpecsPCIE/sfp/specsv2a5.  
/exp/elec/charlet/LHcb/SpecsPCIE/sfp/specsv2a5/specsv2a5.fsp for editing.  
connections...  
c v_2_5(2.5) voltage does not match required voltage 3.3 for pin VCCP03 ( V21 ) in instance M1.  
connections check.  
c HSMS_LVCMOS ( part_hsms_lvcmos ) at x=53.07912 mm, y=92.61553 mm.  
c CLOCK_LVDS ( part_clock_lvds ) at x=53.75519 mm, y=104.29509 mm.  
c HSMS_DIFF ( part_hsms_diff ) at x=55.27595 mm, y=115.45114 mm.  
c M1_TRANCEIVER ( part_m1_transceiver ) at x=56.29156 mm, y=131.32166 mm.
```

charlet] [Allegro Design Entry HDL XL : Allegro... [Allegro Design Entry HDL XL : Allegro... [dialcprt.dat (sur iao.lal.in2p3.fr)] (su

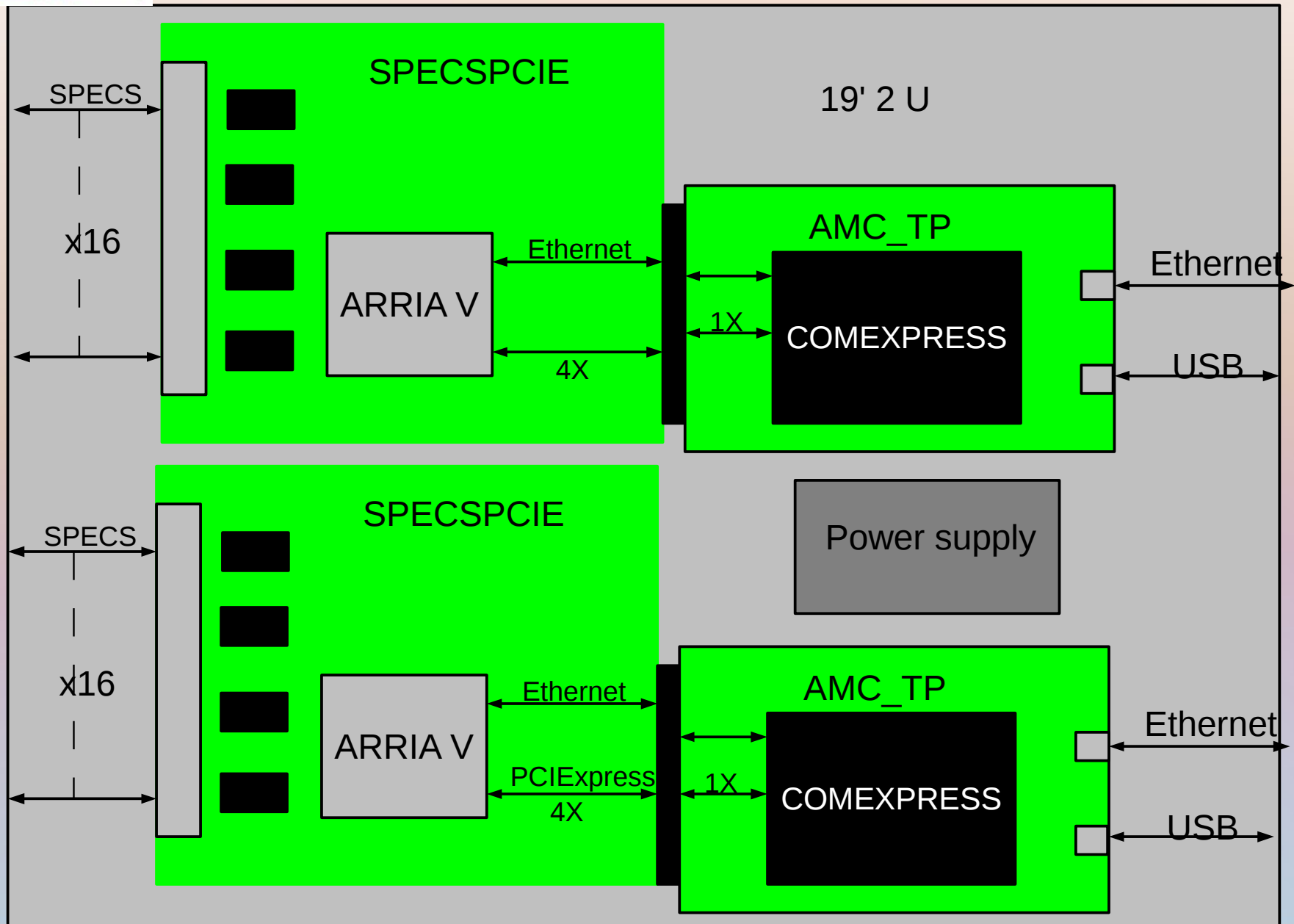


FPGASYSPLANNER schematic



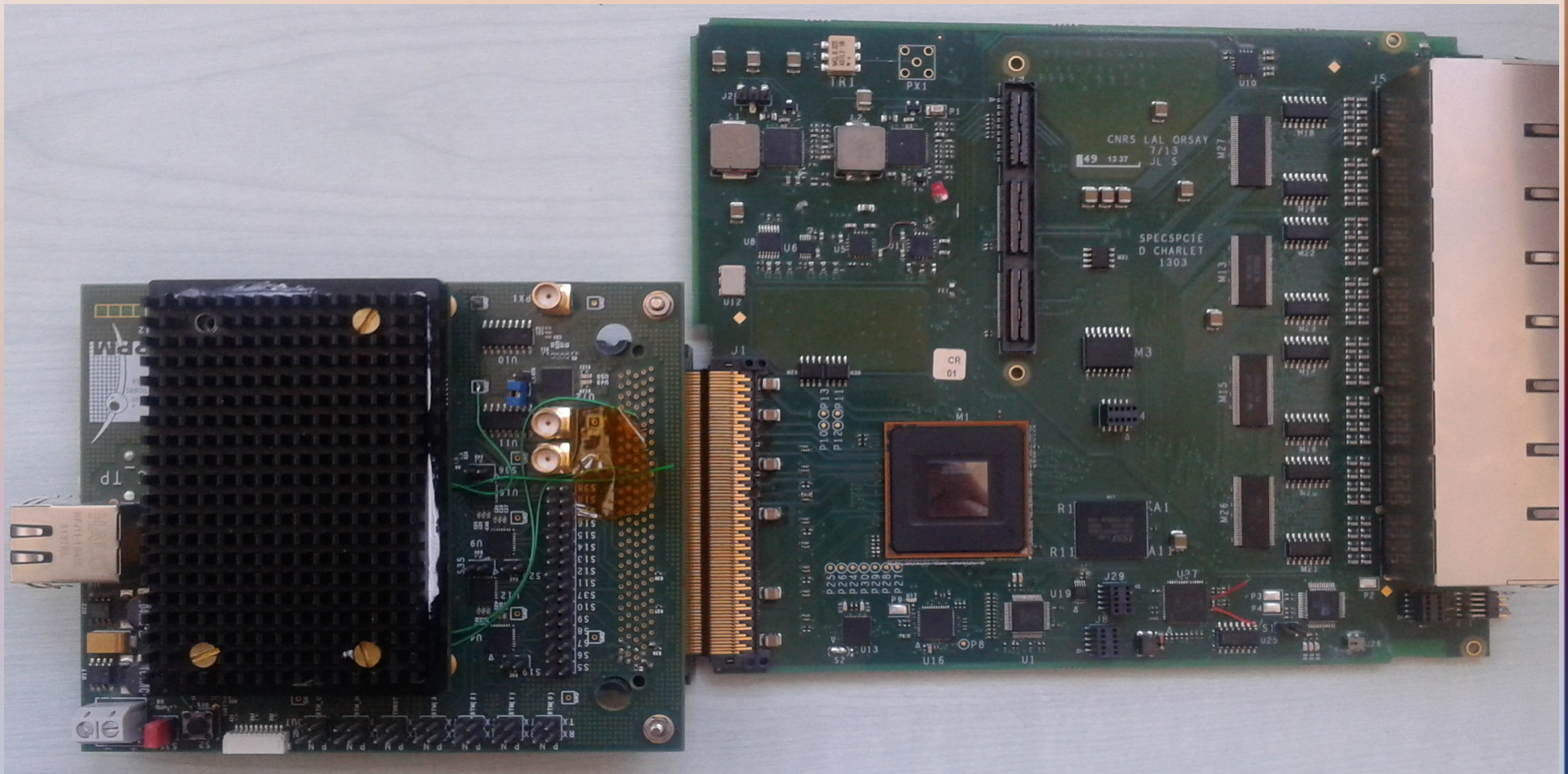


SPECS system rack implementation



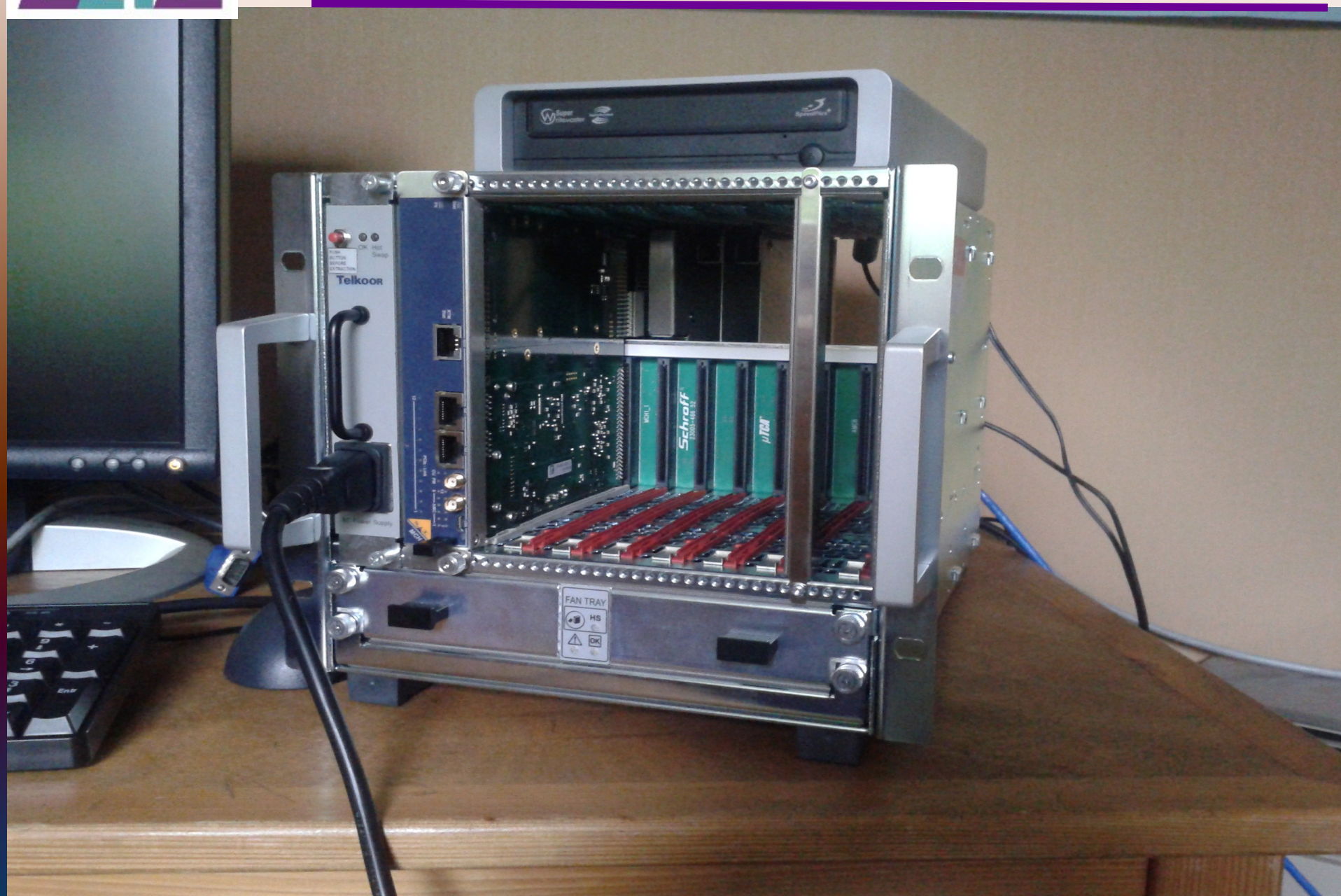


SPECS system rack implementation



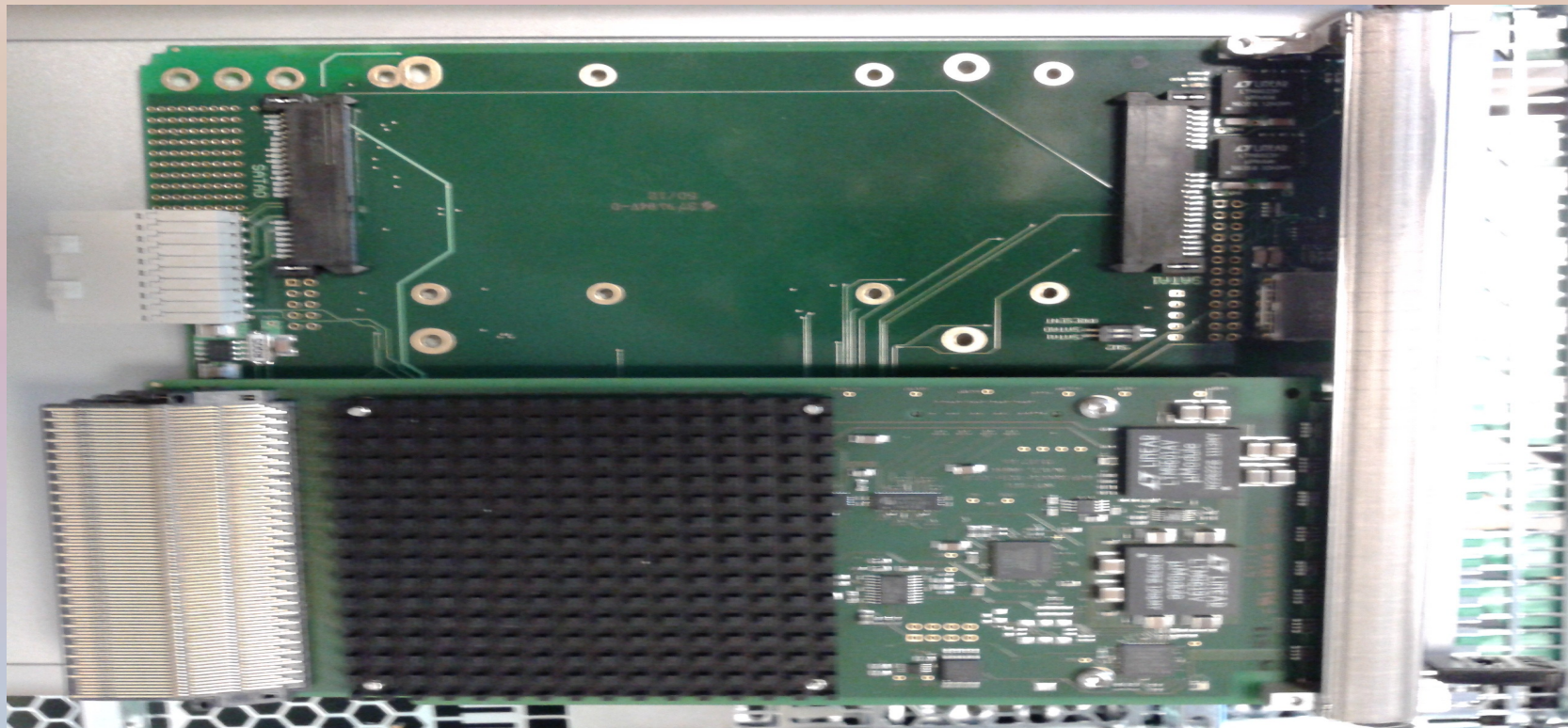
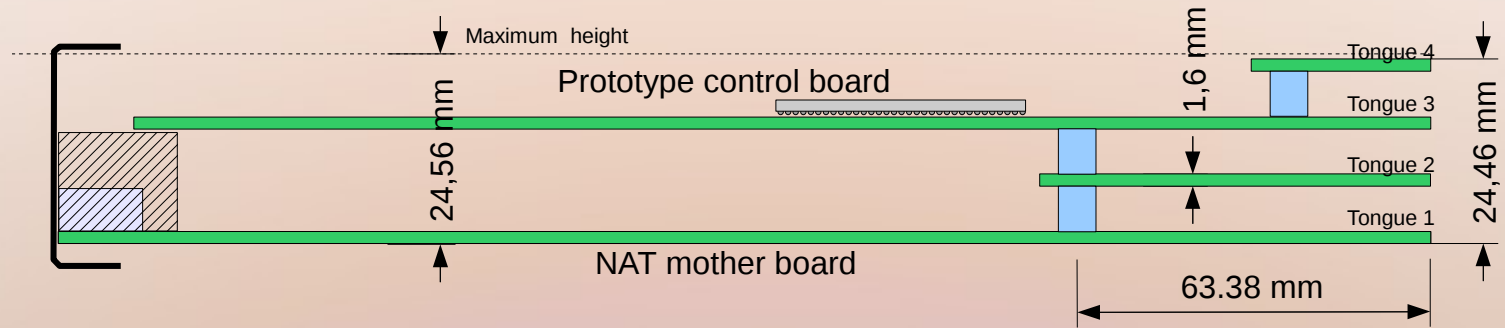


SPECS V2 Crate



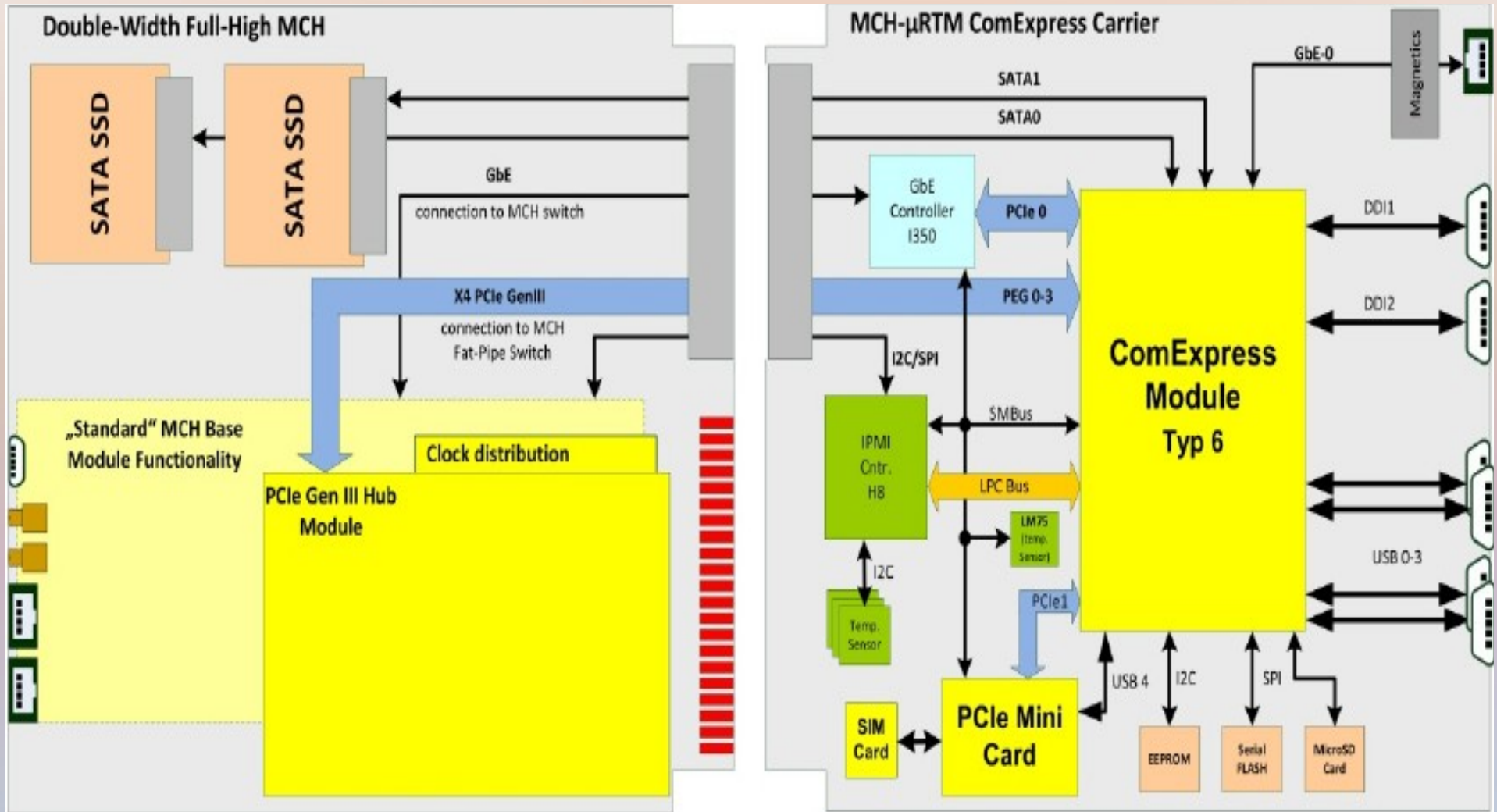


NAT MCH



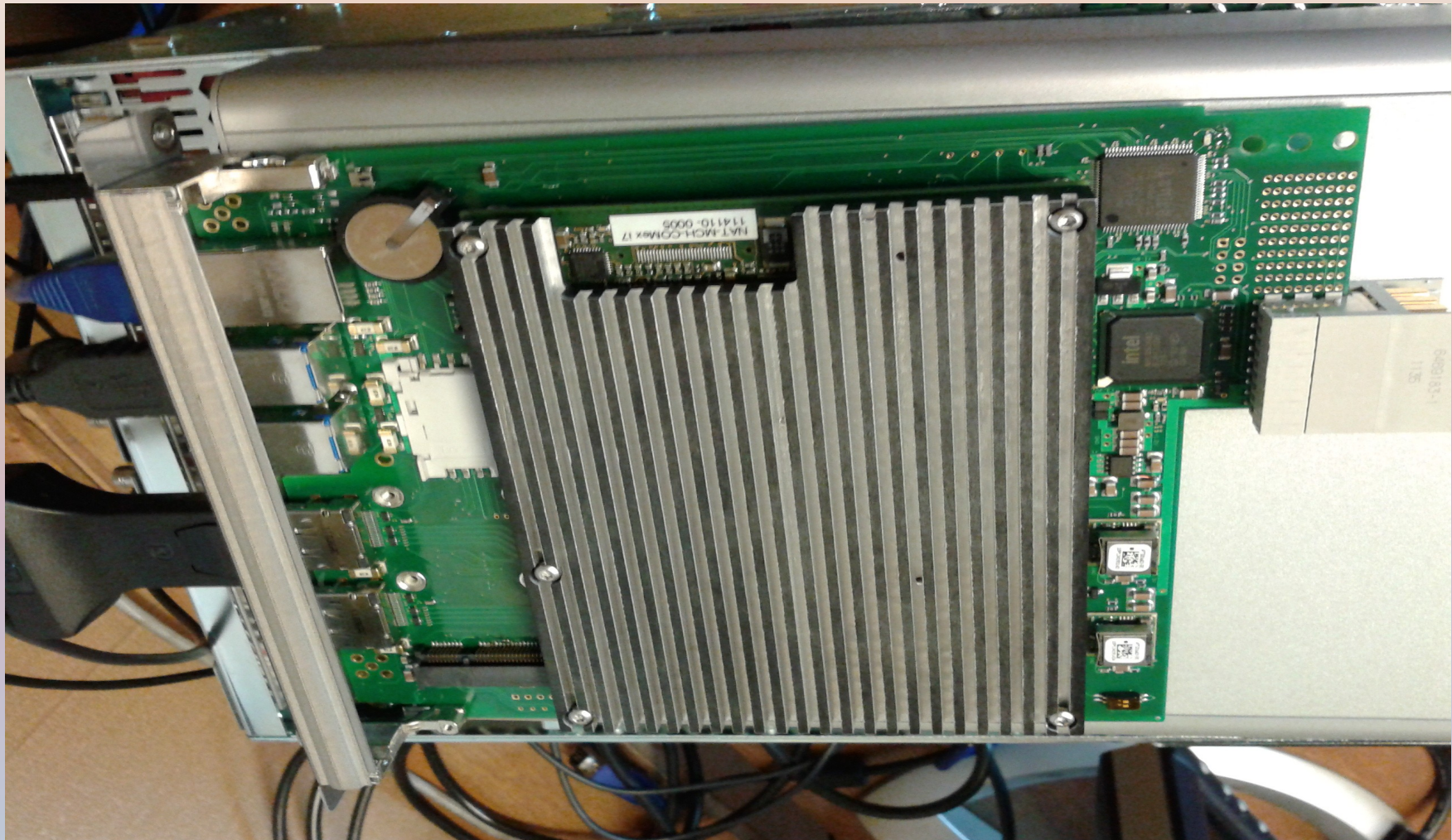


MCH-CPU





NAT CPU





Conclusion

- 21 cartes en production
- Mise en place sur cite courant Juillet
- Problèmes
 - Approvisionnement FPGA.
 - FPGAsysplanner (import export dans allegro)
 -



SPECS Frame

