# SPECS -Master_PCIE_xTCA

- L'histoire ancienne
- SPECS_Master_V2
- Les outils de développement

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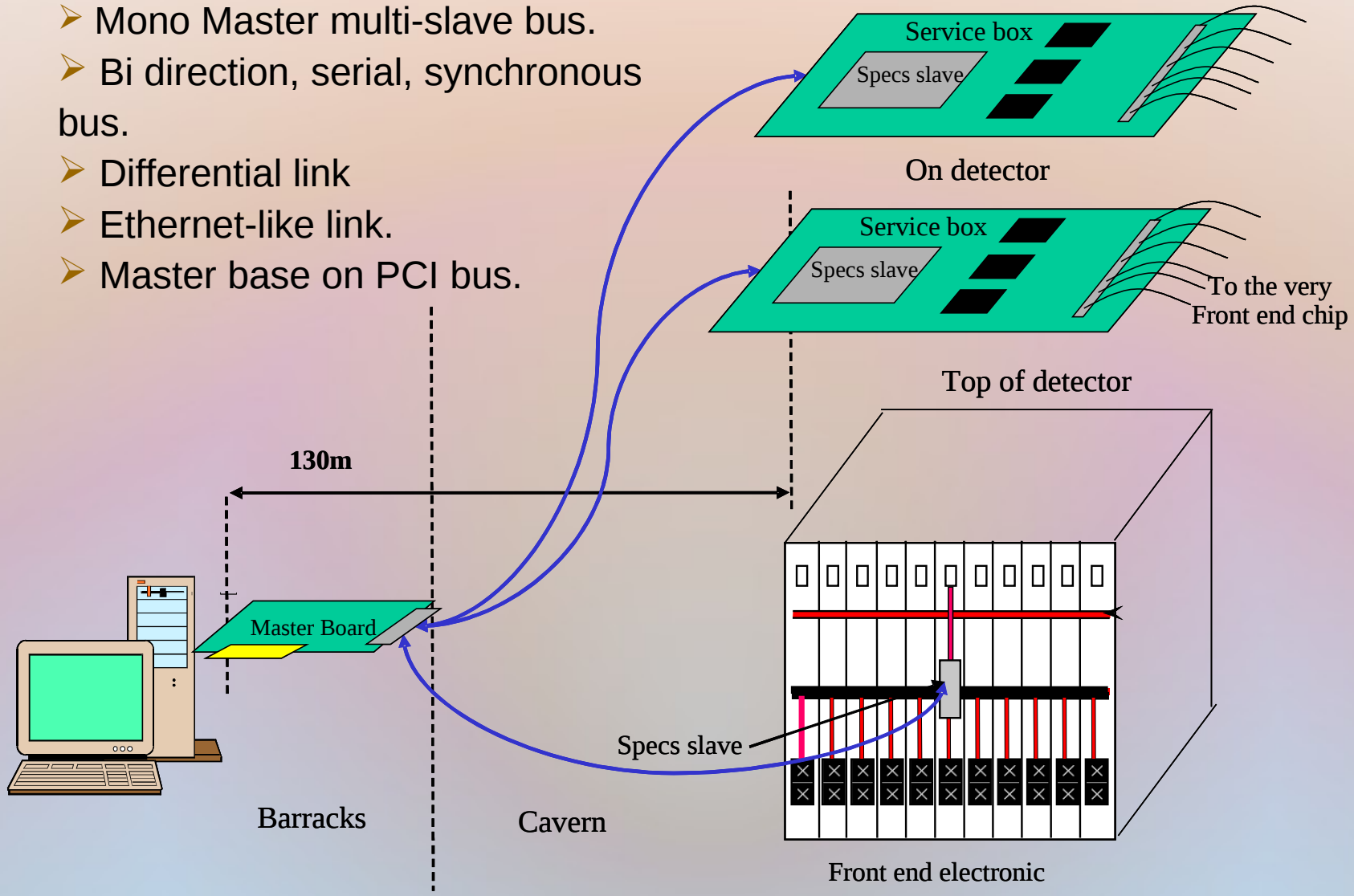
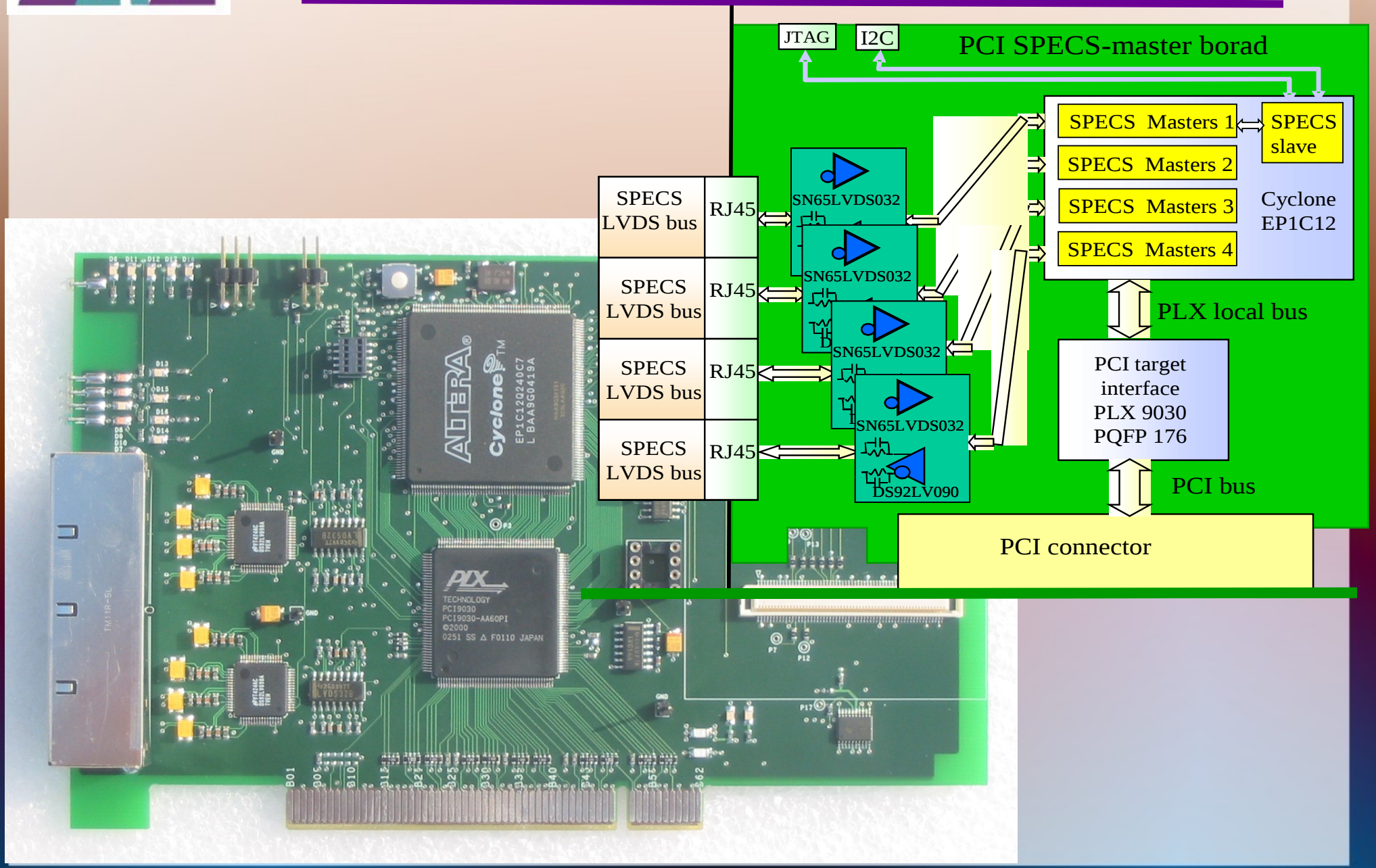
# SPECS System

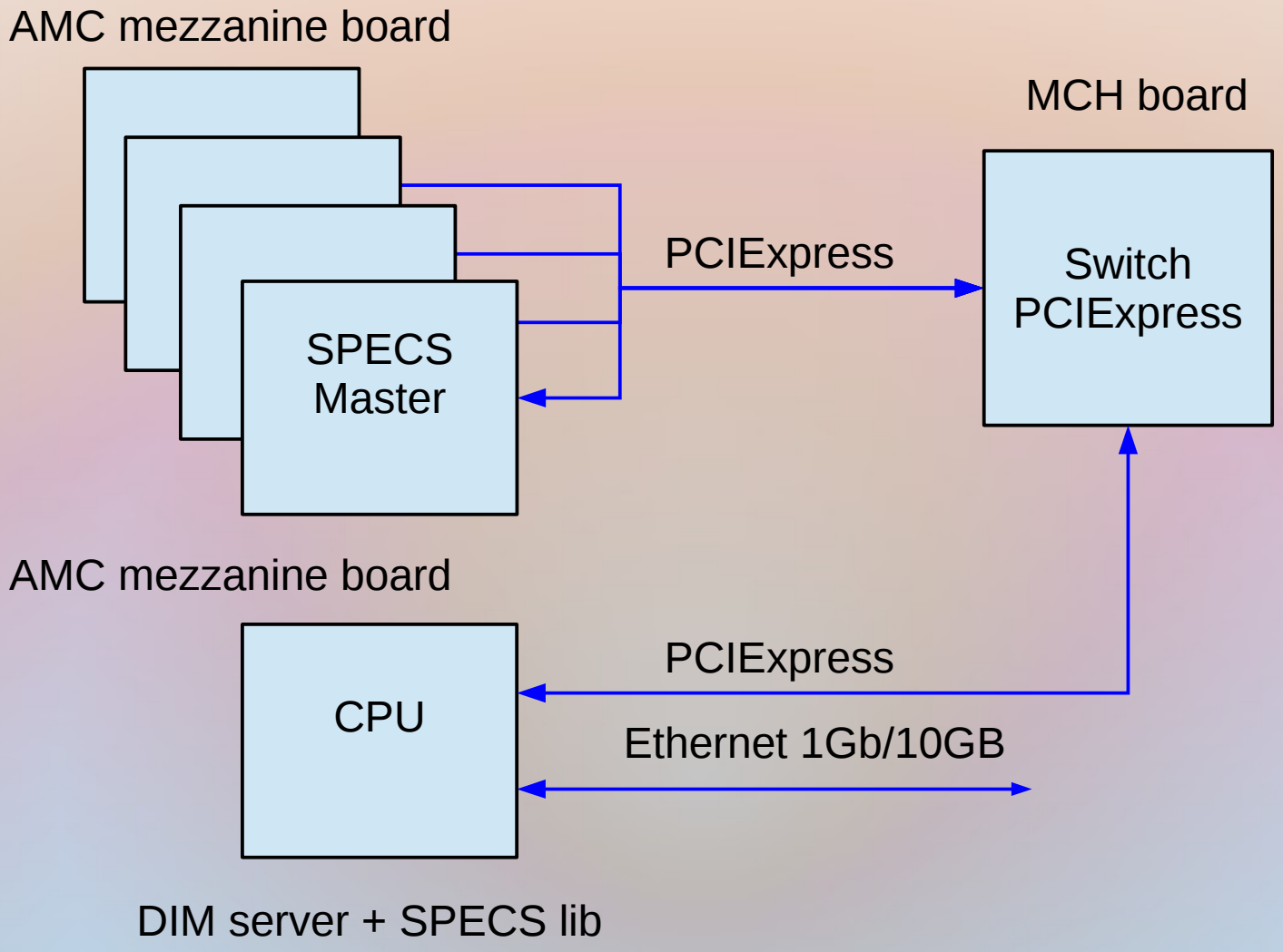
- Mono Master multi-slave bus.
- Bi direction, serial, synchronous bus.
- Differential link
- Ethernet-like link.
- Master base on PCI bus.



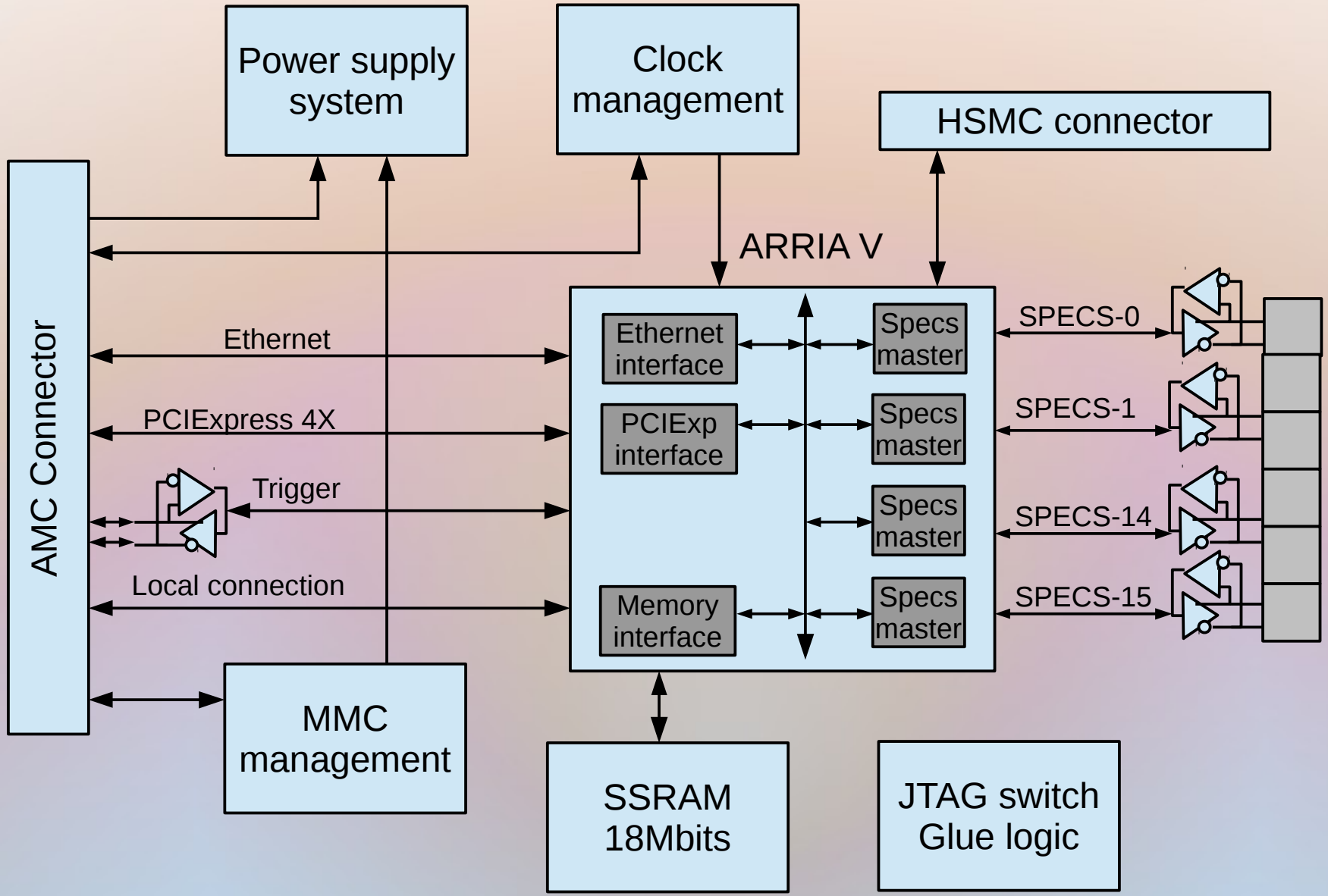
# SPECS master version 1



# SPECS master version 2



# AMC SPECS master V2



# Caractéristique principale

- MicroTCA 4.x double-with full size
- Interface

  PCIExpress Gen 2 4x (hard IP)

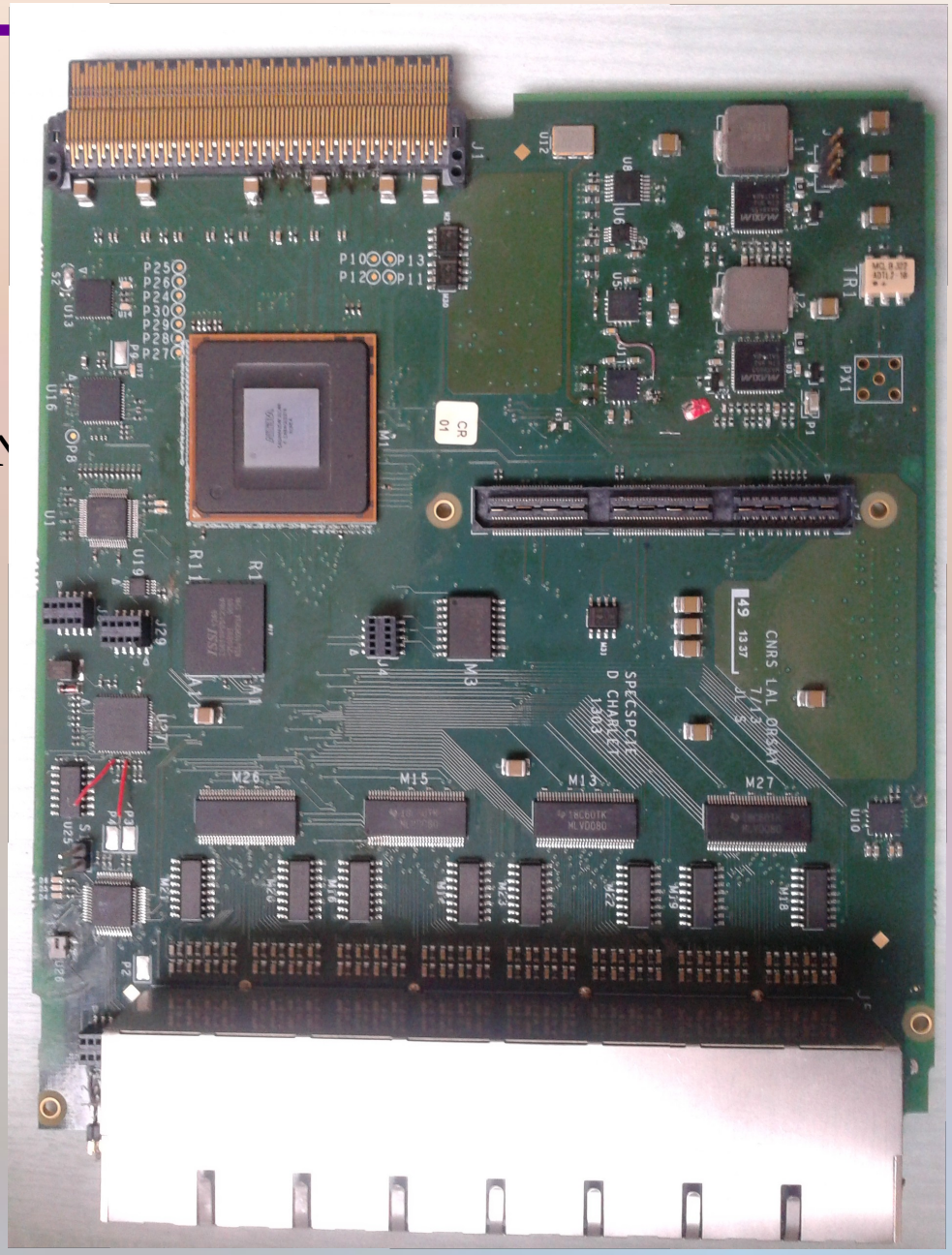
  Ethernet (custom made)
- FPGA ARRIA V GX (5AGXMA3D4F31C5N
- Configuration

  Active serial (Quad SPI 128 Mbits)

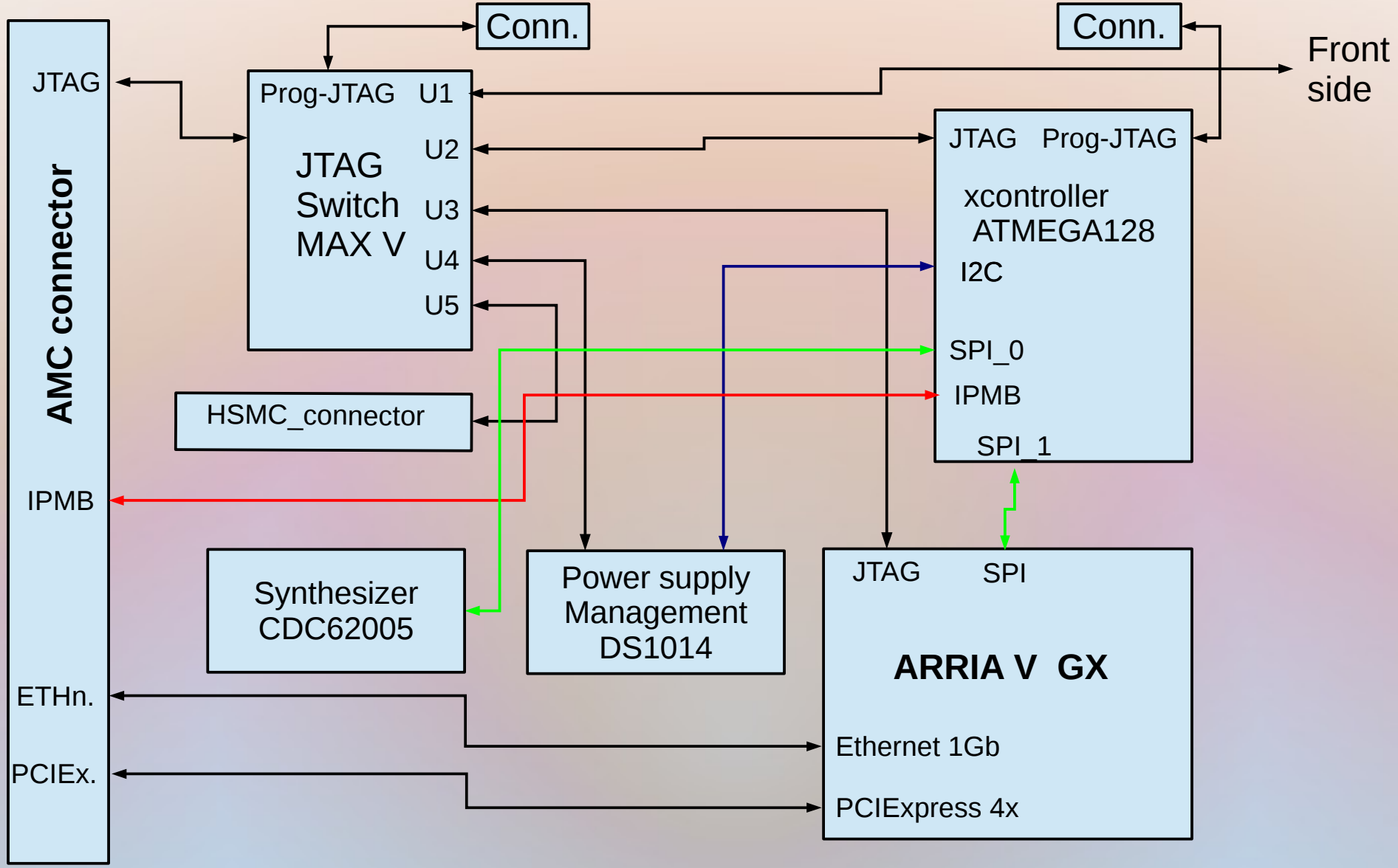
  JTAG

  Partial configuration (Ethernet)

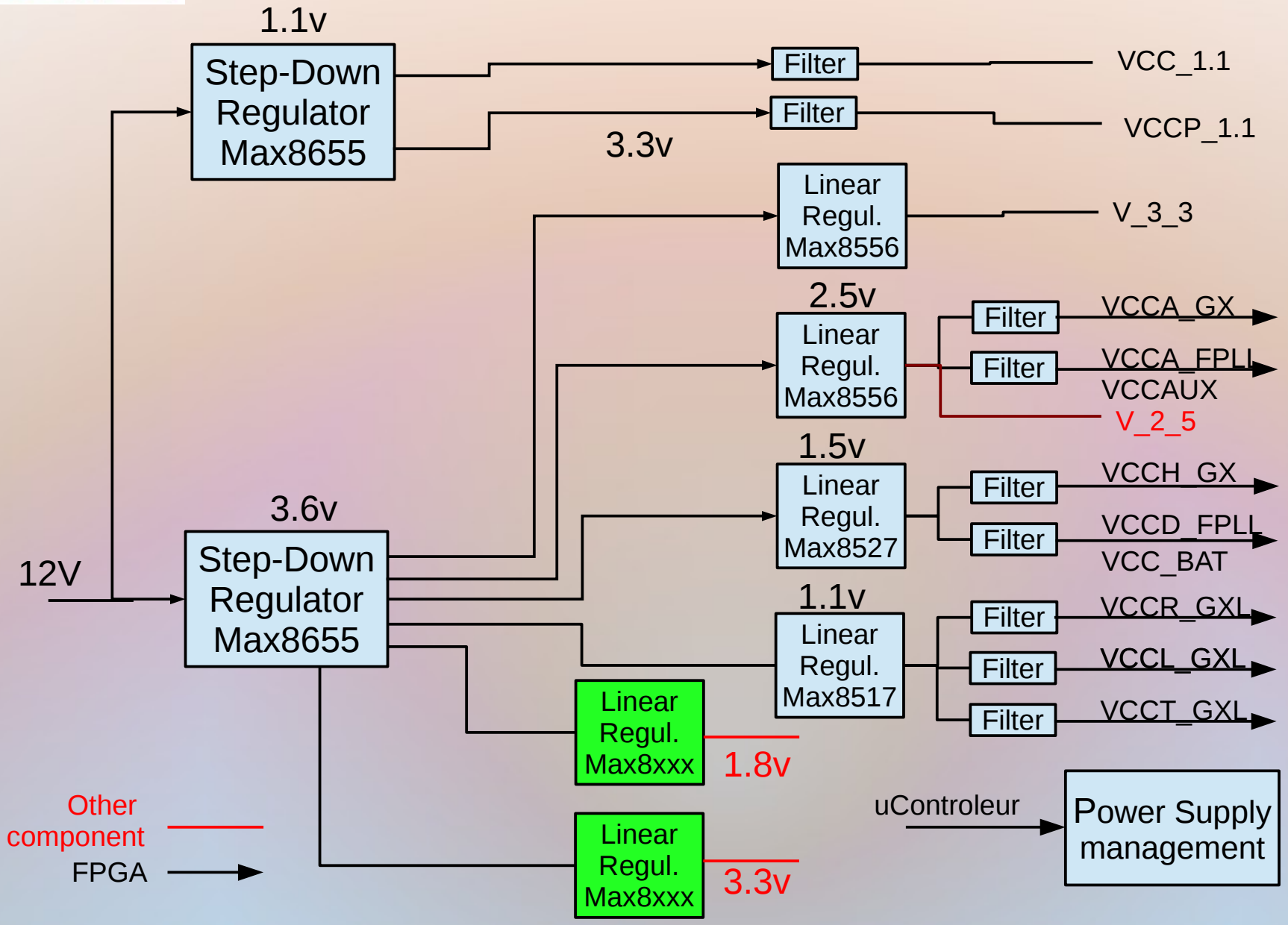
  CvP (configuration via protocol)
- SSRAM 18Mbits
- HSMC connector



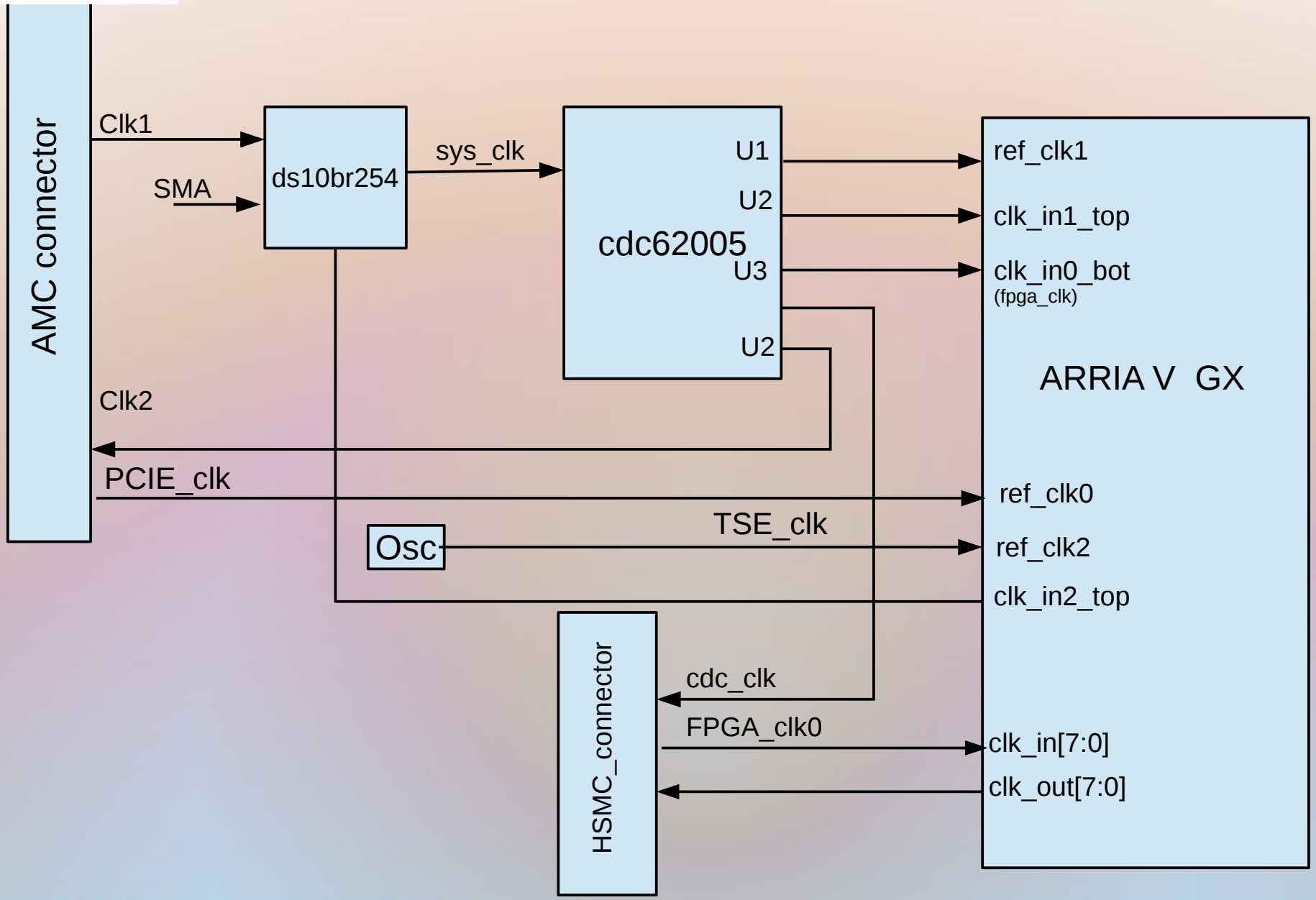
# Bus tree


Conn.
Conn.
Front side
JTAG
AMC connector
Prog-JTAG U1
U2
U3
U4
U5
JTAG Switch MAX V
JTAG Prog-JTAG
xcontroller ATMEGA128
I2C
SPI_0
IPMB
SPI_1
HSMC_connector
IPMB
Synthesizer CDC62005
Power supply Management DS1014
JTAG SPI
ARRIA V GX
ETHn.
PCIEx.
Ethernet 1Gb
PCIExpress 4x

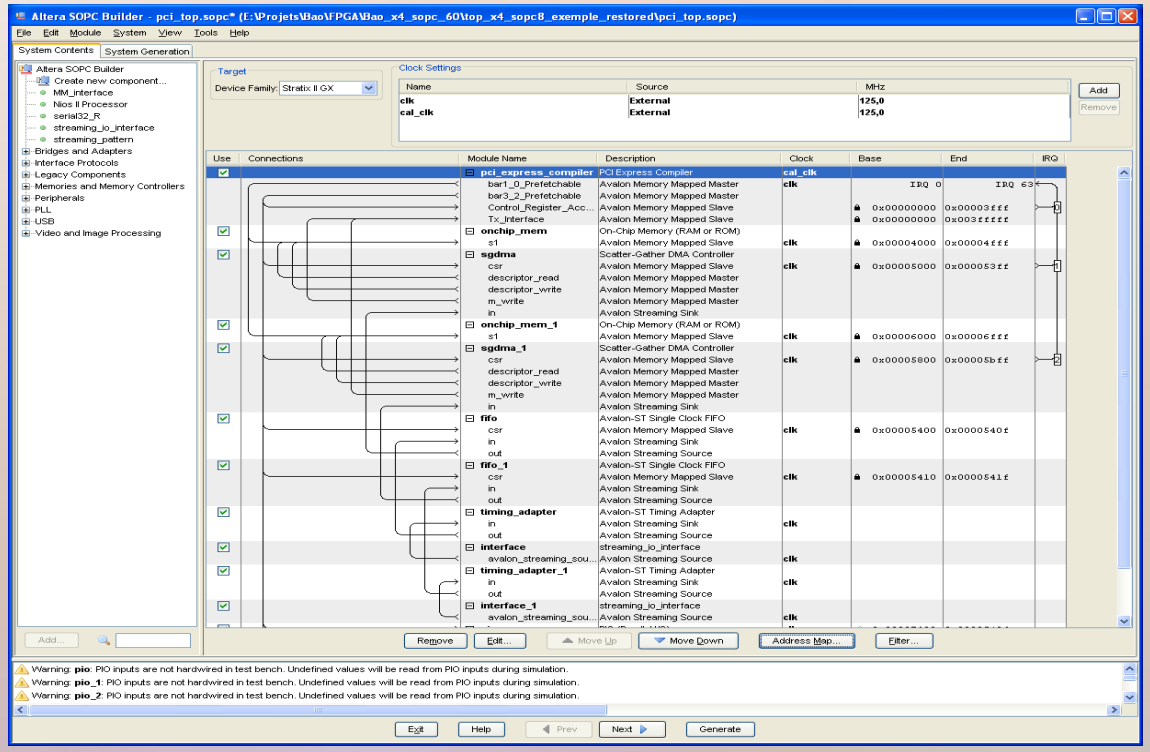
# Power supply

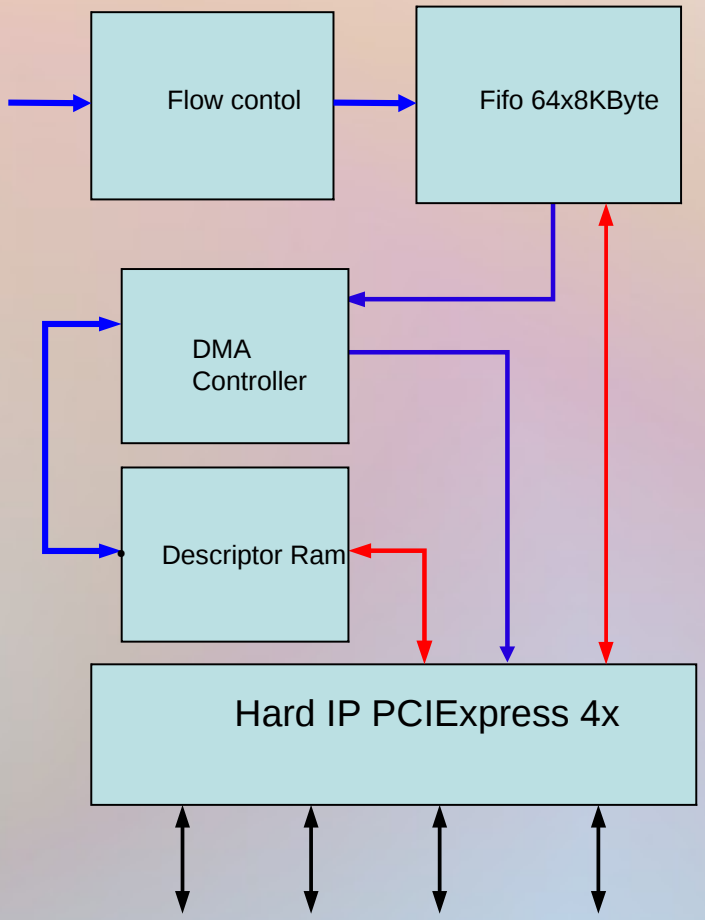


# Clock tree

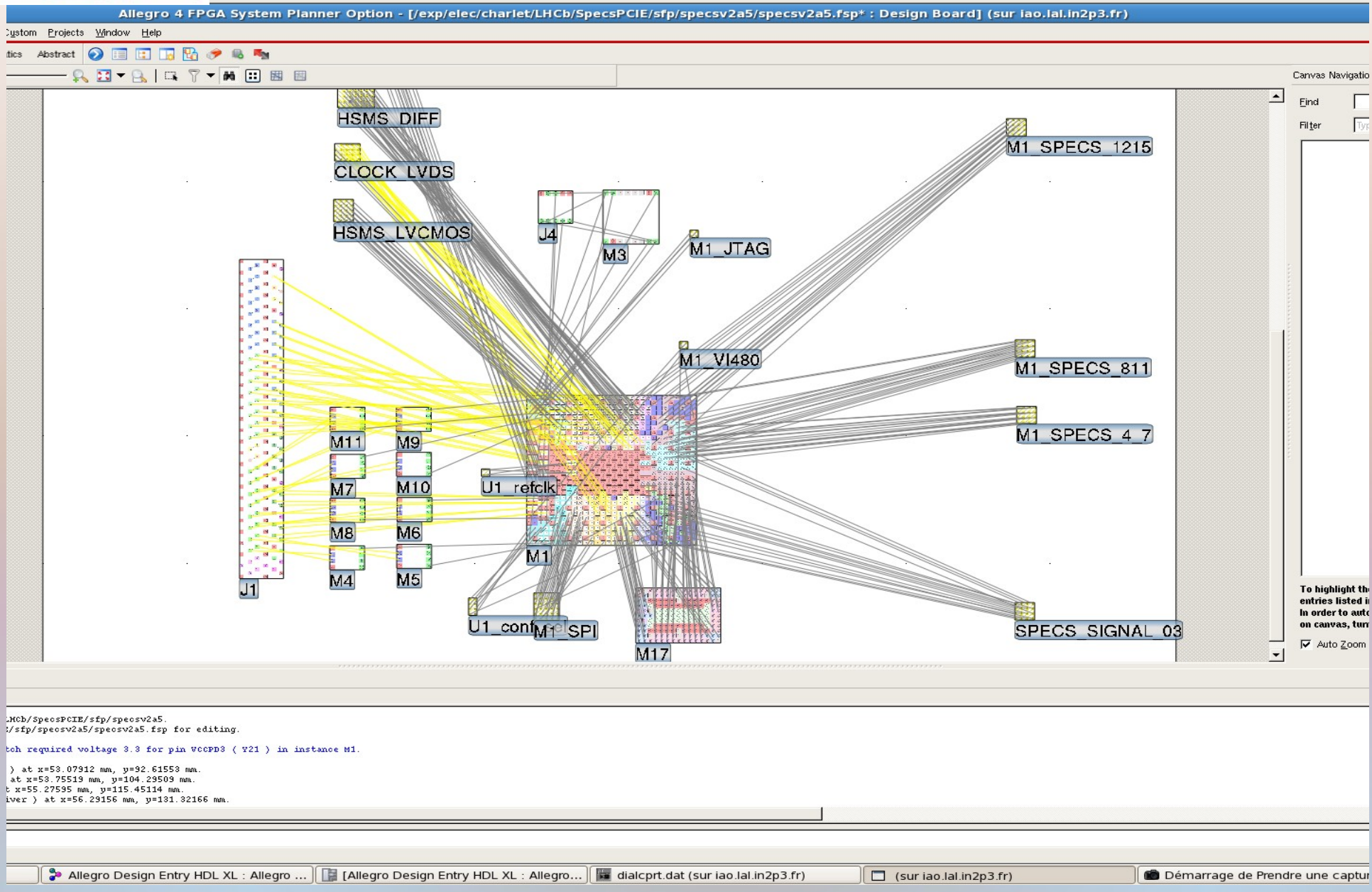

AMC connector
Clk1
SMA
ds10br254
sys_clk
cdc62005
U1
U2
U3
U2
ref_clk1
clk_in1_top
clk_in0_bot
(fpga_clk)
ARRIA V GX
Clk2
PCIE_clk
TSE_clk
Osc
ref_clk0
ref_clk2
clk_in2_top
HSMC_connector
cdc_clk
FPGA_clk0
clk_in[7:0]
clk_out[7:0]

# PCIExpress interface

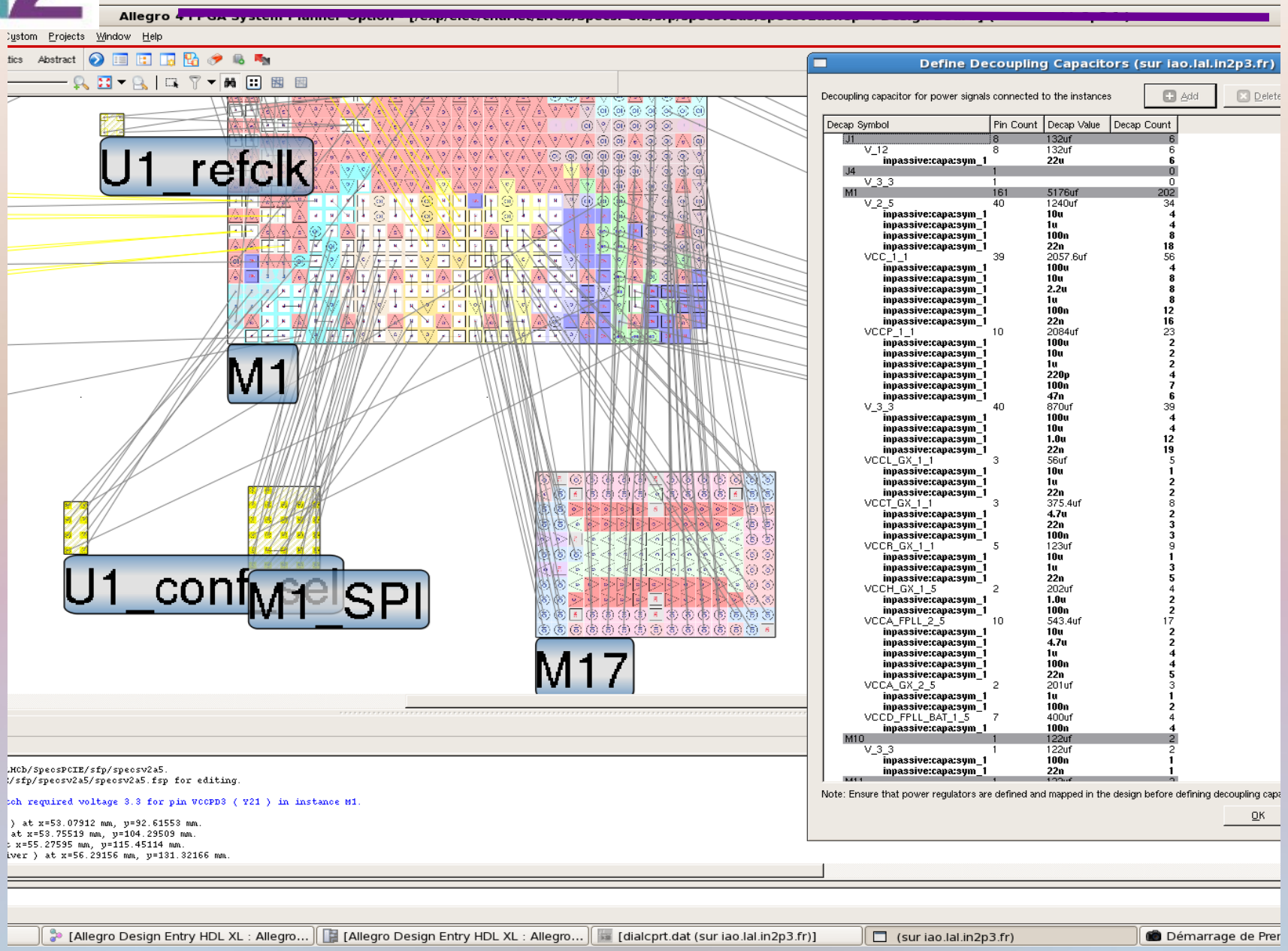


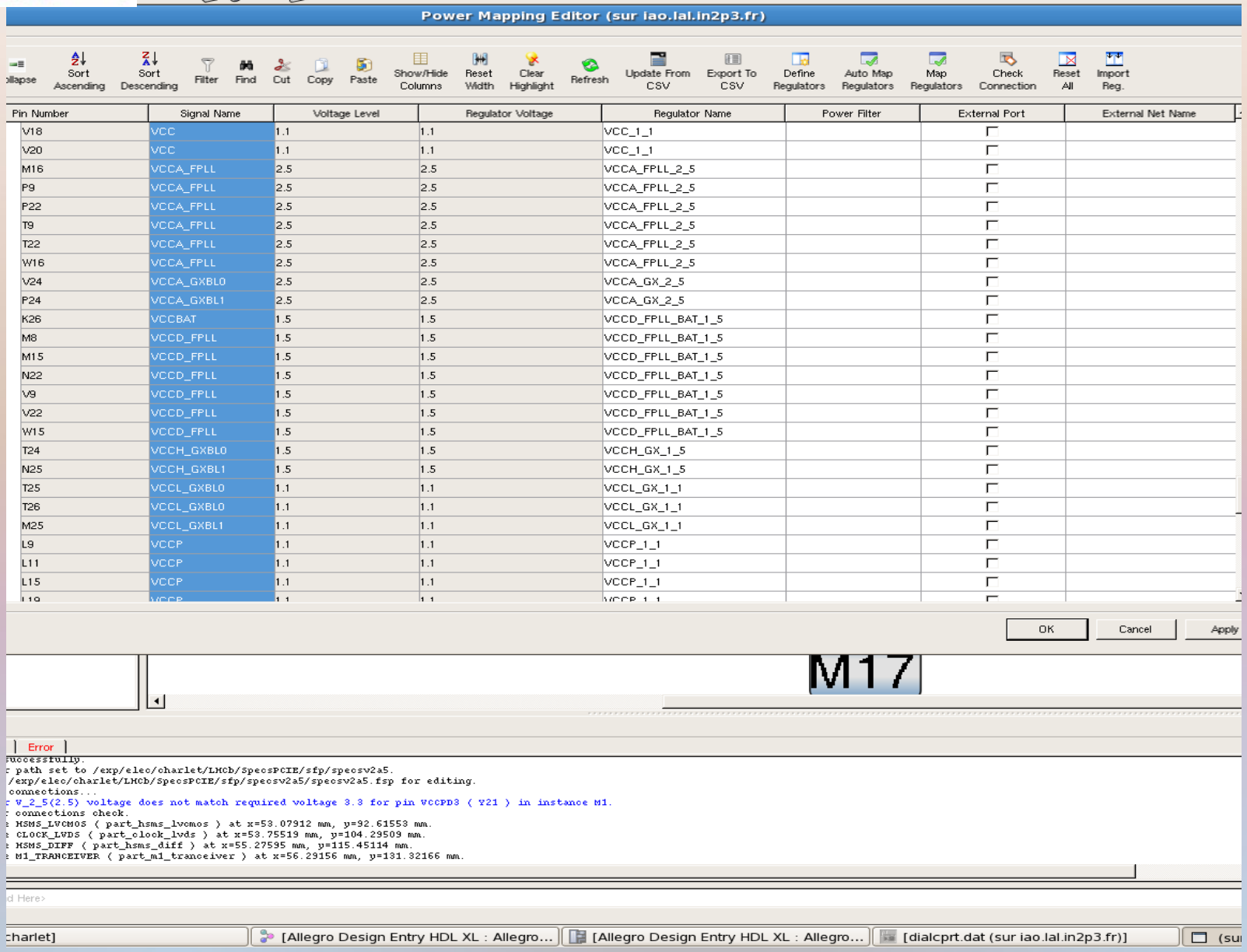
# FPGASYSPLANNER



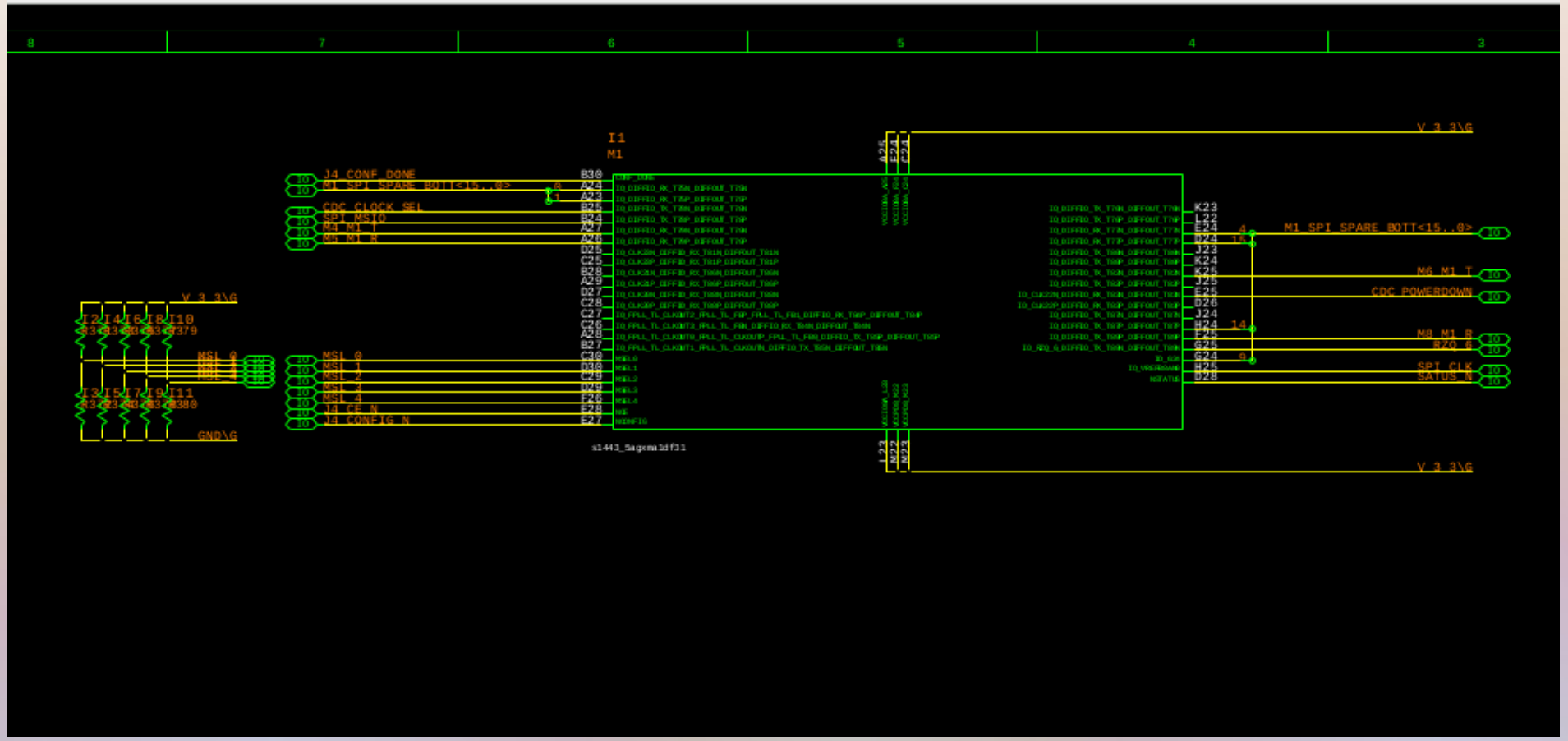
# FPGASYSPLANNER decoupling capacitor



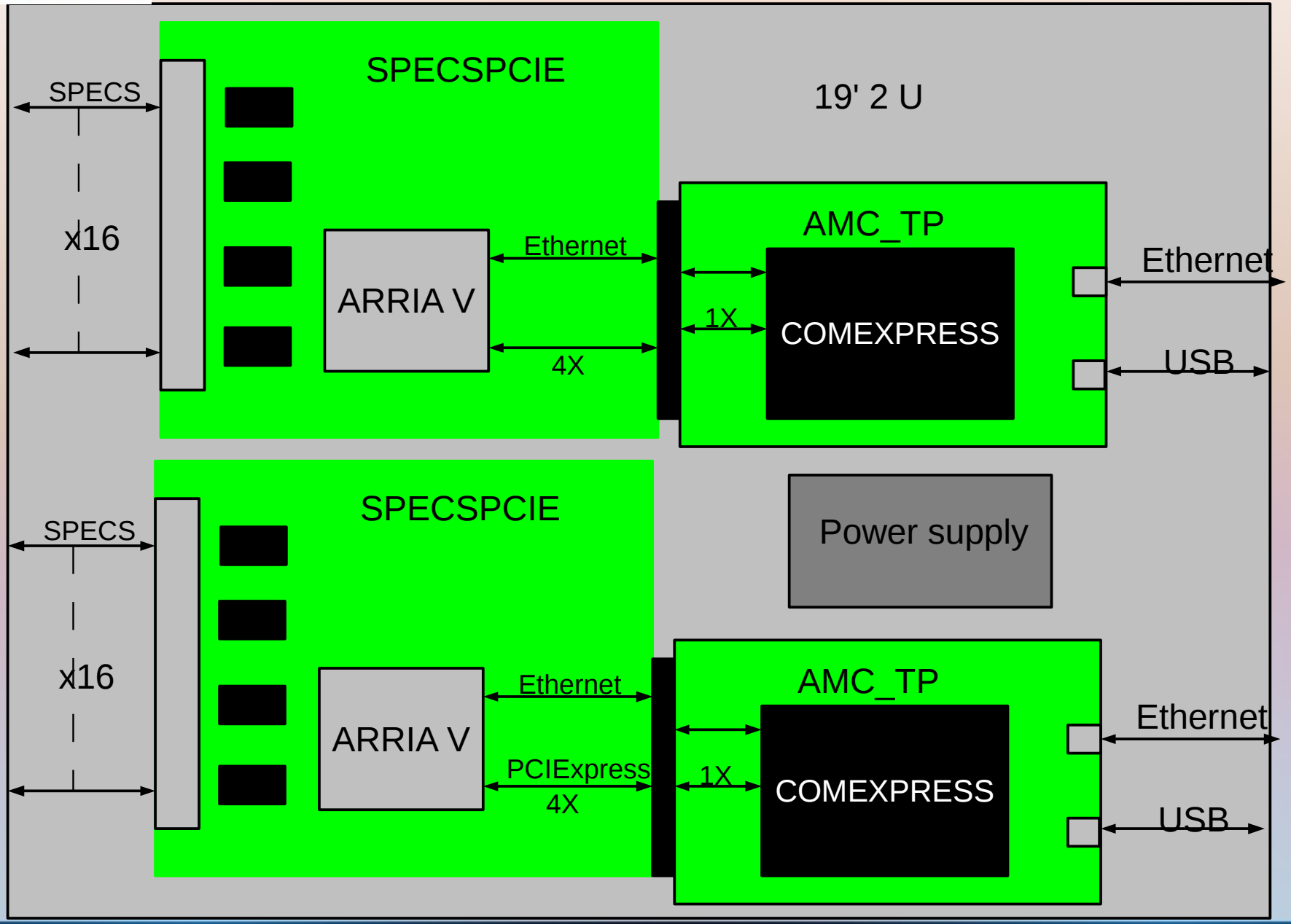
# FPGASYSPLANNER Power supply



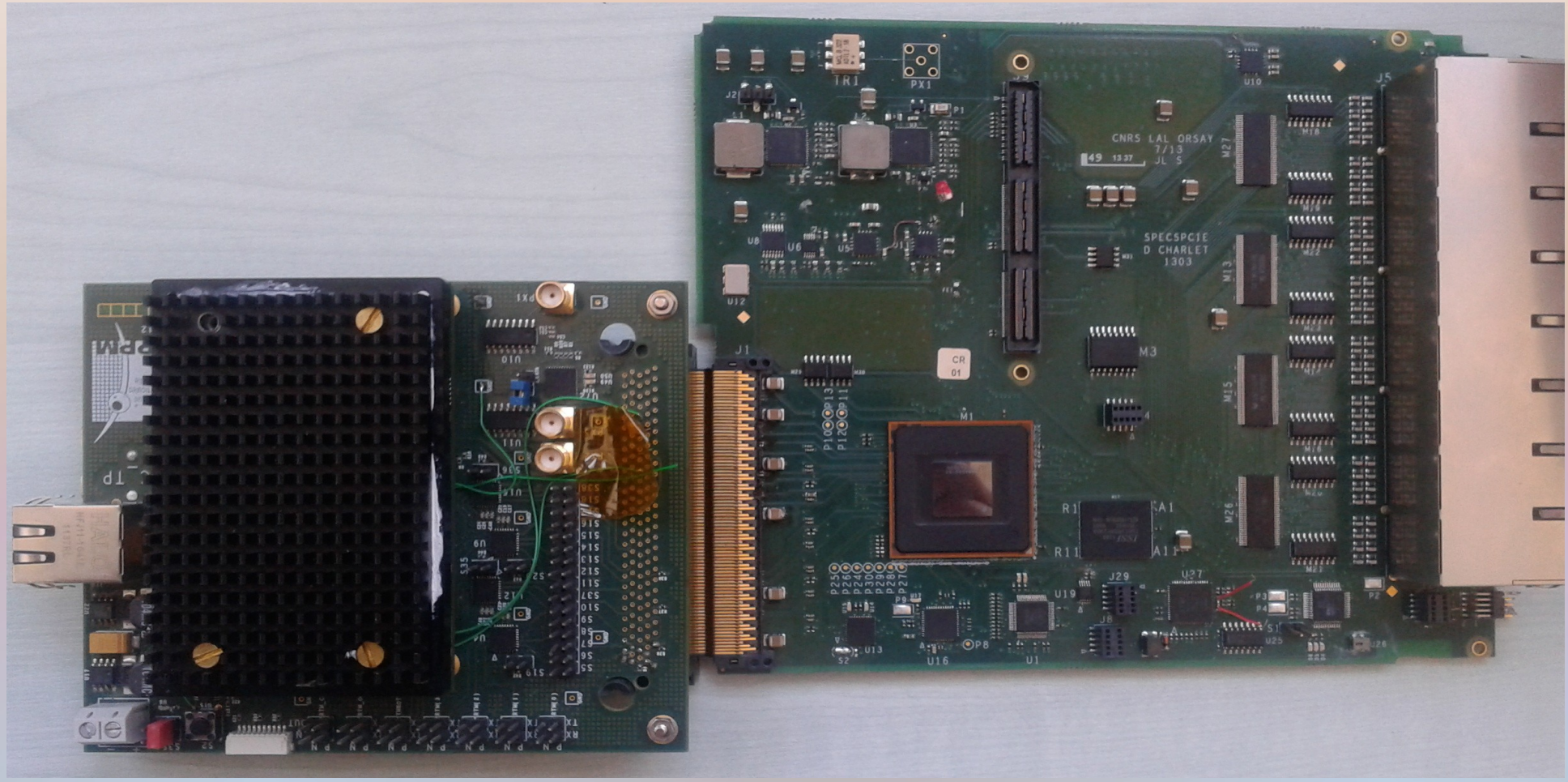
# FPGASYSPLANNER schematic



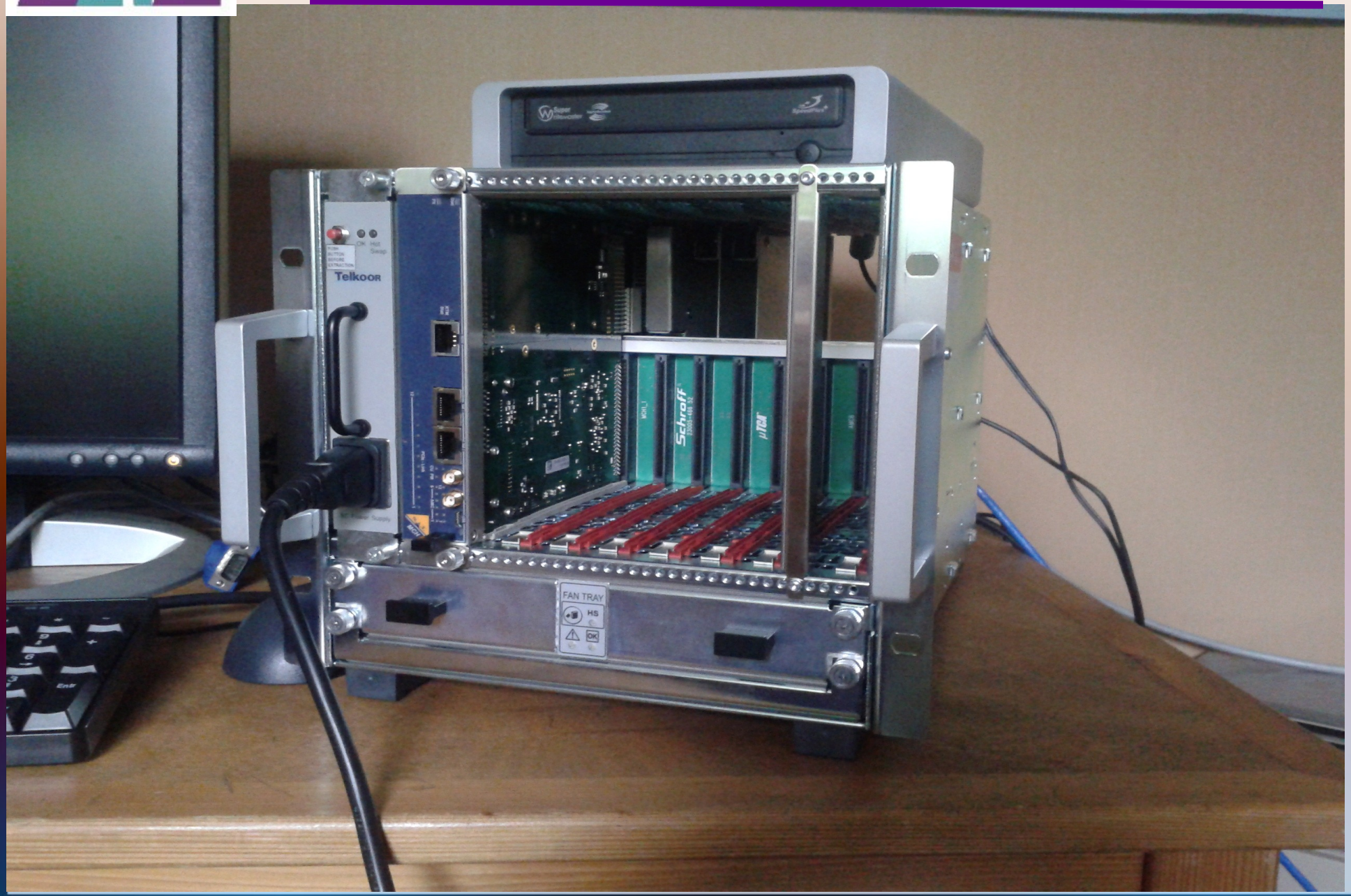
# SPECS system rack implementation



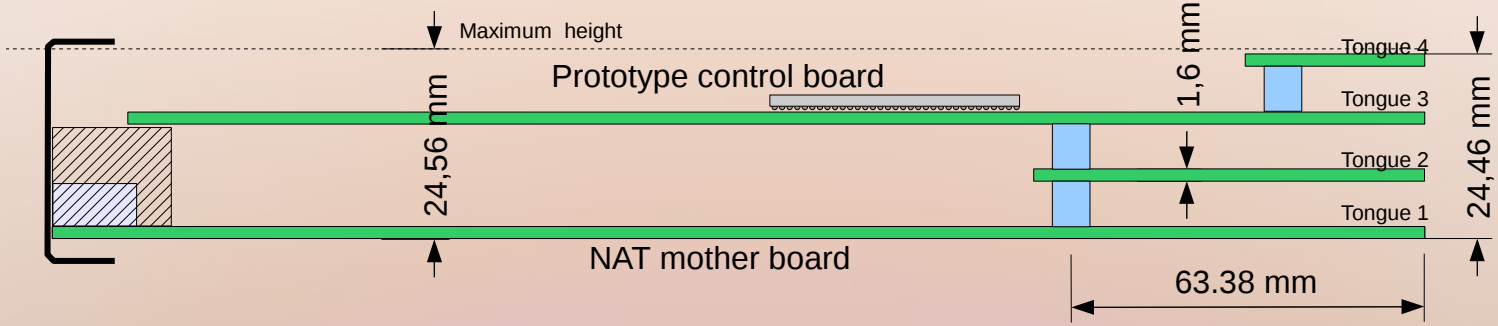
# SPECS system rack implementation

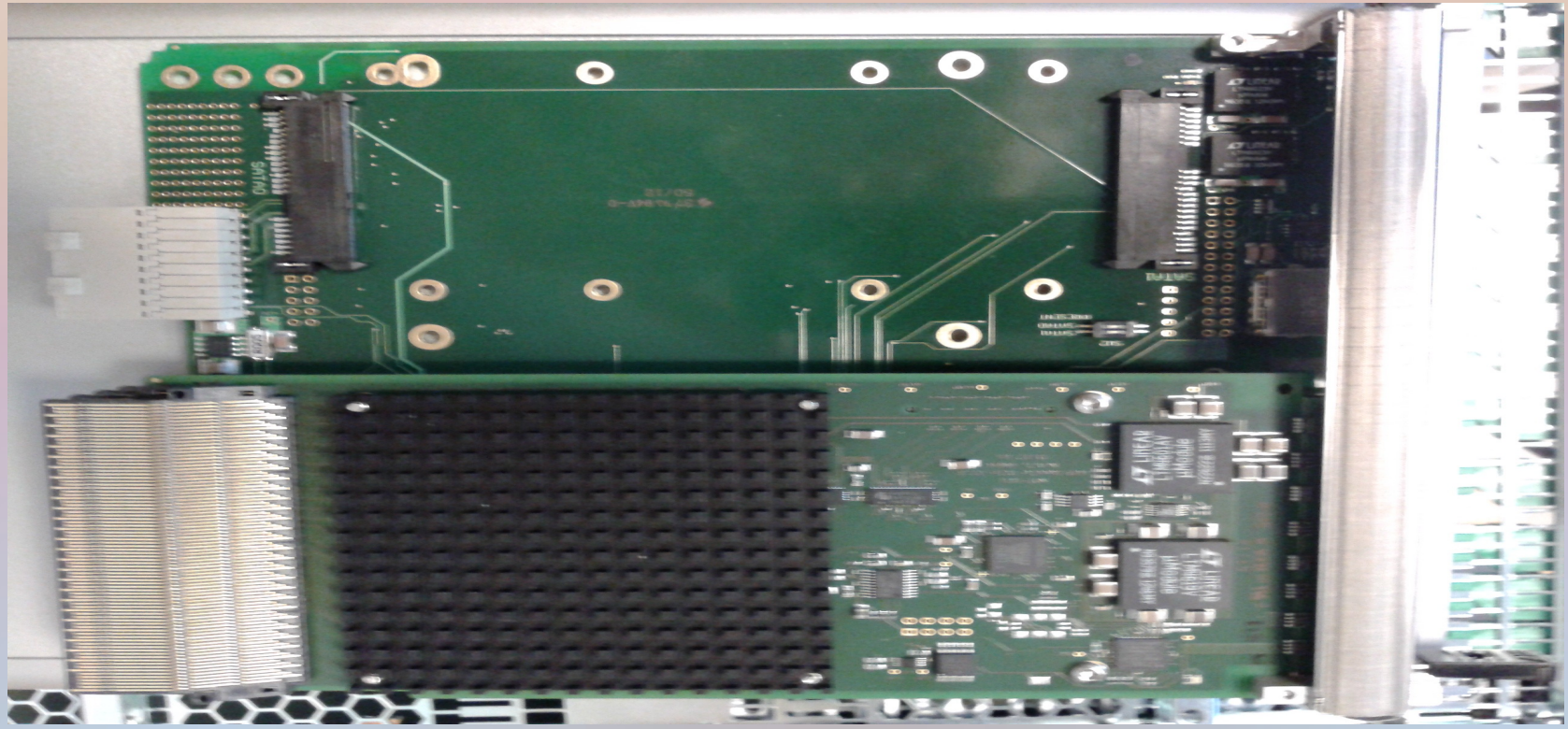


# SPECS V2 Crate

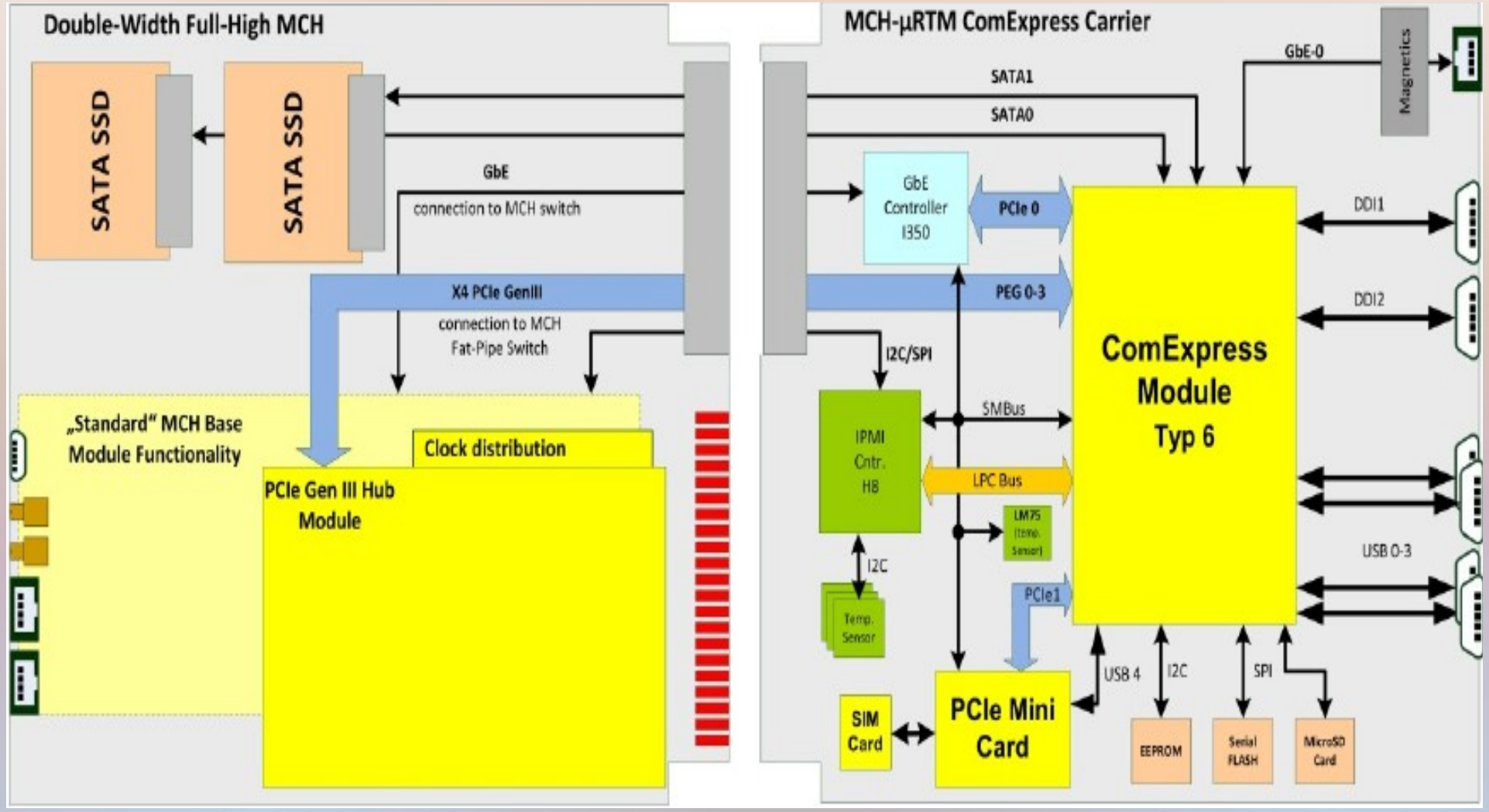


# NAT MCH

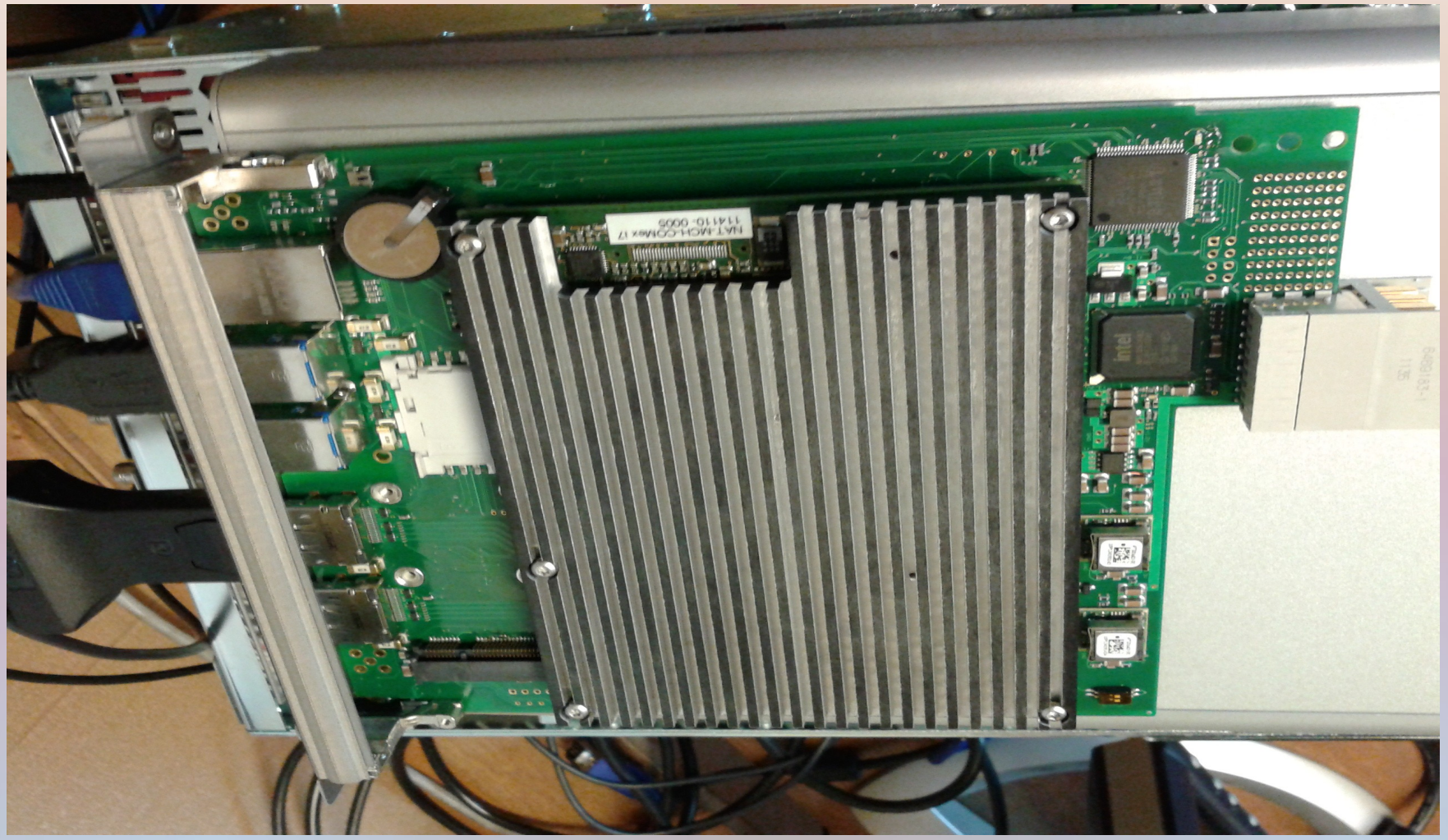

Maximum height
Prototype control board
24,56 mm
1,6 mm
Tongue 4
Tongue 3
Tongue 2
Tongue 1
24,46 mm
NAT mother board
63.38 mm



# MCH-CPU


Double-Width Full-High MCH
SATA SSD
SATA SSD
GbE
connection to MCH switch
X4 PCIe GenIII
connection to MCH
Fat-Pipe Switch
„Standard" MCH Base
Module Functionality
Clock distribution
PCIe Gen III Hub
Module
MCH-µRTM ComExpress Carrier
SATA1
SATA0
GbE-0
Magnetics
GbE
Controller
I350
PCIe 0
PEG 0-3
I2C/SPI
SMBus
IPMI
Cntr.
H8
LPC Bus
LM75
(temp.
Sensor)
I2C
Temp.
Sensor
PCIe1
ComExpress
Module
Typ 6
DDI1
DDI2
USB 0-3
USB 4
I2C
SPI
SIM
Card
PCIe Mini
Card
EEPROM
Serial
FLASH
MicroSD
Card

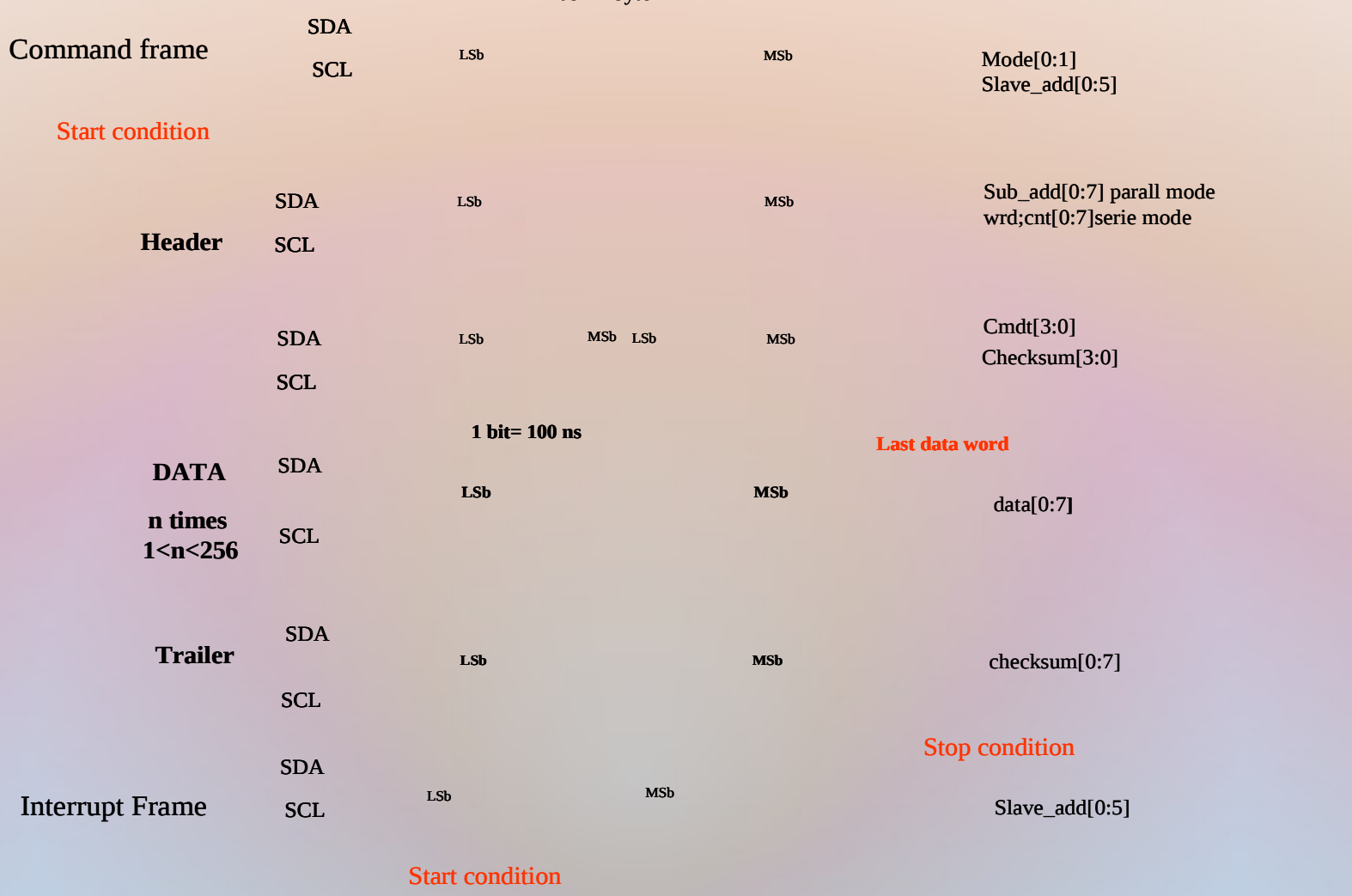
# NAT CPU



# Conclusion

- 21 cartes en production
- Mise en place sur cite courant Juillet
- Problèmes
  - Approvisionnement FPGA.
  - FPGAsysplanner (import export dans allegro)
  -

# SPECS Frame


1us = 1byte
Command frame
SDA
SCL
LSb
MSb
Mode[0:1]
Slave_add[0:5]
Start condition
Header
SDA
SCL
LSb
MSb
Sub_add[0:7] parall mode
wrd;cnt[0:7]serie mode
SDA
SCL
LSb
MSb
LSb
MSb
Cmdt[3:0]
Checksum[3:0]
1 bit= 100 ns
Last data word
DATA
n times
1<n<256
SDA
SCL
LSb
MSb
data[0:7]
Trailer
SDA
SCL
LSb
MSb
checksum[0:7]
Stop condition
Interrupt Frame
SDA
SCL
LSb
MSb
Slave_add[0:5]
Start condition