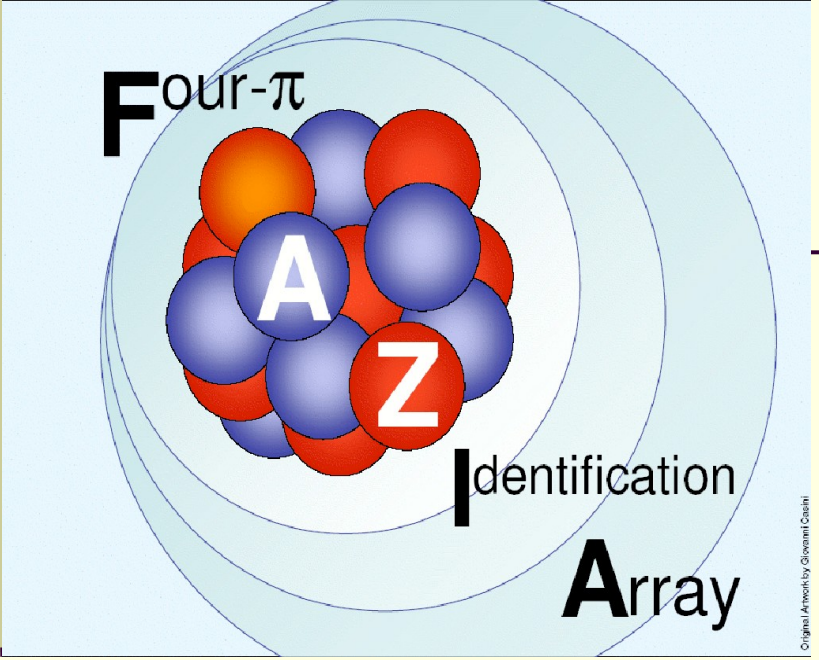
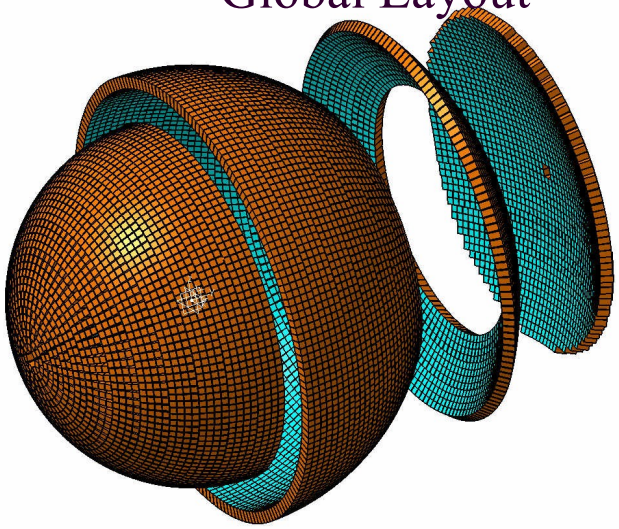


FAZIA

FRONT-END ELECTRONICS, TRIGGER AND ACQUISITION

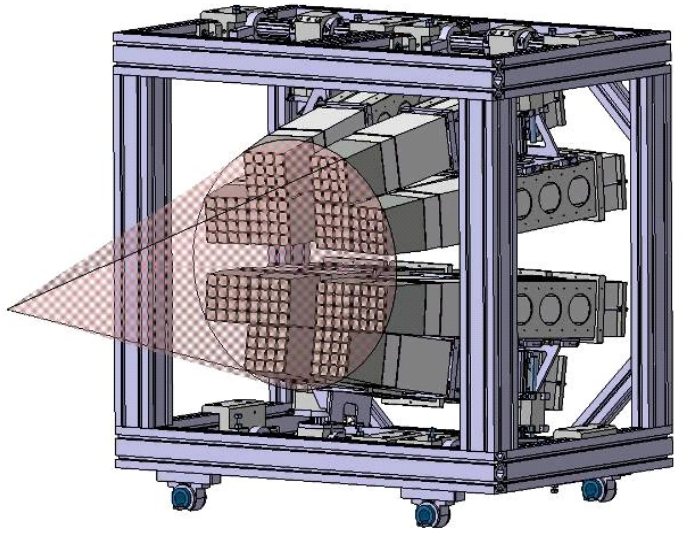
The FAZIA experiment

Global Layout



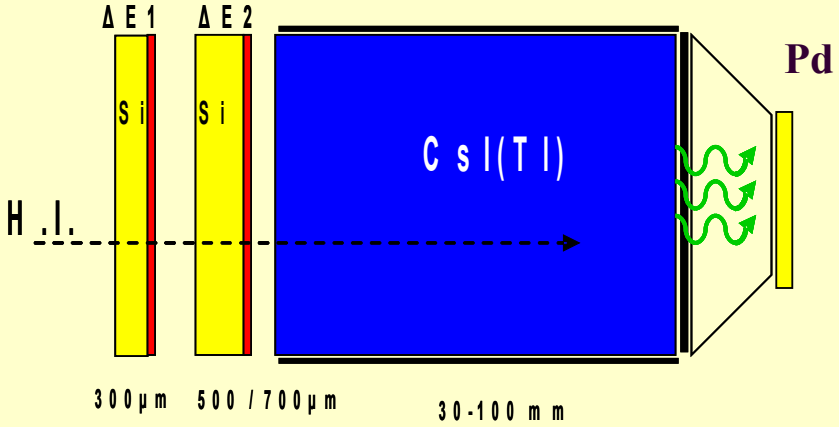
10k telescopes

Test prototype *"FAZIETTO"*

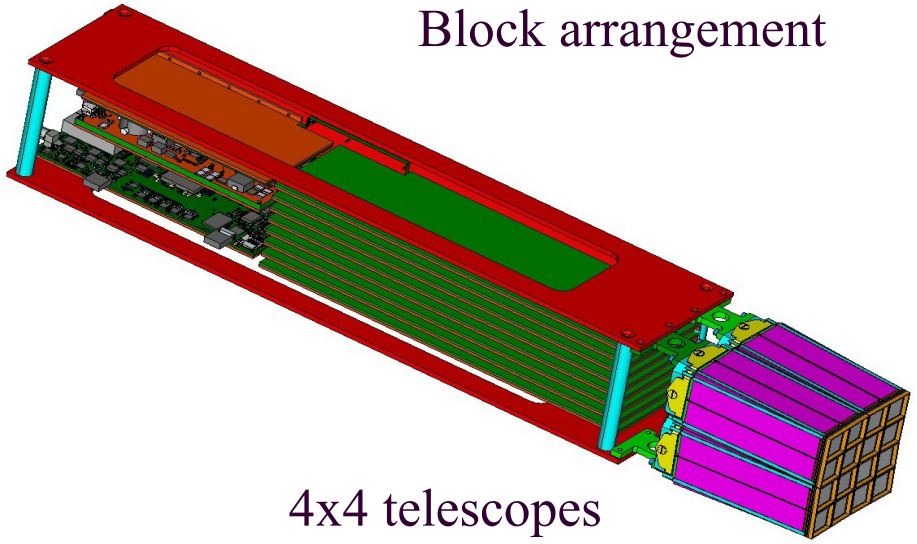


12 blocks - 192 telescopes

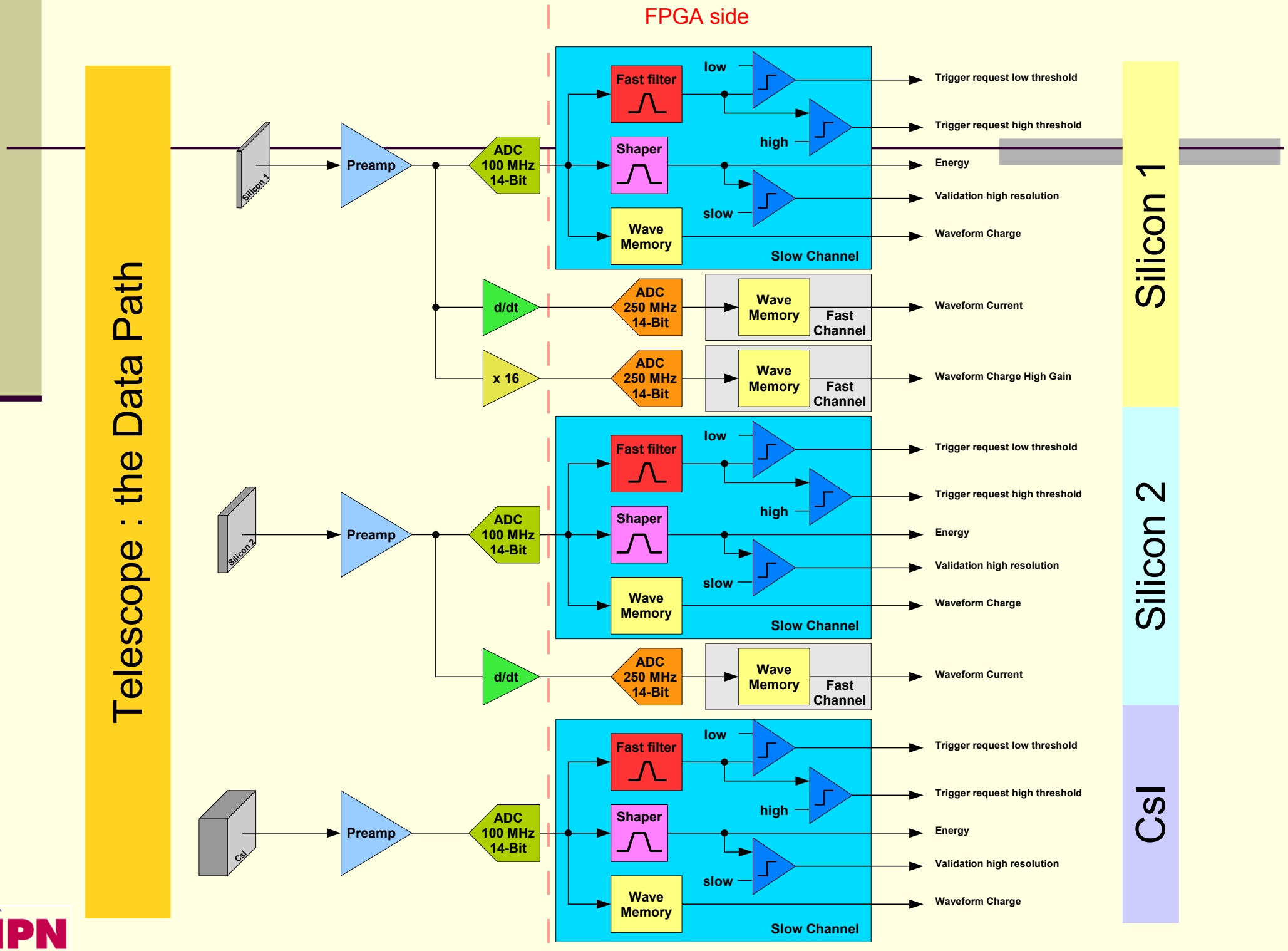
Telescope structure



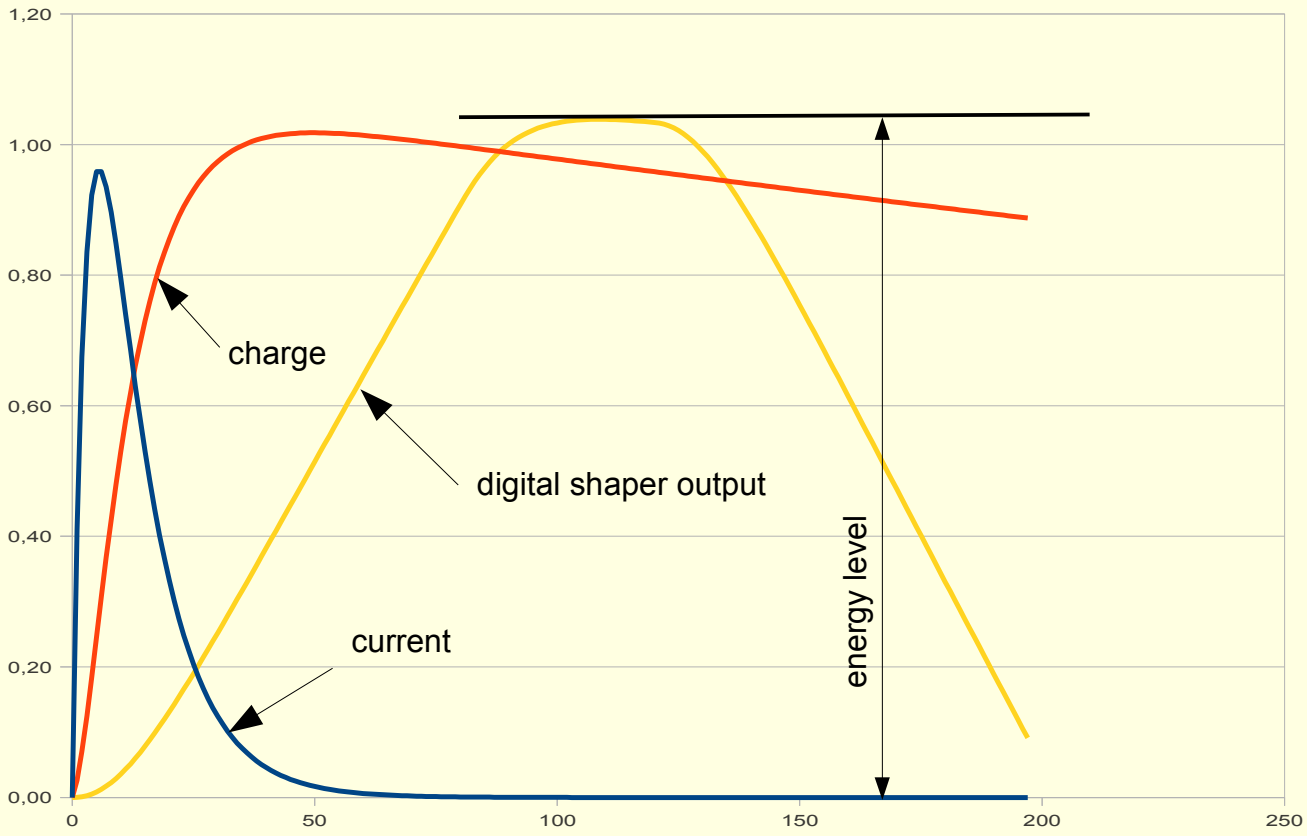
Block arrangement

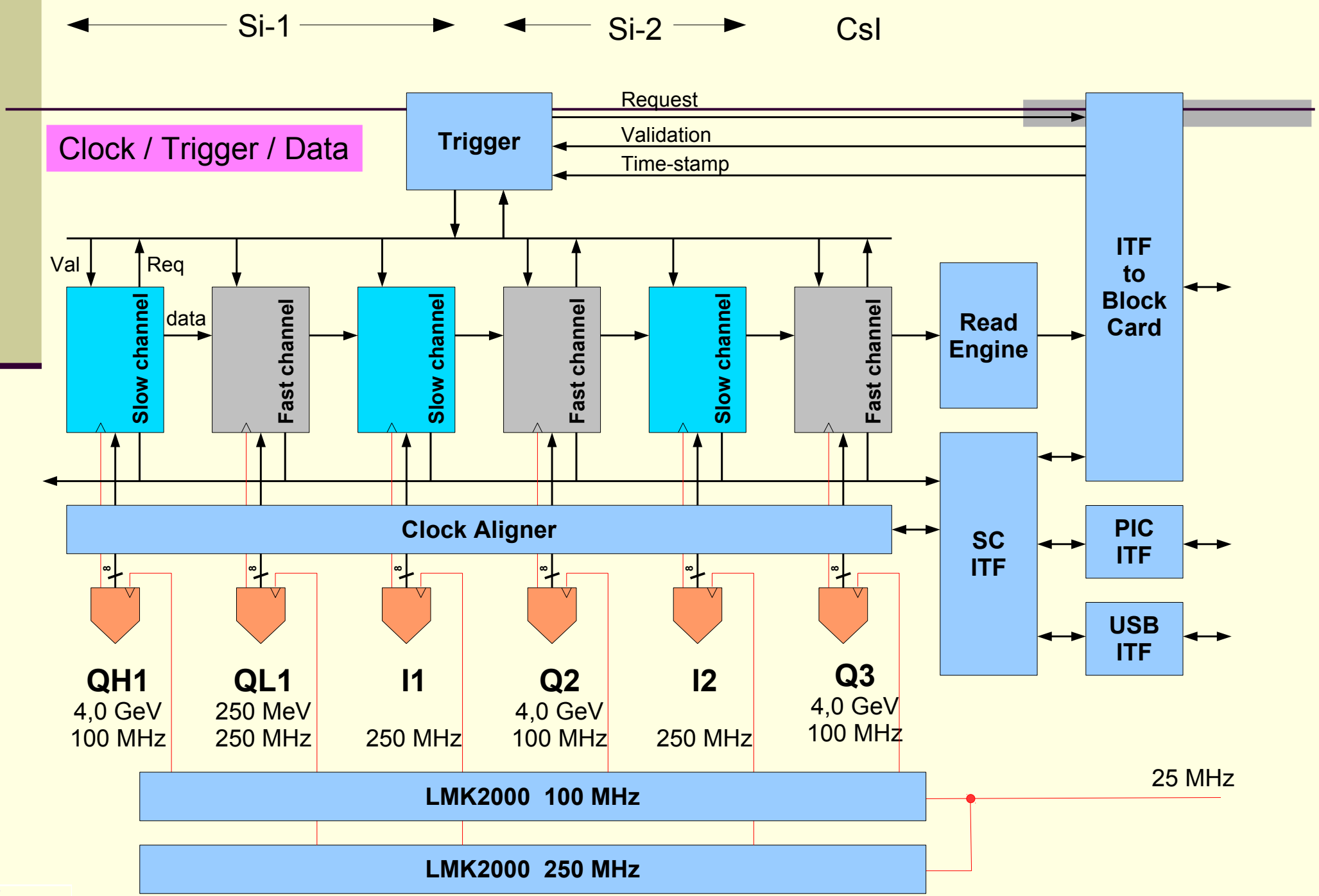


4x4 telescopes

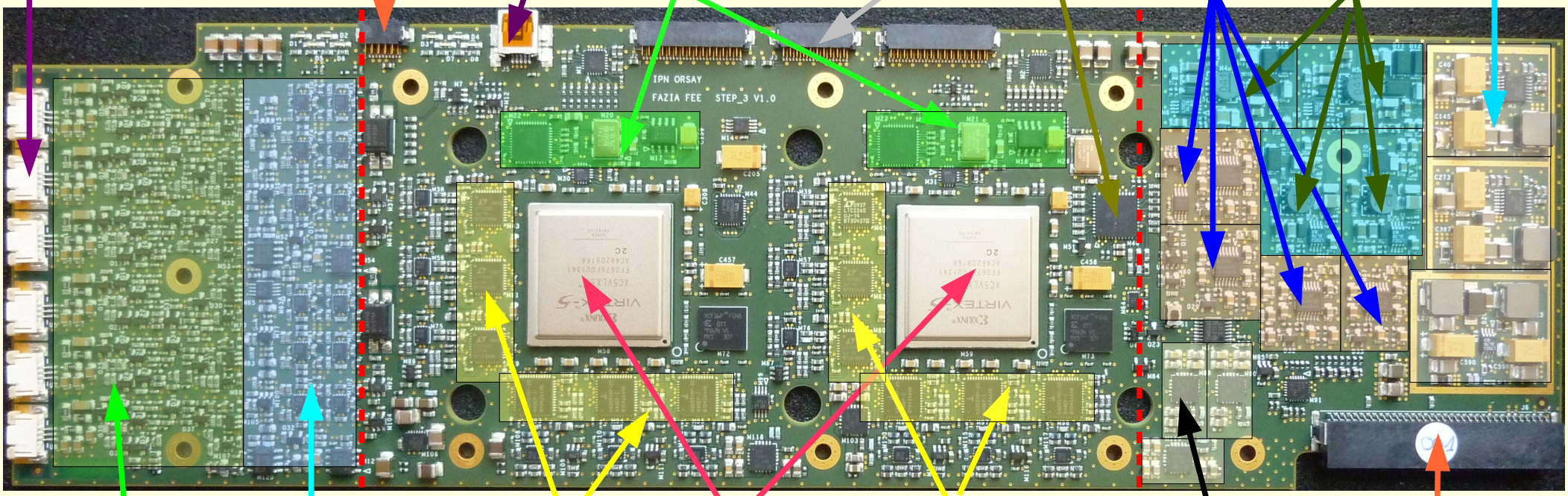

FPGA side
Telescope : the Data Path
Silicon 1
Preamp
ADC
100 MHz
14-Bit
Fast filter
Shaper
Wave
Memory
low
high
slow
Slow Channel
Trigger request low threshold
Trigger request high threshold
Energy
Validation high resolution
Waveform Charge
d/dt
x 16
ADC
250 MHz
14-Bit
Wave
Memory
Fast
Channel
Waveform Current
Waveform Charge High Gain
Silicon 2
CsI
Silicon 1
Silicon 2
CsI

Current, Charge and Energy Signals



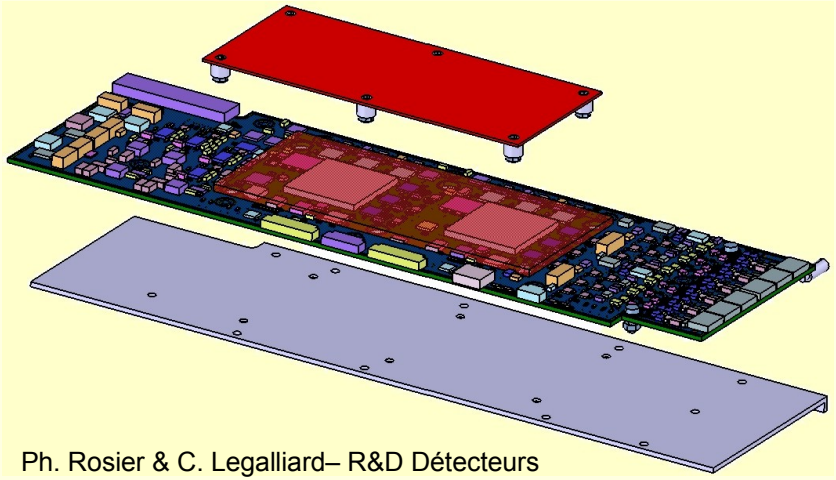

Si-1
Si-2
CsI
Clock / Trigger / Data
Trigger
Request
Validation
Time-stamp
ITF to Block Card
Val
Req
data
Slow channel
Fast channel
Slow channel
Fast channel
Slow channel
Fast channel
Read Engine
Clock Aligner
SC ITF
PIC ITF
USB ITF
8
QH1
4,0 GeV
100 MHz
QL1
250 MeV
250 MHz
I1
250 MHz
Q2
4,0 GeV
100 MHz
I2
250 MHz
Q3
4,0 GeV
100 MHz
LMK2000 100 MHz
LMK2000 250 MHz
25 MHz

FEE card overview

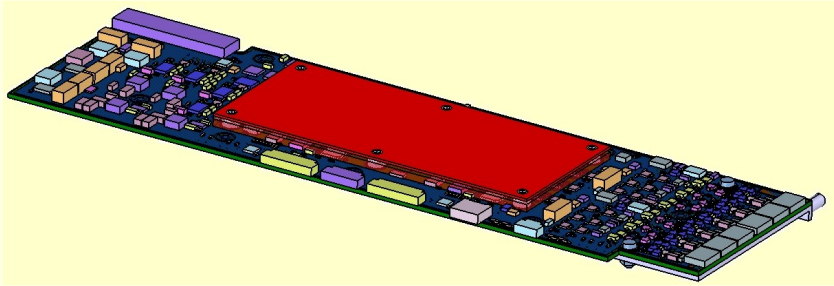


Dimensions : 300 mm x 88 mm

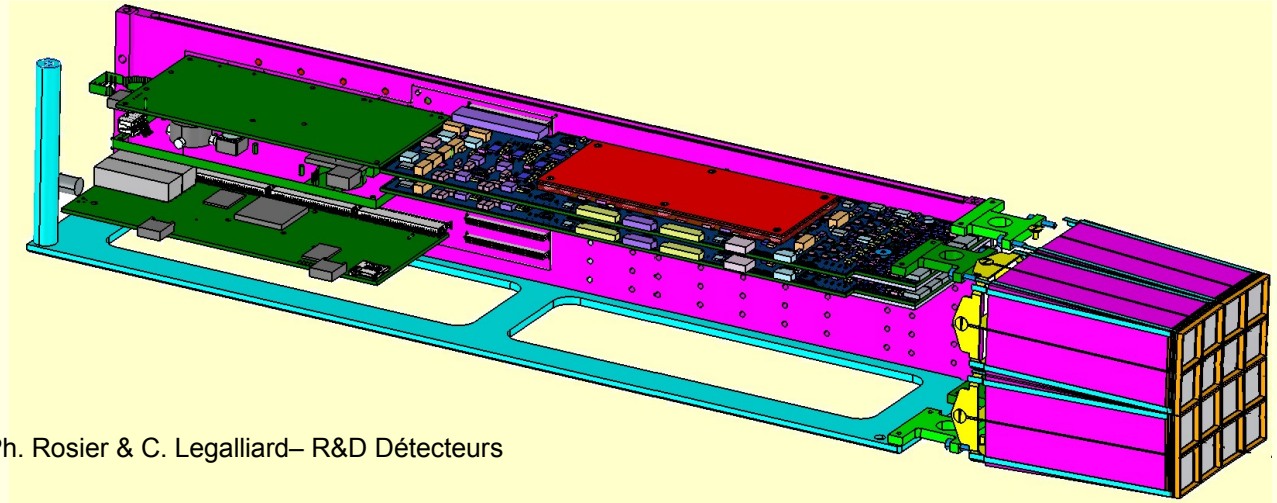
Heat dissipation in a vacuum chamber



Ph. Rosier & C. Legalliard– R&D Détecteurs

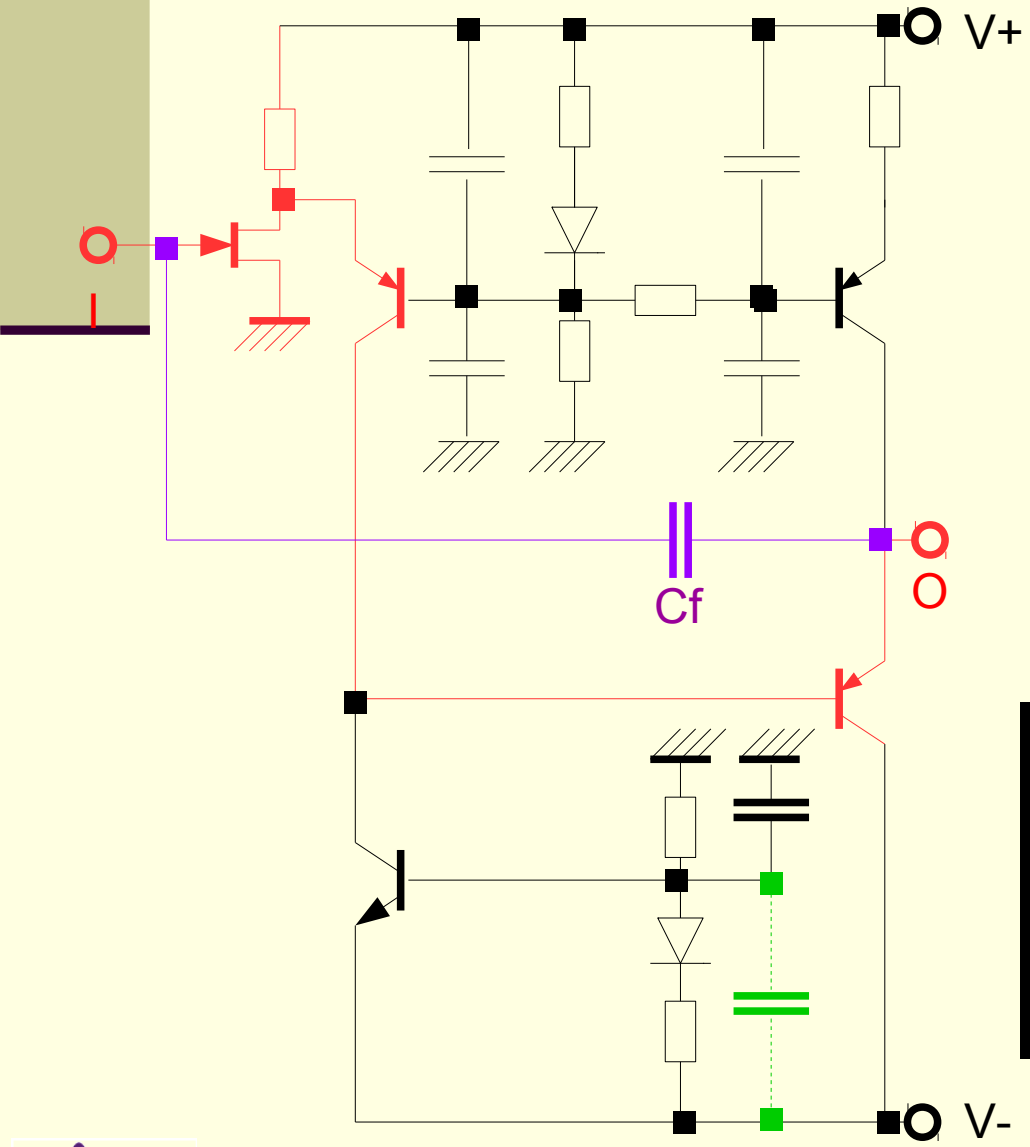


Ph. Rosier & C. Legalliard– R&D Détecteurs

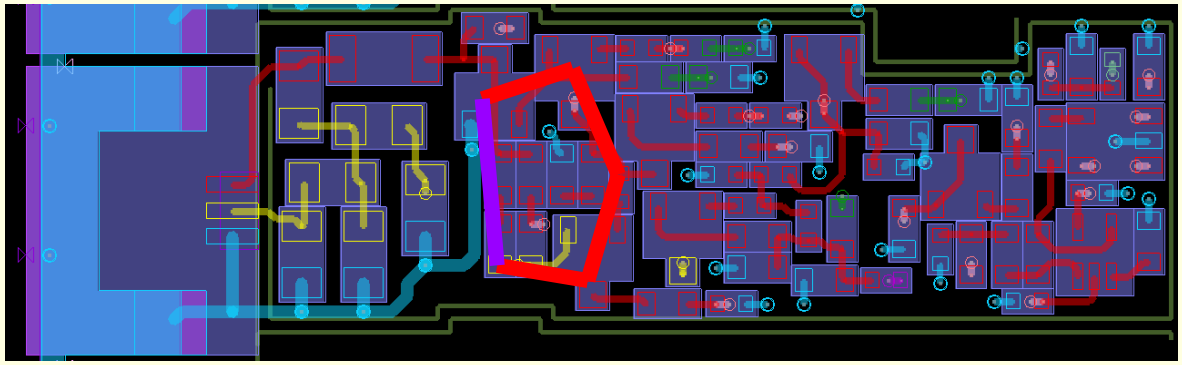


Ph. Rosier & C. Legalliard– R&D Détecteurs

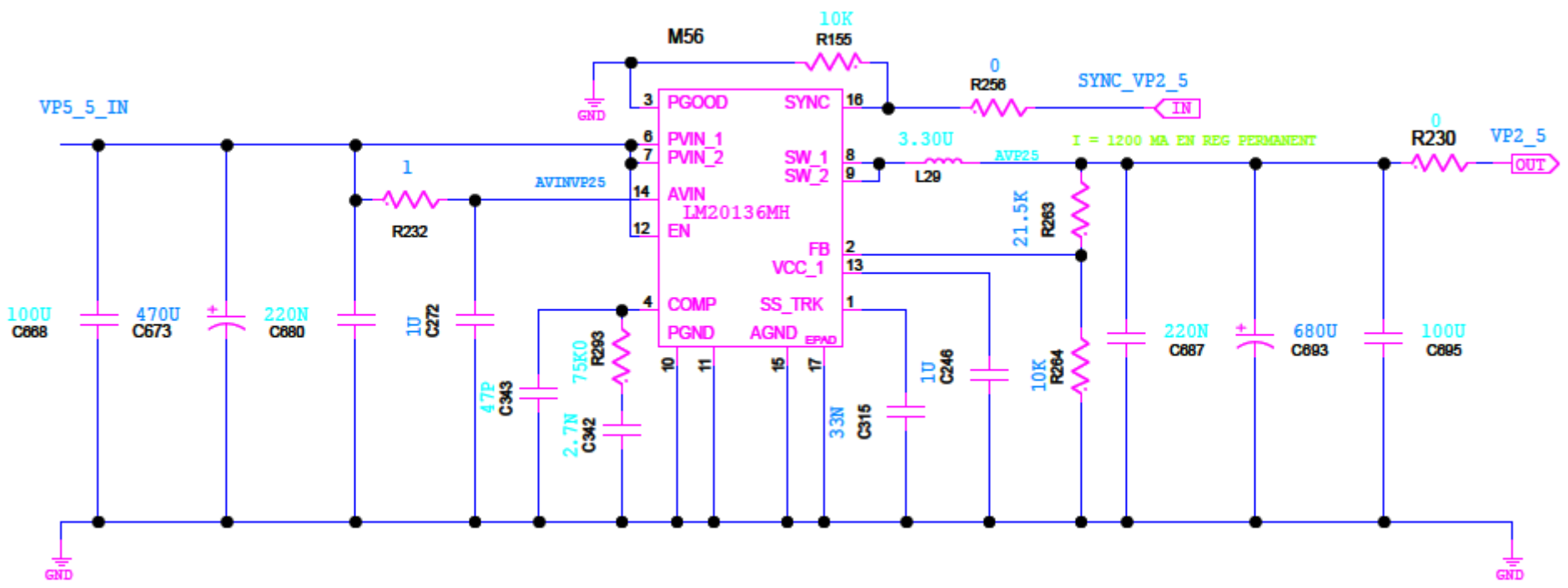
Routing design of the preamplifier

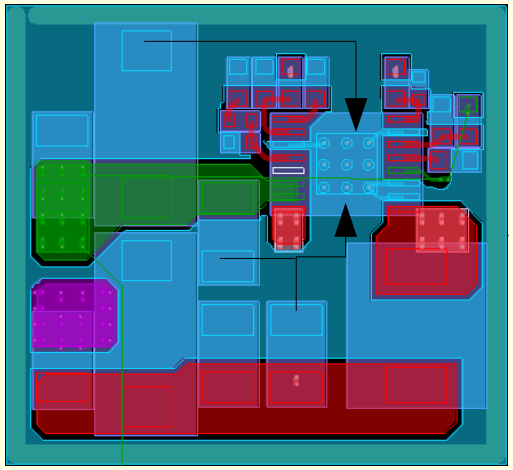


- The amplification part coloured in red and the feedback part coloured in purple are routed on the surface
- These two parts are located near the 3-pin connector
- The source of the JFET transistor is directly connected to the ground of the connector

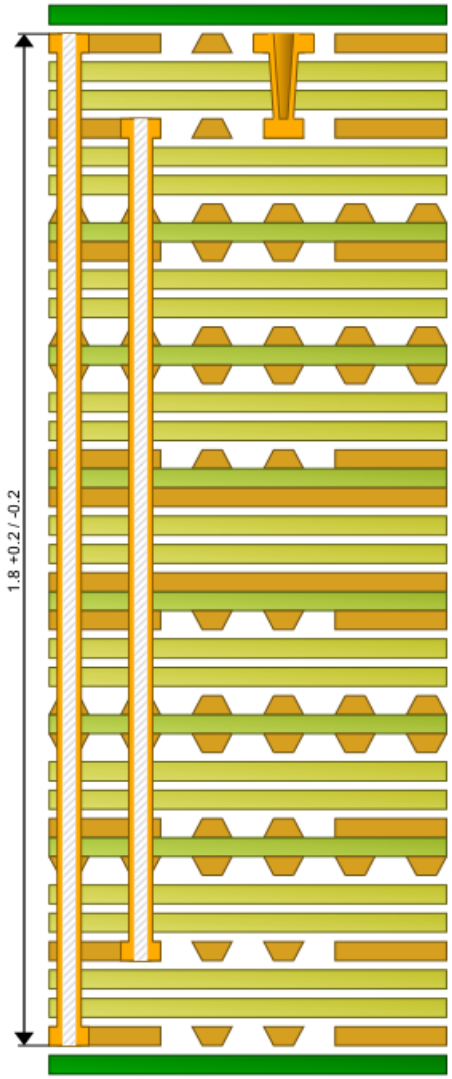


Rooting design of a SW regulator





Stackup



	Soldermask		0.020	4.100		SolderMask	0
1	Foil	0.035				Foil	0
	VT47-106	0.048		4.000		PREPREG	
	VT47-106	0.048		4.000		PREPREG	
2	Foil	0.035				Foil	0
	VT47-106	0.053		4.000		PREPREG	
	VT47-106	0.053		4.000		PREPREG	
3		0.018			1, 2		
	VT-47	0.102		4.120		Core	
4		0.018					
	VT47-1080	0.075		4.000		PREPREG	
	VT47-106	0.053		4.100		PREPREG	
5		0.018			3, 4		
	VT-47	0.102		4.120		Core	
6		0.018			5, 6		
	VT47-106	0.053		4.100		PREPREG	
	VT47-1080	0.075		4.000		PREPREG	
7		0.018					
	VT-47	0.102		4.120		Core	
8		0.018					
	VT47-106	0.053		4.000		PREPREG	
	VT47-106	0.053		4.000		PREPREG	
9		0.018					
	VT-47	0.102		4.120		Core	
10		0.018					
	VT47-1080	0.075		4.000		PREPREG	
	VT47-106	0.053		4.100		PREPREG	
11		0.018			7, 8		
	VT-47	0.102		4.120		Core	
12		0.018			9, 10		
	VT47-106	0.053		4.100		PREPREG	
	VT47-1080	0.075		4.000		PREPREG	
13		0.018					
	VT-47	0.102		4.120		Core	
14		0.018			11, 12		
	VT47-106	0.053		4.000		PREPREG	
	VT47-106	0.053		4.000		PREPREG	
15	Foil	0.035			13, 14	Foil	0
	VT47-106	0.048		4.000		PREPREG	
	VT47-106	0.048		4.000		PREPREG	
16	Foil	0.035				Foil	0
	Soldermask		0.020	4.100		SolderMask	0

Copper Thickness = 0.353 | Dielectric Thickness = 1.631 | Solder Mask Thickness = 0.040 | Stack Up Thickness = 1.985 | Stack Up Thickness with Solder Mask = 2.025 |

Technical characteristics

- Power supply : 28 W
- Preamplifiers :
  - Rise time : ~ 10 ns
  - Output dynamical range : 8V (for 4 GeV)
- High voltage module
  - Current resolution : 0,1 nA
  - Current noise measurement : 3 nA RMS
  - Current range going through the detector : 10 nA to 2 µA
  - Voltage resolution : 3mV (200V) , 6mV (400V)
- FPGA : Communication SERDES @ 400 Mbits/s : OK

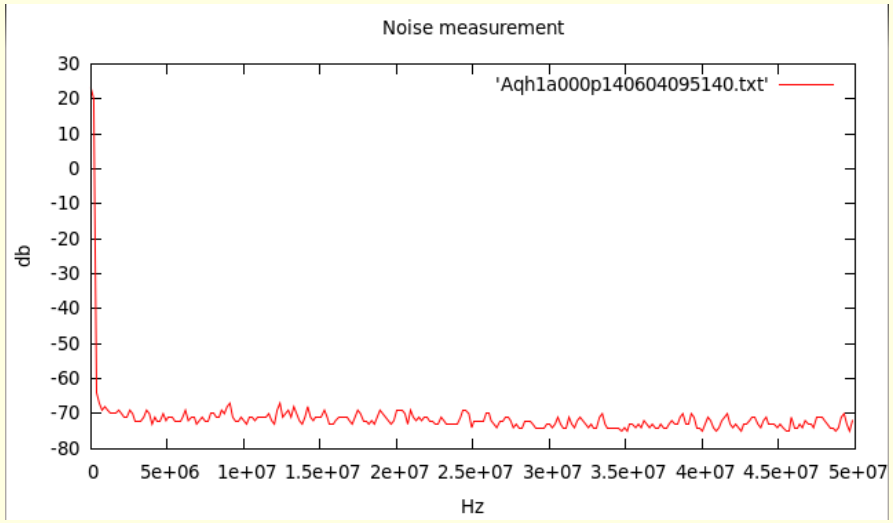
Test results

- Noise measurement on the signal baseline without detector

HV device OFF

Stdev : 1,60 mV or 0,8 MeV

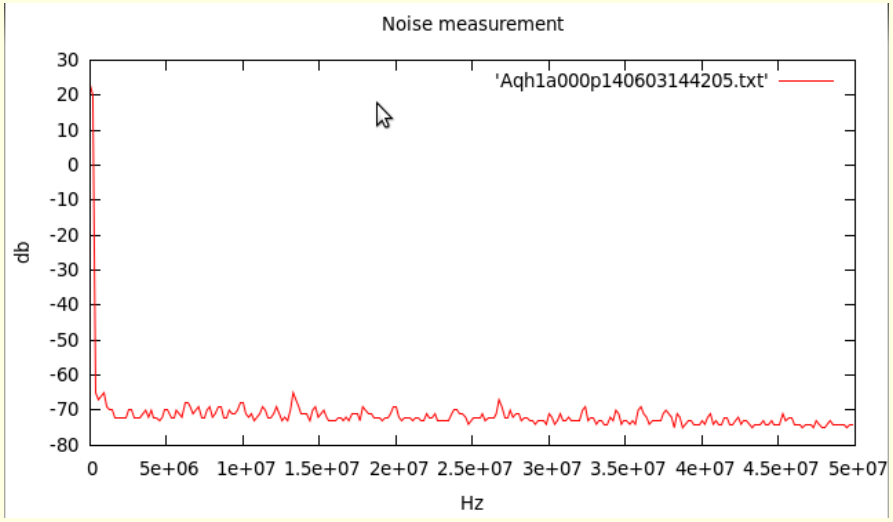
Frequency domain of the noise



@ 140 V

StdeV : 7,58 mV or 3,79 MeV

Frequency domain of the noise



Noise expressed in dB (= $10*\log(V^2/Hz)$)