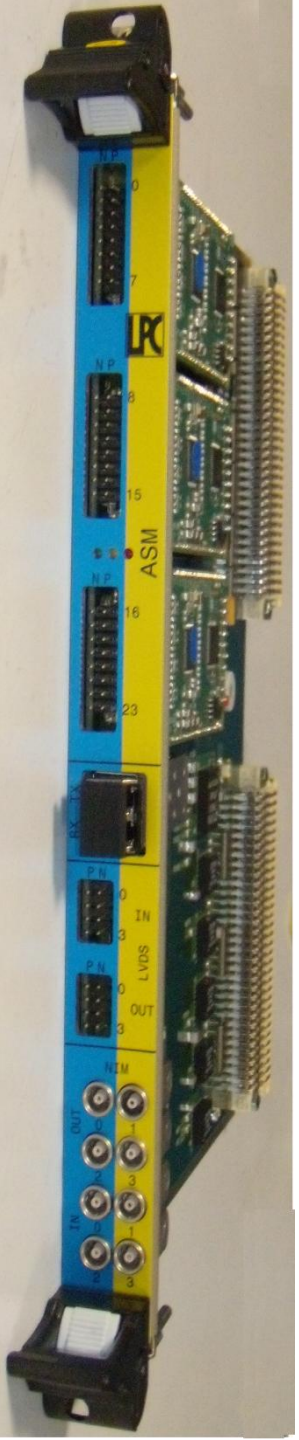


# Carte d'échantillonnage pour une application TEP en hadronthérapie

**Journées VLSI - FPGA - PCB de l'IN2P3**

mercredi 11 juin 2014

**CPPM**

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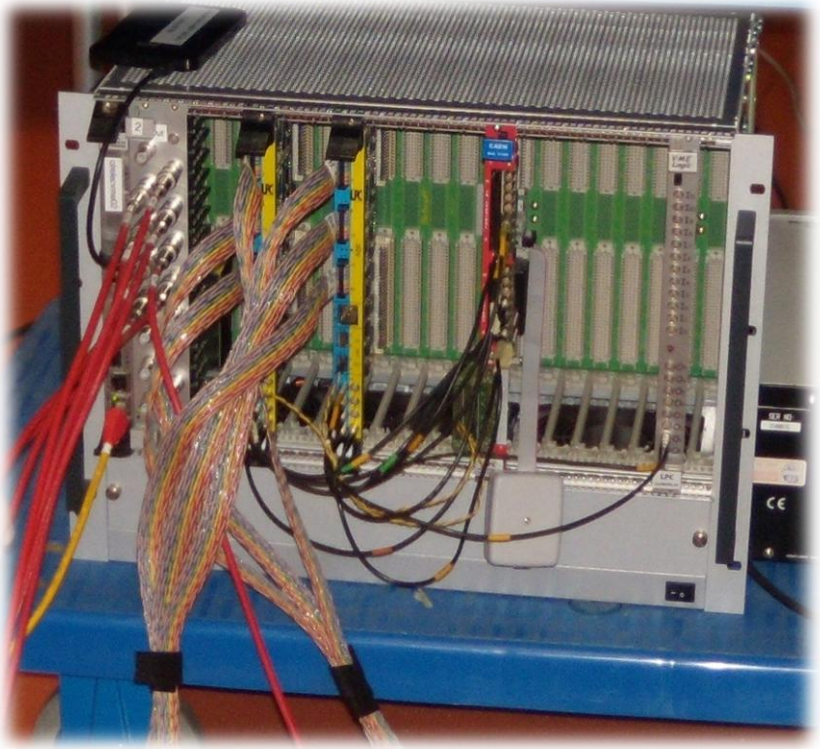
# Outlines

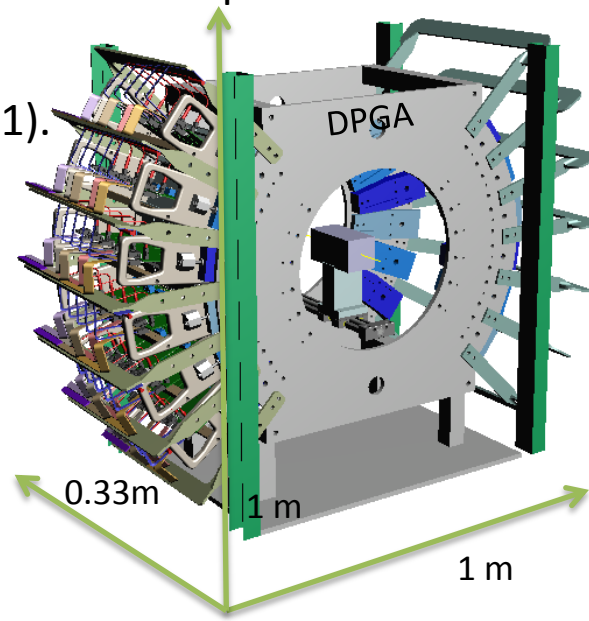
- Context
- ASM technical functionality
- Return of experiment
- Conclusion & Perspectives



Experiment system


# Context

- This board is a requirement of the team AVIRM of my Lab for the Project DPGA ( Pixelized detector with a large acceptance)
- Have news sampling boards with higher performances than the ARS16 boards developed at the Laboratory and based on ARS0 chip.
- Electronic development begin in September 2011).
- Detector with 240 PMT sensors
- The goal is to have a good timing resolution with a fast sampling frequency.
- The choice of the DRS4 is the good compromise between sampling frequency, acquisition windows and dead time.

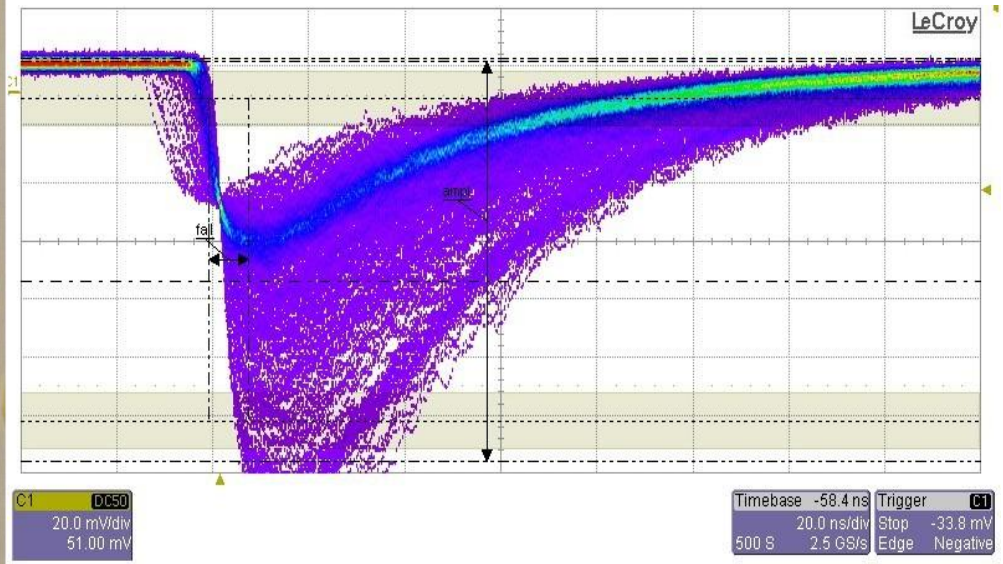



# Requirements

- <u>Signal to be acquire by the board:</u>

The picture below is a capture of the anode signal of the PMT (HR+ PET system).

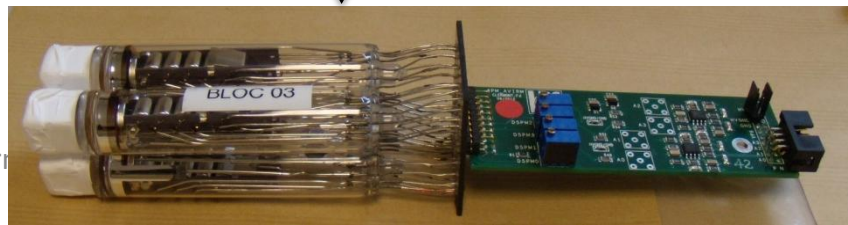
The HV divider circuit include a differential amplifier with a gain 2 to the board.




Width : 200 ns
Amplitude : 0 to 200 mV
Rise time : 8 ns

4 PMT sensors & HV divider circuit

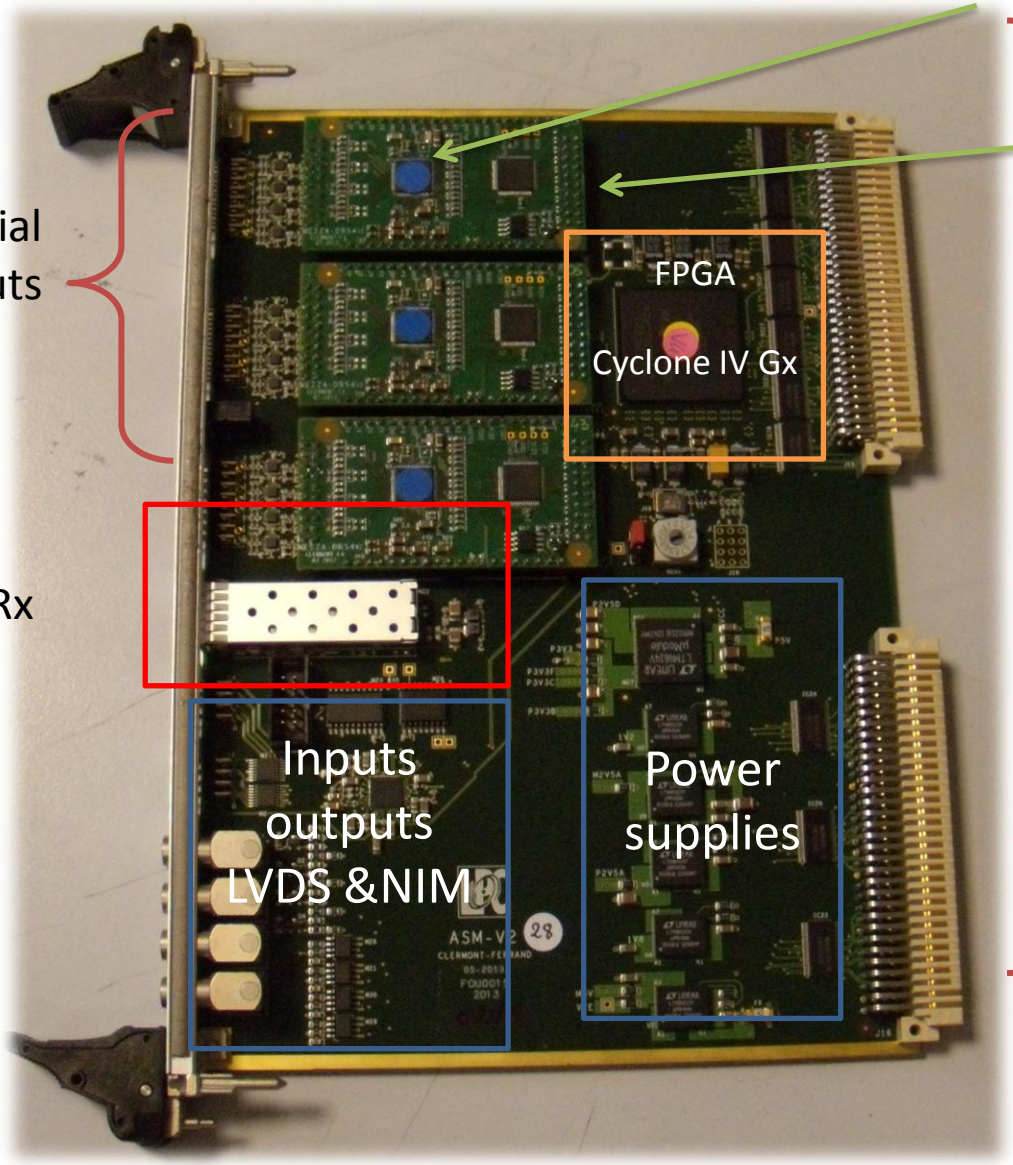
Scintillators crystals




# ASM

- ASM for “Analog Sampling Module”
- **G**eneric electronic board
- 24 differentials analog inputs (600mV amplitude)
- VME 6U board format (compatible VME 64x)
- Scalable system
- Functions:
  - sampling data at up to 6 GHz on a windows up to 1000 samples.
  - Generate an own trigger detection by channel and by board.
- Data acquisition used VME BLT protocol

# ASM specifications




3 Sampling & digitizing mezzanines

under mezzanines
Analog trigger generation part

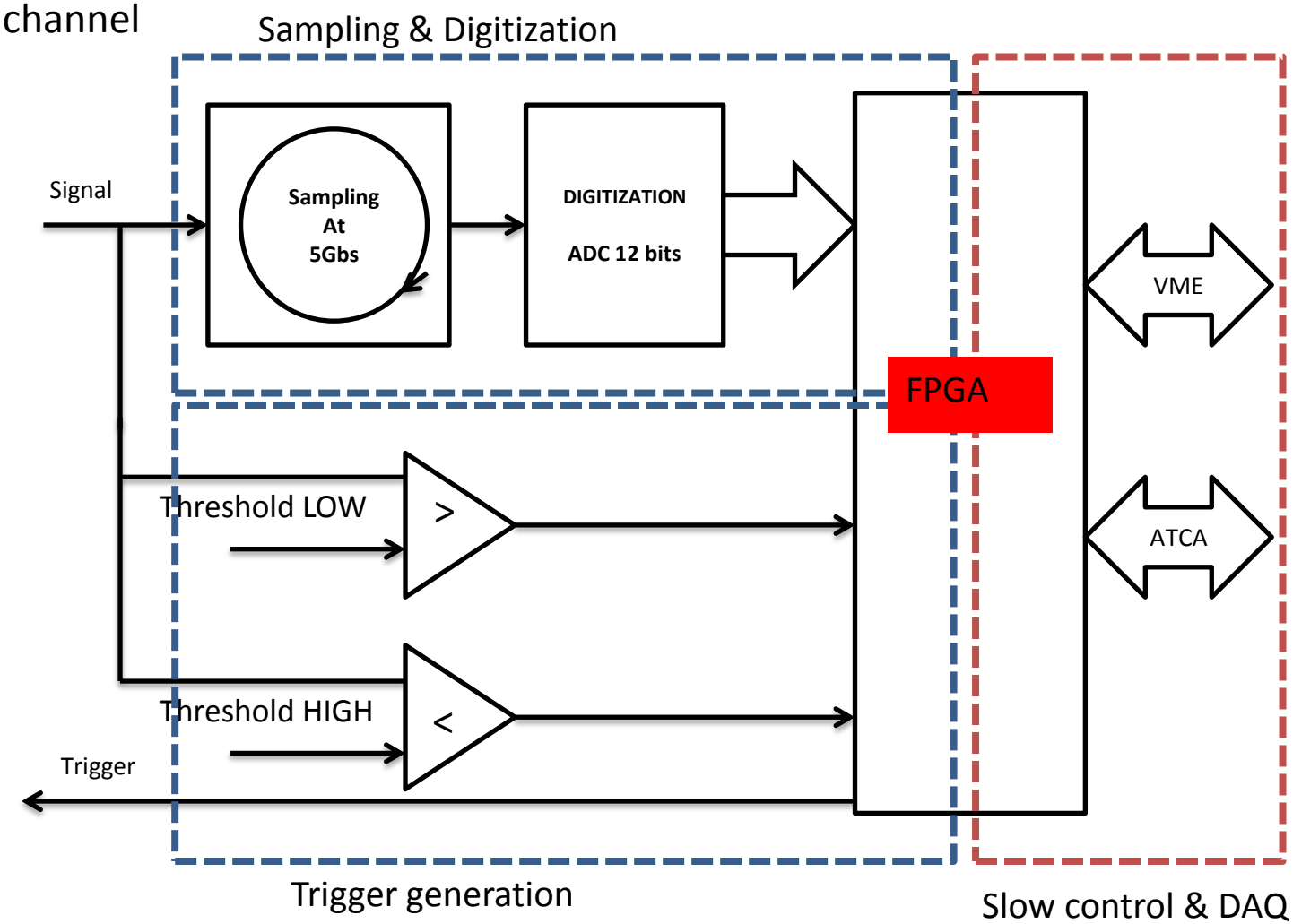
24 differential analog inputs

Connectors to VME Backplane

Optical Tx/ Rx 3.65 Gbs

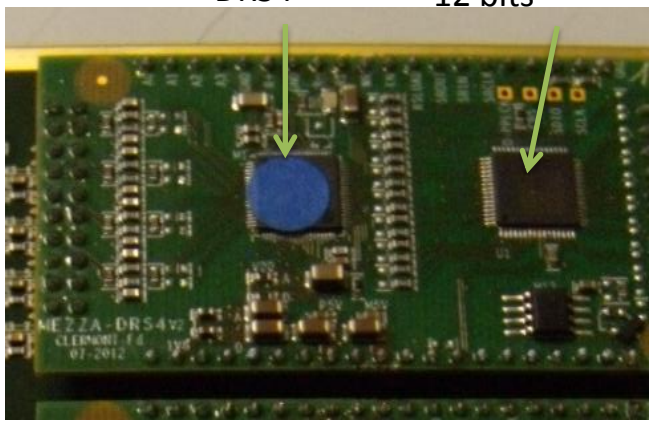

# Board functional diagram

1/24 channel



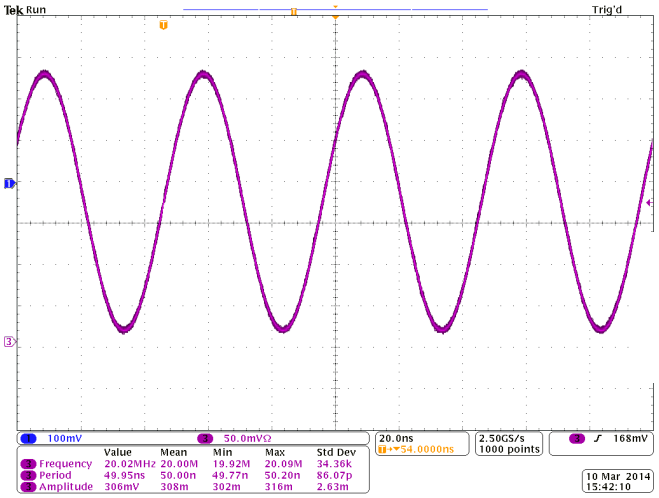

# Sampling & digitization

- Used DRS4 chips coupled with an ADC 12 bits
- By configuring VME register: one determines :
  - Buffer size 10 to 1000 samples
  - Sampling frequency ( for stand alone work)
  - Select internal sampling frequency or external LVDS clock for multiple boards used
  - Each mezzanine can be individually configured.




Sampling & digitizing mezzanine

Signal view by oscilloscope



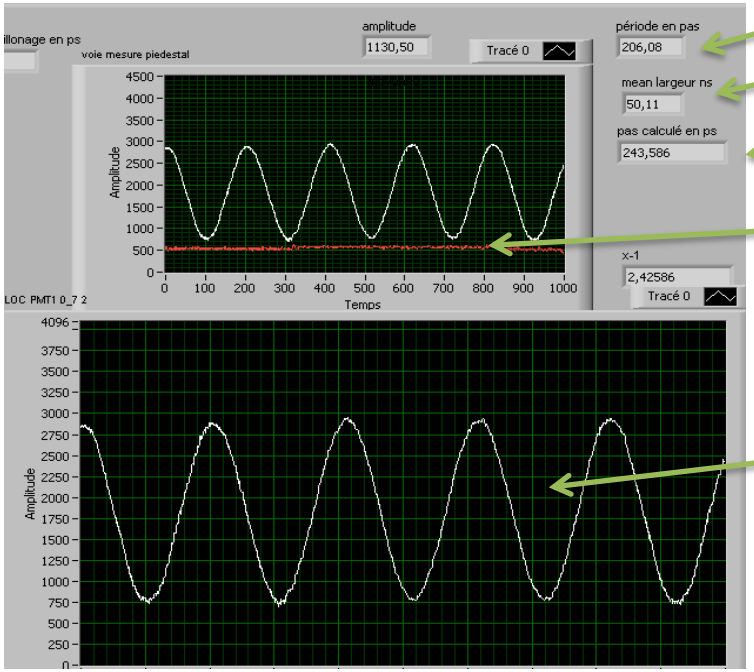

| | Value | Mean | Min | Max | Std Dev |
|---|---|---|---|---|---|
| 3 Frequency | 20.02MHz | 20.00M | 19.92M | 20.09M | 34.36k |
| 3 Period | 49.95ns | 50.00n | 49.77n | 50.20n | 86.07p |
| 3 Amplitude | 306mV | 308m | 302m | 316m | 2.63m |

Input signal :

sinusoidal signal : 50ns period

Amplitude 300mV single ended

Same signal view by ASM test bench acquisition& triggered by channel 0




Calculate period in step (206.08)

Equivalent period in ns (50.11 ns)

Calculated step value (243.5 ps)

View of channel 0 & 1

View of channel 0

Subtract to channel 1

Pedestal pattern

Result :

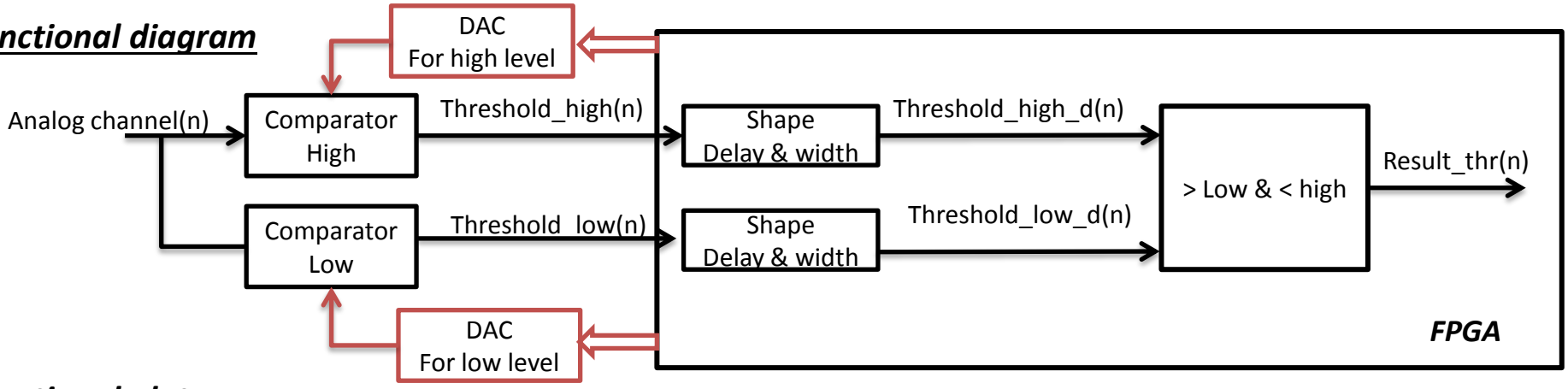
Amplitude 120 µV / ADC step

1269 *(120µV *2) =304 mV

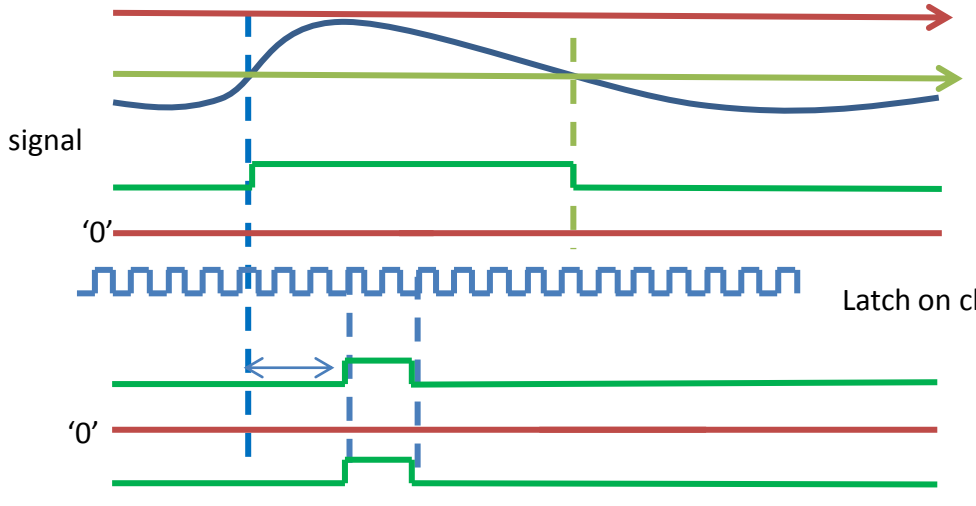
# Thresholds detection to trigger signal

## First step : individual trigger generation

***Functional diagram***




***Functional plot***




High threshold level
Low threshold level
Analog inputs

Low threshold signal
High threshold signal
After comparator

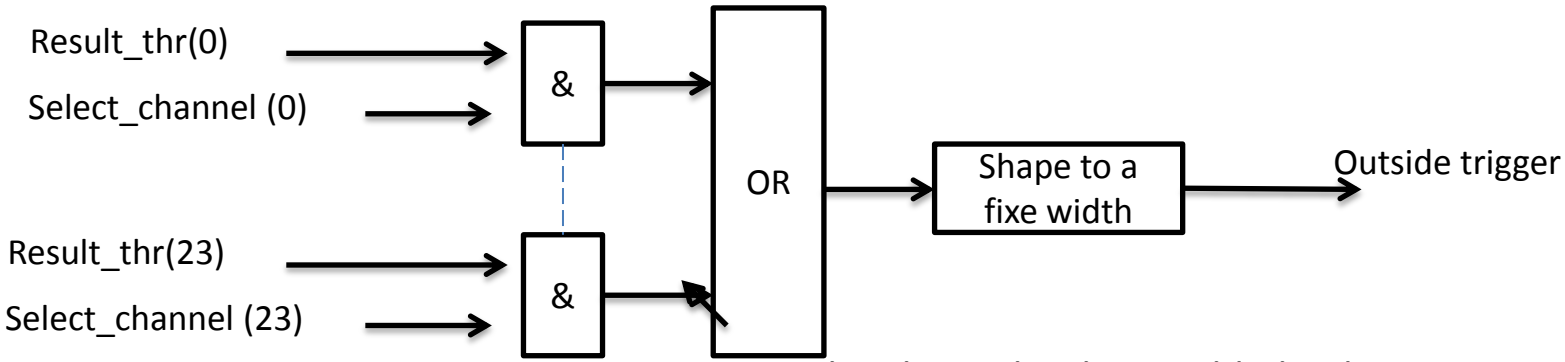
Latch on clock and added numeric delays by steps of 4.16 ns

Threshold_low_d(n)
Threshold_high_d(n)
Result_thr(n)
After shaping


# Thresholds detection to trigger signal

## Second step: board trigger generation

- Each channel can be select to be in the board trigger




This shaper has been added to be sure to have the right signal to stop the sampling

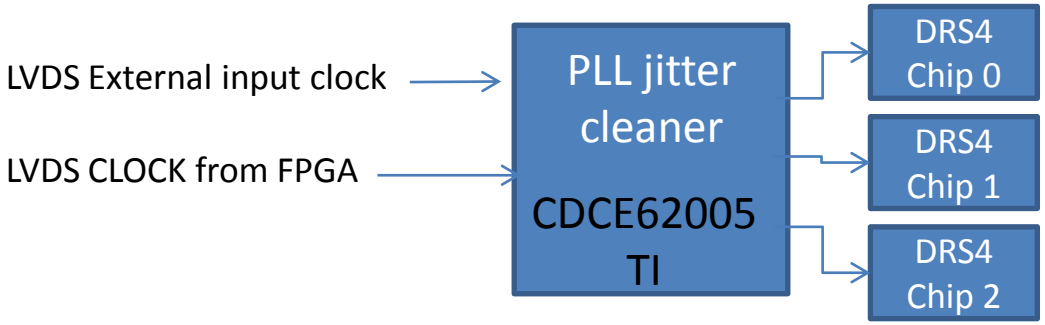
This signal go outside the board to permit make an external logic.
Coincidences of others trigger boards

And permit to include BUSY of each board in equation to have less problem with the DAQ
when we use more than one board.

# Sampling Clock network

- The PLL jitter cleaner permit to select on 2 inputs clock and generate 3 clocks for the 3 DRS4 chips.

*Functional sampling clock network*




- The PLL jitter cleaner ensure the low jitter between the 3 chips.
- The tracks on the PCB have been carefully studies .

---

Sampling step : 244ps

**PRELIMINARY Results**

**more measures must be done**

<u>Measure jitter on a same chip:</u>

Result : 0,8 to 1,93 sampling step.

<u>Measures jitter between 2 channels in 2 chips in same ASM board</u>

Result : 1.5 to 3.2 sampling steps on the first board

1.4 to 1.5 sampling steps on the second board


# Data acquisition

At the output of the ADC the data are put 2 by 2 channels in a FIFO(24 bits width).
( to be compatible with 32 bits VME bus).

For the first step of the acquisition data we used VME BLT protocol :

The acquisition time is function of numbers of channel read, numbers of samples by channel and digitization time .

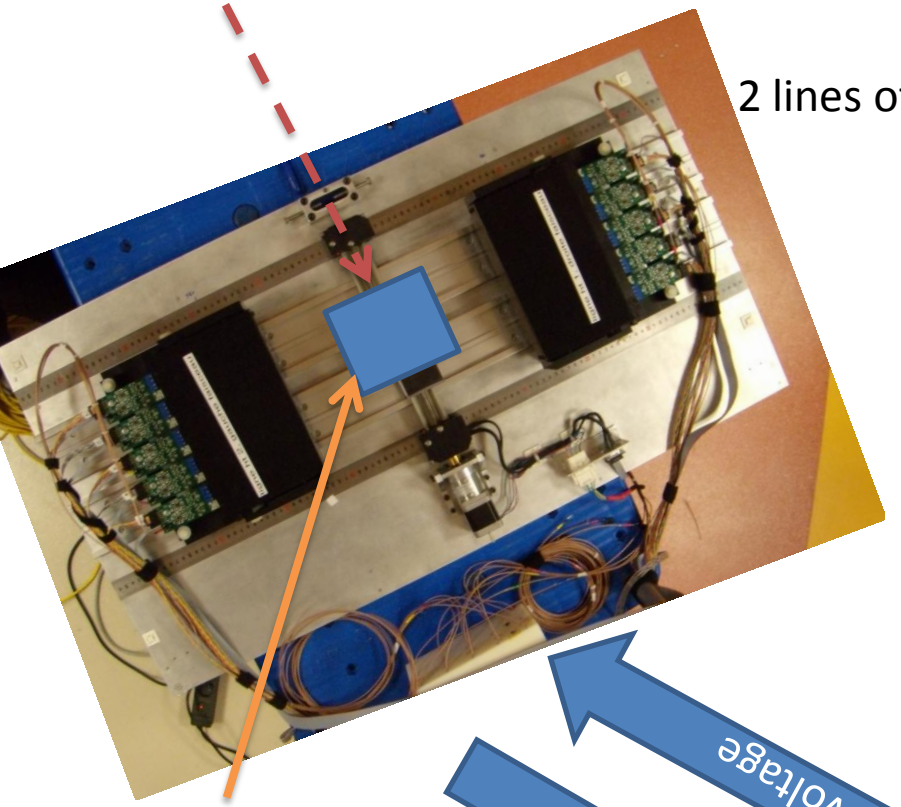
- ***DATA VME OUTPUTS : ( available solution)***
- Worst case : If you read 24 channels with 1000 samples each :
- **818 HZ Max** readout frequency ➔ Result in experiment **500 Hz** by board
  ( to be divide if the number of board is increase)

- ***Next STEP : optical link***
- The next step is to used the optical link : for the same example we hope a max readout of **6 KHz by board**

# Test beam setup: January 2014

Centre de protonthérapie d'Orsay

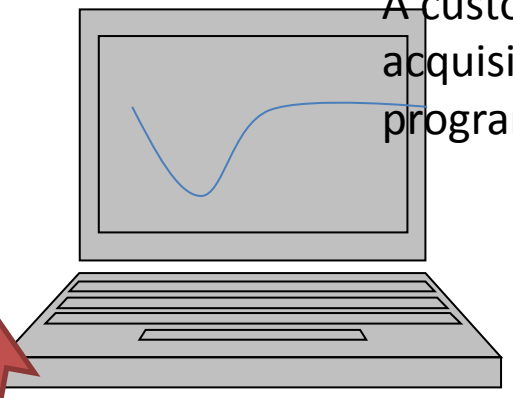
Beam



2 lines of 20 PMT each

PMMA target

A custom acquisition program



**Compact acquisition system**

VME CPU

2 High Voltage boards

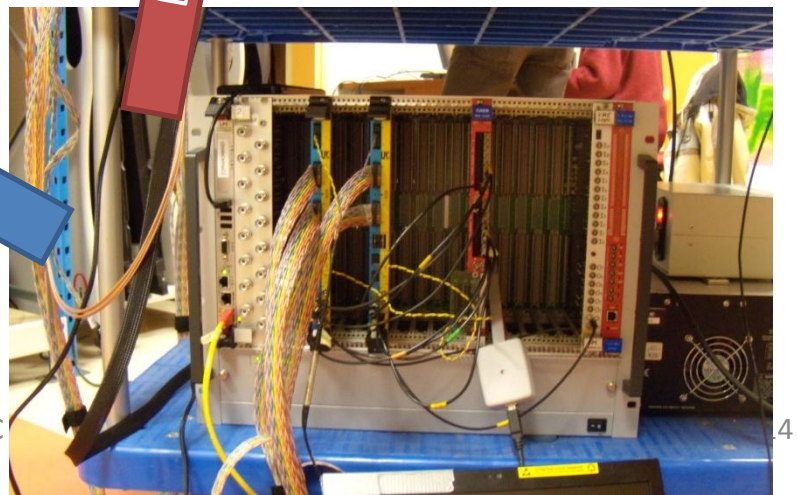
2 ASM boards

1 VME logic board(CAEN V1495)

Ethernet Link

High voltage

data




# Conclusion & Perspectives

- **<u>Conclusion</u>**

- This board has begin to give his performances

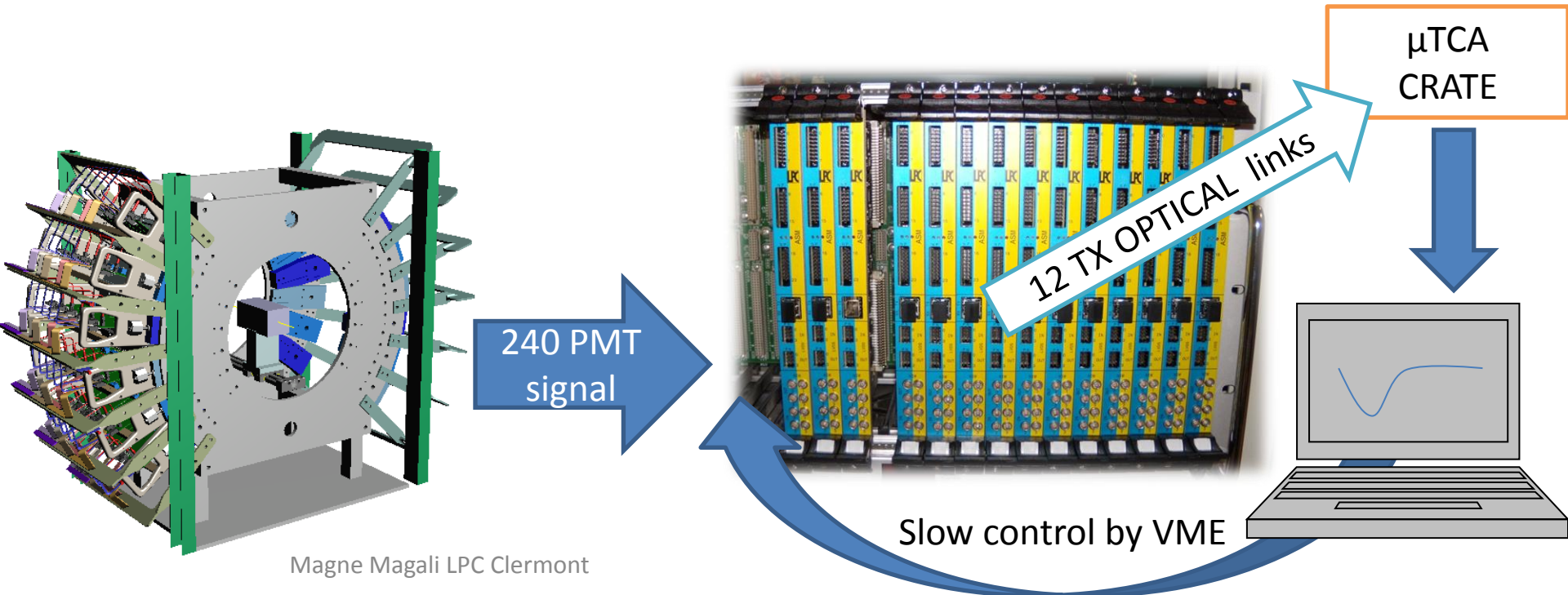
- The firmware are now stable and permit to make tests to well qualified it.

- Calibration must be add to current setup to hope to obtain low jitter permit by the DRS4 chip.

- More results in the next month

# Conclusion & Perspectives

- **<u>Perspectives</u>**
- Increase the data rate acquisition by implementing optical link to ATCA.
- Achieve  complete characterization  of the boards.
- Scale the whole system to 12 ASM boards




# Merci

Questions …