Développements de blocs 65 nm dans le cadre du projet RD53

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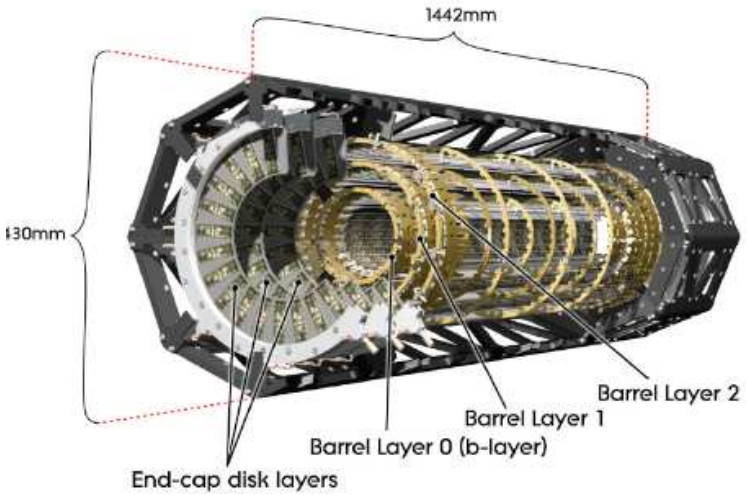
Introduction

- Pixels pour les expérience du LHC
  - Reconstruction précise des trajectoires de particules chargées proches du point de collision
- Programme RD53 :
  - R&D pour le développement du chip de lecture des pixels de ATLAS/CMS - Upgrade phase 2 (~2022)
- Principales spécifications :
  - Résolution spatiale : Pixels de 50 x 50 µm2 (25 x 100 µm2)
  - Résolution temporelle
  - Taux de Hit : 1 à 2 GHz/cm2
  - Tolérance aux radiations : 1000 Mrad
  - Faible consommation – Budget de Matière
  - Taille du chip : 2cm x 2cm (~10^9 transistors)
  - Radiation: 1 Grad, 10^{16} neq/cm2
  - Process : 65nm CMOS



- 19 instituts, 100 collaborateurs, Organisation en Technical Working Groups (WG)

Introduction

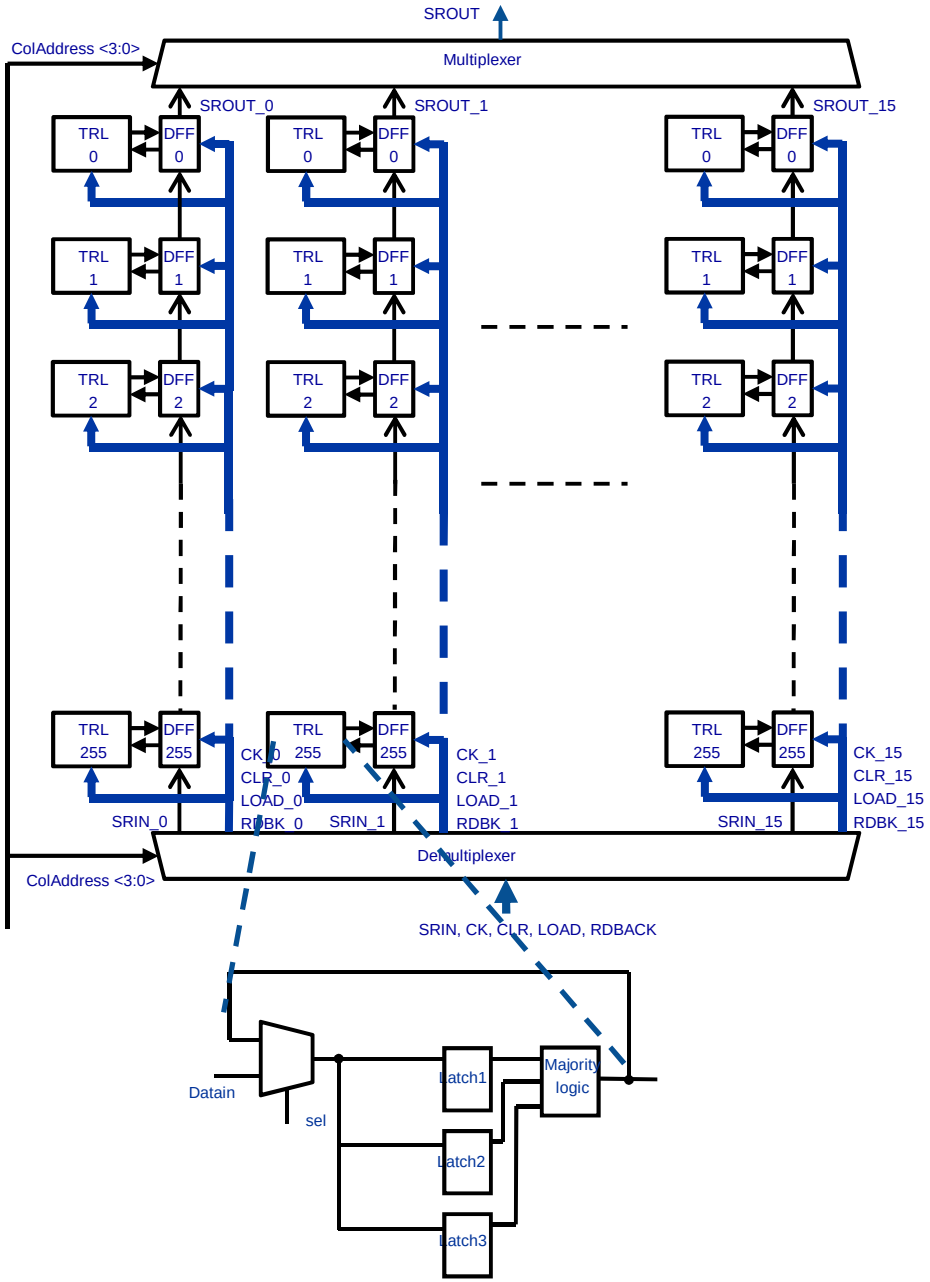
- Radiation WG :
  - Test et qualification du (des) process 65 nm pour un niveau de dose de 1 Grad (10^{16} neq/cm²)
  - Niveaux internes des détecteurs à pixels ?
- Analog WG
  - Spécifications du front-end analogique : Planar, 3D sensors, capacitance, seuil, bruit, charge …
  - Architectures alternatives : TOT, ADC, Synchrone, Asynchrone, Ajustement de seuil …
- Top level WG
  - Floorplan global pour la matrice de pixels
  - Choix du design flow approprié
- IP WG :
  - Listes des IPs analogiques ou mixtes (30)
  - Revue des spécifications en juin 2014

CPPM activities

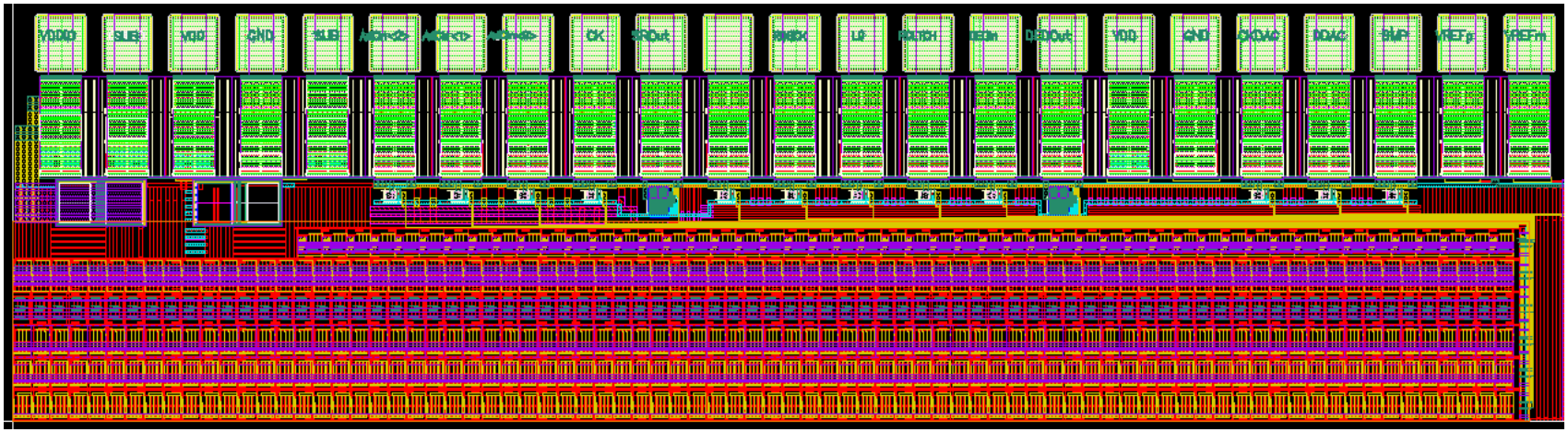
- CPPM participates in different WG
- Test and qualification of 65 nm process for a dose level of 1 Grad
- Analog IP blocks
  - ADC for monitoring
  - Bandgap voltage reference
  - Temperature sensor
  - Radiation monitor
- Analog pixel
  - SEU tolerant configuration memories
  - Pixel ADC for charge measurement

Pixel configuration memory

- Previous tests on the LBL chip :
  - Good results in term of tolerance to SEU
  - Design based on standard cells from ARM library
  - Some issues with dose effects
- New design :
  - Minimize the effect of glitches
  - Test of new structures (based on Hamming code …) to reduce the memory cell area
  - Design tolerant to a total dose of 1000 MRad



SEU chip organization



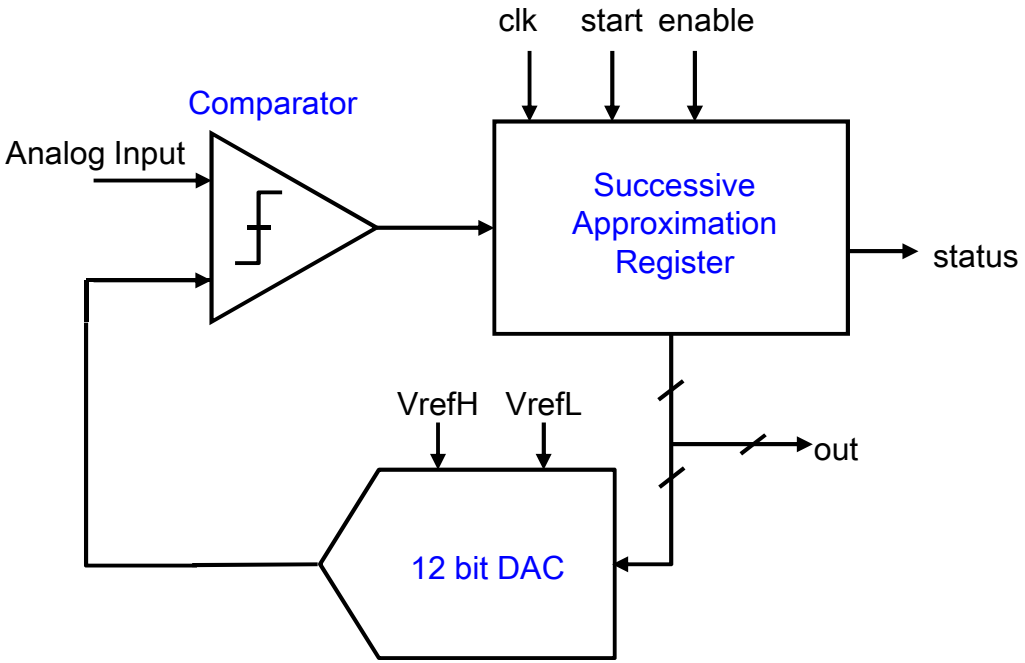
- SEU tolerant configuration memories to be implemented in the pixel

Denis Fougeron

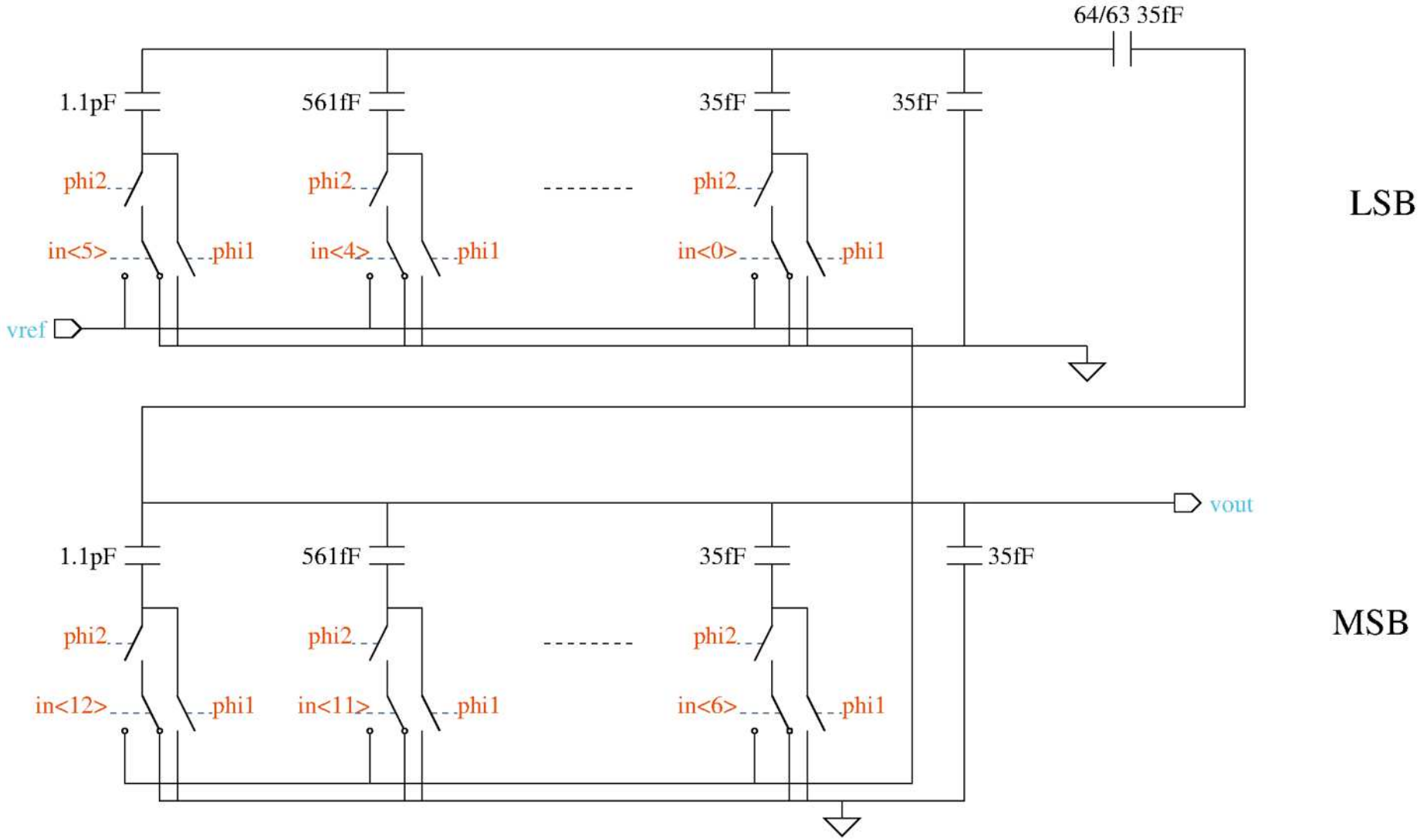
- 6 rows of around 600 memories to be tested:
  - Reference from LBL chip
  - Reference design with setting Wmin>300µm
  - DICE latches (with guard ring)
  - Interleaved DICE latches (a la FEI4)
  - Delay insertion on the Load node (typ: 5ns ± 1ns)
  - Hamming code (errors correction, double errors detection)
- Total area = 230 µm x 1820µm

Generic ADC for monitoring

- General purpose ADC
- Inputs are slow variation signals :
  - Temperature, leakage current …
- Power supply = 1.2 V
- Sampling rate: (<100) ksample/s
- Architecture : Successive Approximation Register (SAR)
- Precision : 12 bit (LSB ~ 250 µV)
- DC accuracy :
  - Integral linearity error : +/- 1 bit
  - Differential linearity error +/- 0.5 bit
- Operating input voltage : 0-Vref (VrefL-VrefH)
- Conversion time : 14 clock cycles
- Tolerance to a TID of 1000 Mrad



DAC design

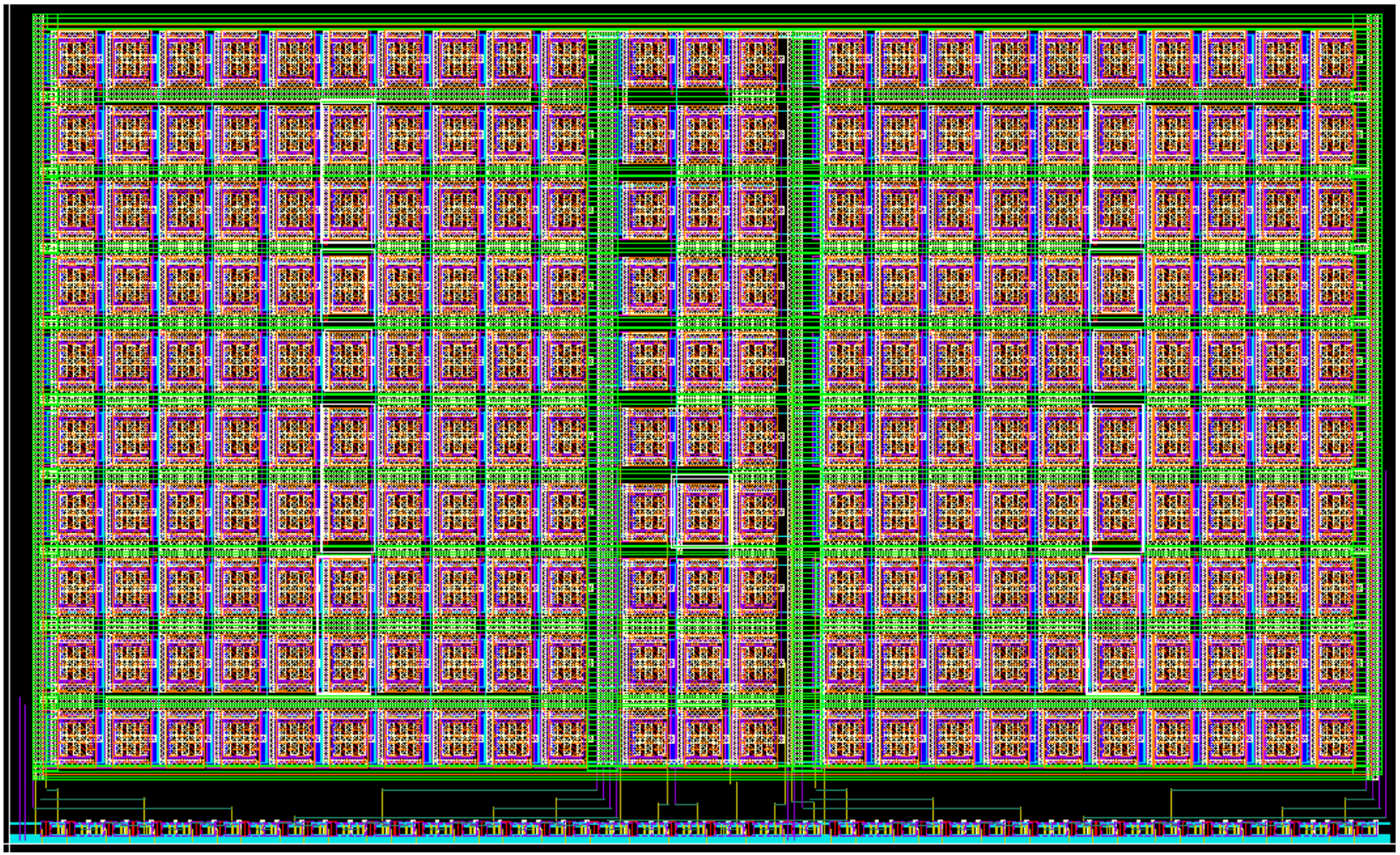


- 12 bits DAC : Divided into two 6bits sub-DACs

DAC design status

- 12 bits with 0 to 1 V dynamic range -> LSB=244µV for Vref = 1 V
- MIM capacitance with 2.0fF/µm²
  - Cu = 35 fF (4µm x 4µm) is enough for matching and set to 100fF (7µm x 7µm)
- Schematic simulations : INL < 1LSB
- Main issue : layout parasitic capacitors
  - Post layout simulations show a high non linearity
  - Layout re-optimized but the output capacitance still high
- MSB array output capacitance :
  - Global gain decrease
  - LSB = 237 µV instead of 244 µV
  - A buffer stage can be added between the DAC and the comparator
  - An OpAmp stage with DC gain > 86 dB is designed but not yet inserted in the ADC
  - Will be tested and can be used as a general purpose operational amplifier
- LSB array output capacitance :
  - High non linearity
  - Extracted view : the INL estimated to 4 LSB
  - 5 bits trimming DAC implementation to compensate this non linearity

Layout



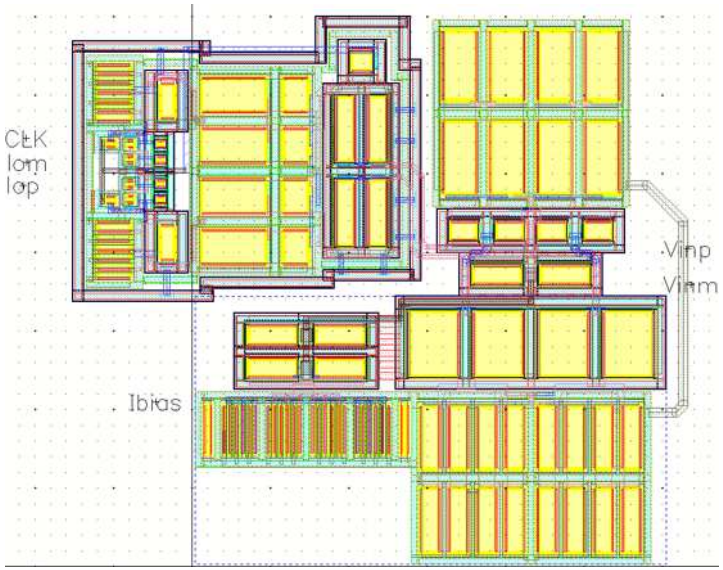
- Dimensions : 180µm by 300 µm

Renaud Gaglione

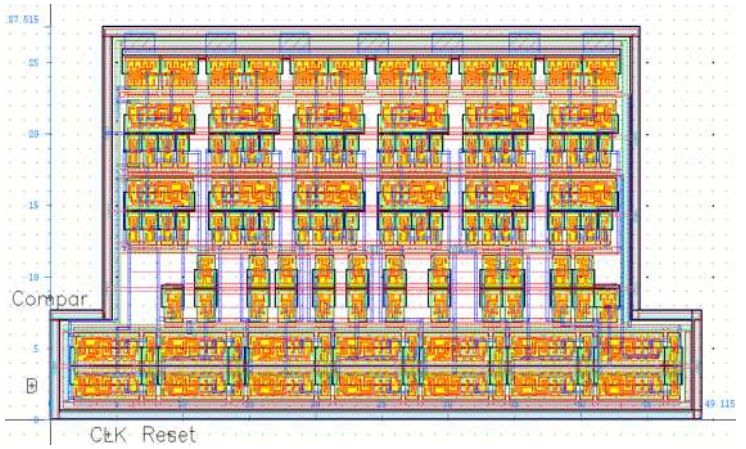
Comparator and SAR logic for 12-bit ADC in 65nm CMOS technology

- Dynamic comparator:
  - CLK = 0, compare the data
  - CLK = 1, the output keeps the ancien value

Input offset	135µV
Delay (max)	4,3µs (at 1,03V)
Input range	0V - 1,03V
Dimension	40µm * 35µm
Power	1,2V / 0V
Consomation	21µW



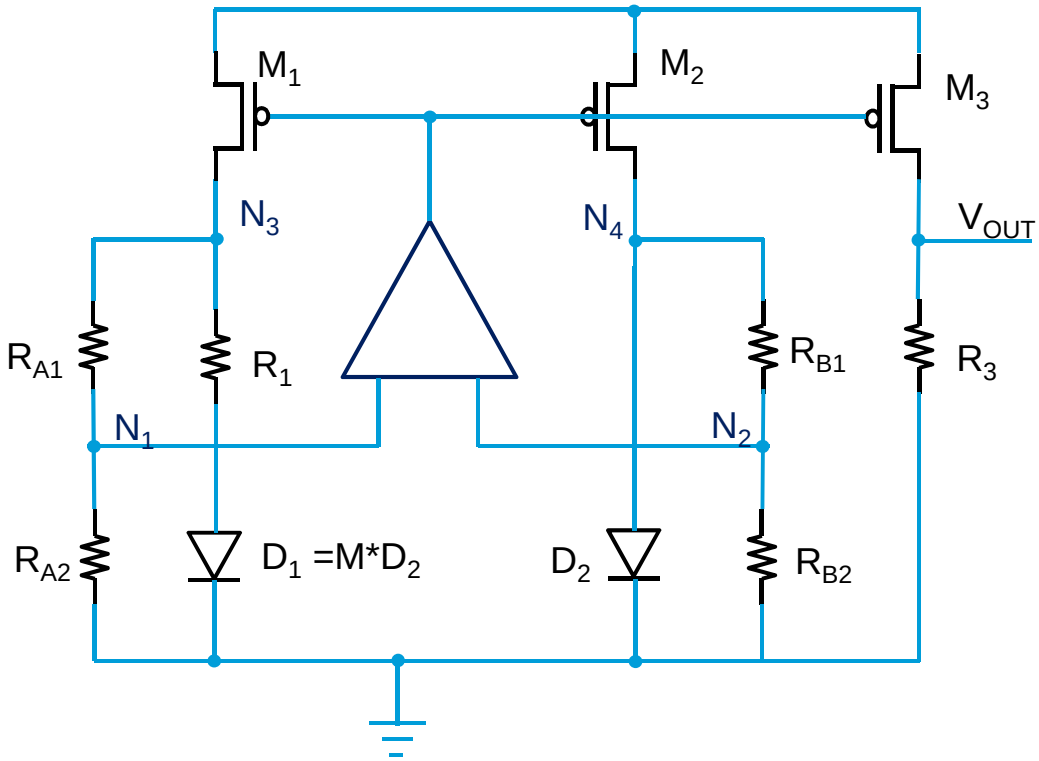
- 12-bit SAR Logic: (dimension: 28µm * 50µm)
  - CLK ↗ , readin data from comparator
  - CLK ↘ , output 12-bit binary code to DAC
  - At the 13th clock, output a flag to the memory for saving the final 12-bit binary code.



Anqing Wang

Bandgap reference

- Bandgap Reference for general purpose provide voltage reference for :
  - Biasing, DAC, ADC …
- 2 BG design versions are implemented :
  - Bipolar device
  - DTMOS device
- 1 CTAT block designed with irradiation effects compensation
  - Main block of a BG design or a temperature sensor design
  - Power supply = 1.2V to 2V
  - Each device Vds or Vgs still < 1.2V
- Simulated from -50 °C to 120 °C
- Layout : OK
- Post layout simulations : OK



Devices for irradiation test

NMOS & PMOS (multiplier=finger=1)

(common G, common S and common SUB for all the mos)

PCH (W/L)	120n/60n	240n/60n	480n/60n	1u/60n
	120n/120n	240n/120n	10u/10u	240n/240n
PCH_lvt (W/L)	120n/60n	240n/60n	480n/60n	1u/60n
	120n/120n	240n/120n	10u/10u	
NCH (W/L)	120n/60n	240n/60n	480n/60n	1u/60n
	120n/120n	240n/120n	10u/10u	240n/240n
NCH_lvt (W/L)	120n/60n	240n/60n	480n/60n	1u/60n
	120n/120n	240n/120n	10u/10u	

Bipolars (W=L=10u)

in BandGap circuit

	Multiplier
PNP	1
	8
NPN	1
	8

NMOS & PMOS (m=f=1)

(each one has its own G,D,S,SUB)

Type	W/L
PCH	10u/10u
NCH	10u/10u

Diodes in Bandgap circuit

(using PMOS in replacement)

Multiplier	PCH (W/L)	
4	1u/1u	20u/1u
32	1u/1u	20u/1u

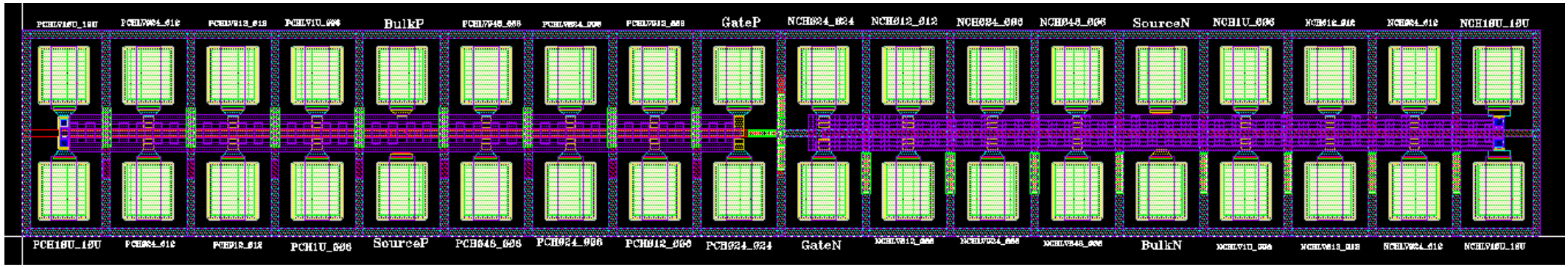
Diodes (thin OD) in IO circuit for ESD protection

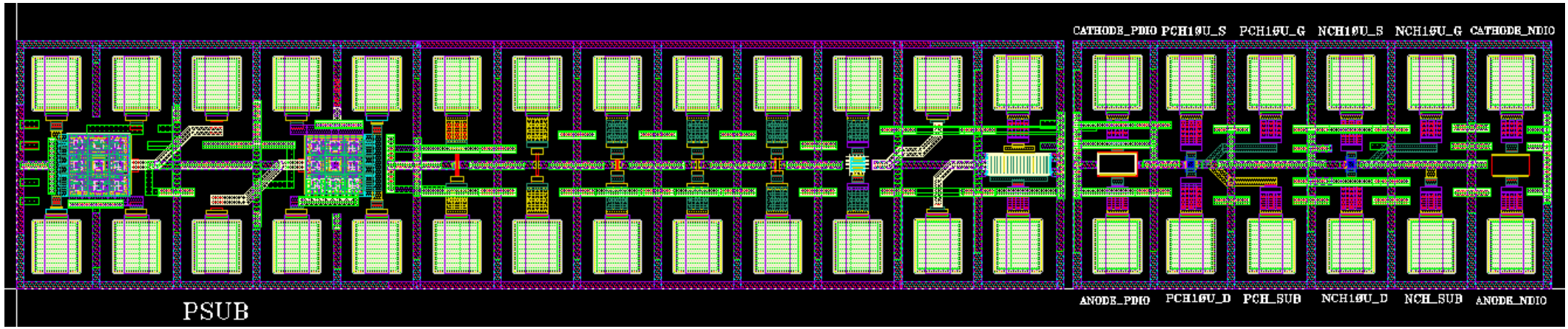
Type	L	W	Multiplier
PDIO	22,095um	1,86um	15
NDIO	22,095um	1,86um	15

Resistances in BandGap circuit

rppolywo	rppoly	rnpolywo	rnpoly	rnwod
10K ohm	200 ohm	1K ohm	100 ohm	2K ohm

Layout



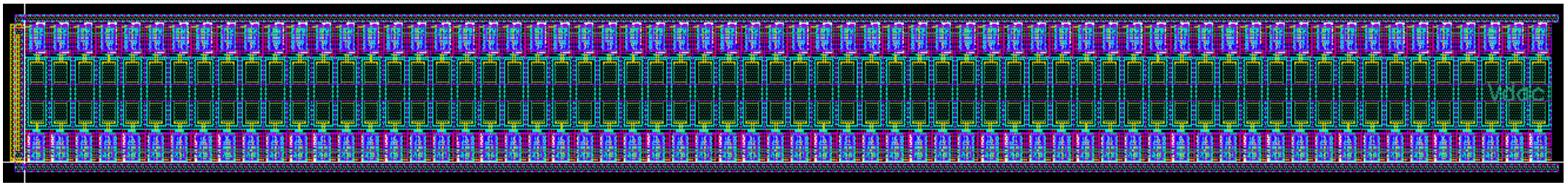


Anqinq Wang

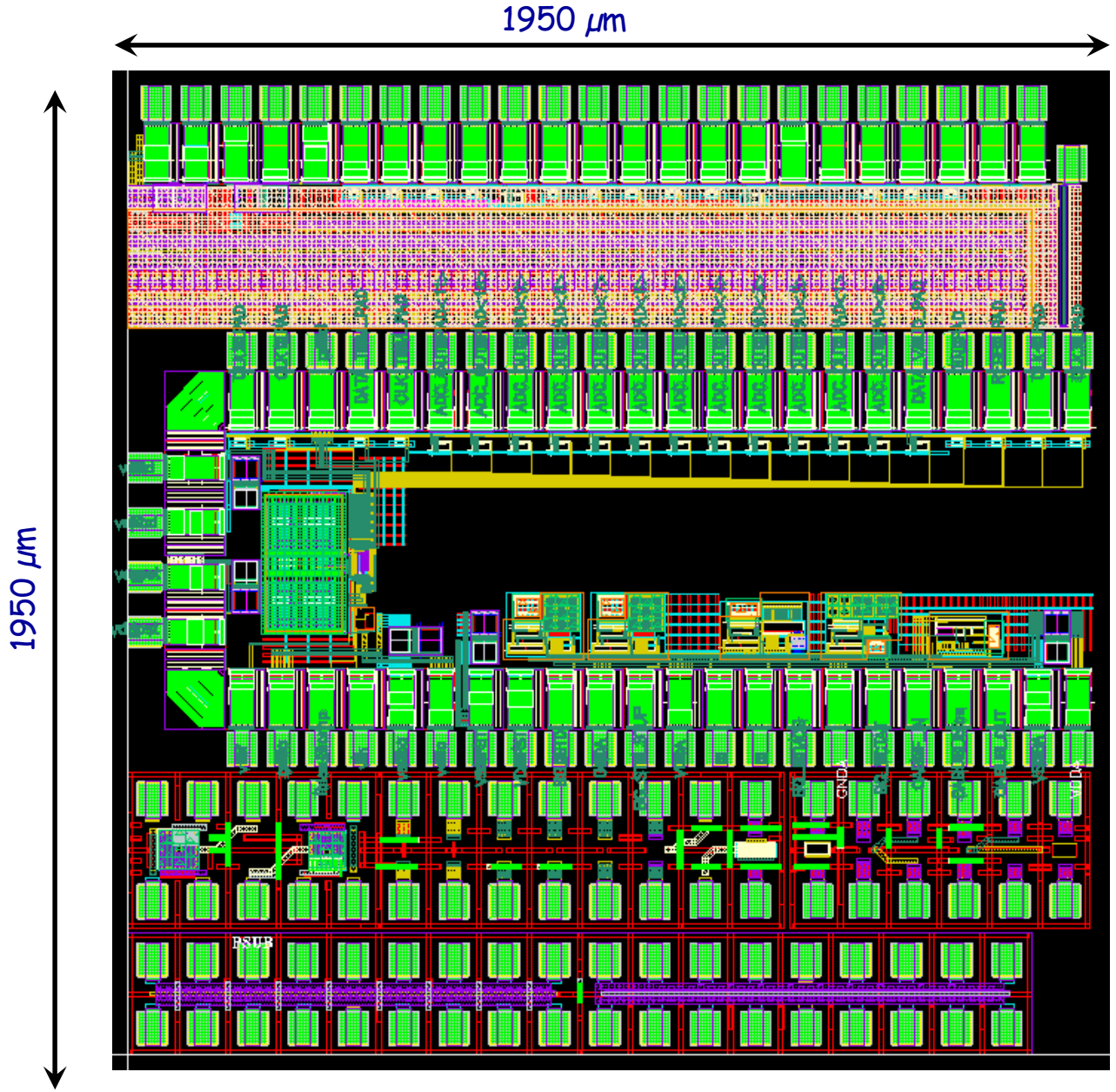
- Pads without ESD protections
- Size : 270 µm x 1800 µm

In pixel 7 bits ADC block

- Replace the ToT inside the pixel
  - Charge measurement
- DAC Schematic and layout proposed by LPSC in 130 nm process
  - The design adapted to the 65 nm process
  - Unit capacitance Cu ~ 3 fF based on metal parasitic capacitance M2-M1/M3
  - Parasitic output capacitance
- Area : 280 µm x 30 µm (Non optimized)
- Test of mismatch effects, linearity …
- The design and the layout have to be optimized to reduce the area
  - 25 µm x 25 µm or less



Chip Layout



Conclusion

- A parts of the different IP blocks were implemented and submitted successfully
- Base line for the final design
  - Have to be re-optimized and improved …
- The digital blocks designed with ARM library
  - Waiting for the CERN design kit
- Modification of I/O cells ARM library (only use of thin oxide devices)
- Collaboration of different IN2P3 institutes inside RD53 project
- Submission date : June 4 (mini@sic) through Europractice

Merci pour votre attention

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