LPSC Grenoble
Laboratoire de Physique Subatomique et de Cosmologie

Converters R&D

LPSC Grenoble

Team

- D. Dzahini, L. Gallin-Martel, F. Rarbi, J. Bouvier
- PhD Student: M. Zeloufi
- Internship students

Outline

- Physic experiments:
  - ATLAS-Larg: Phase-I
    - PEALL chips
  - ATLAS-Larg: Phase-II
    - New SAR Architecture
- Imaging Read-Out chip:
  - MASSAR
  - Ramp ADC

Outline

- Physic experiments:
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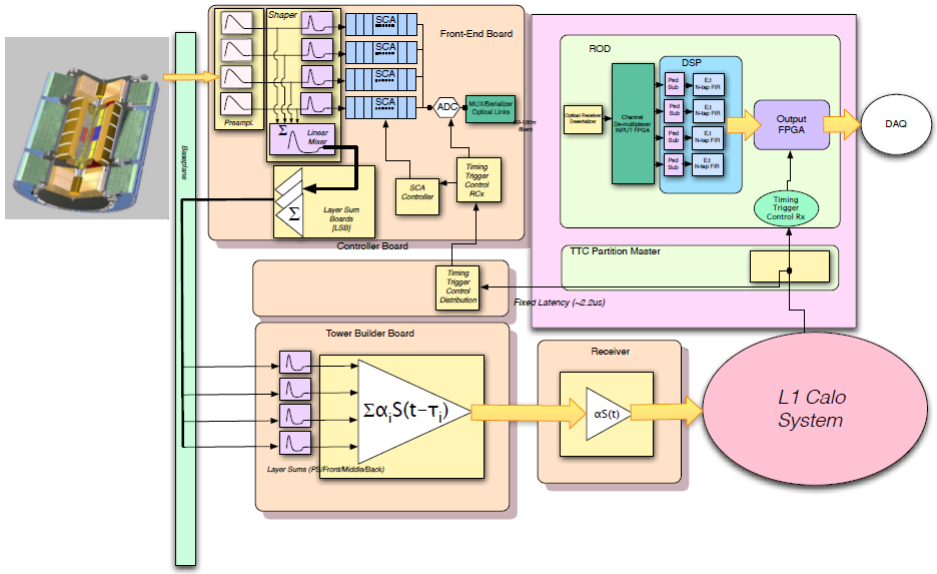
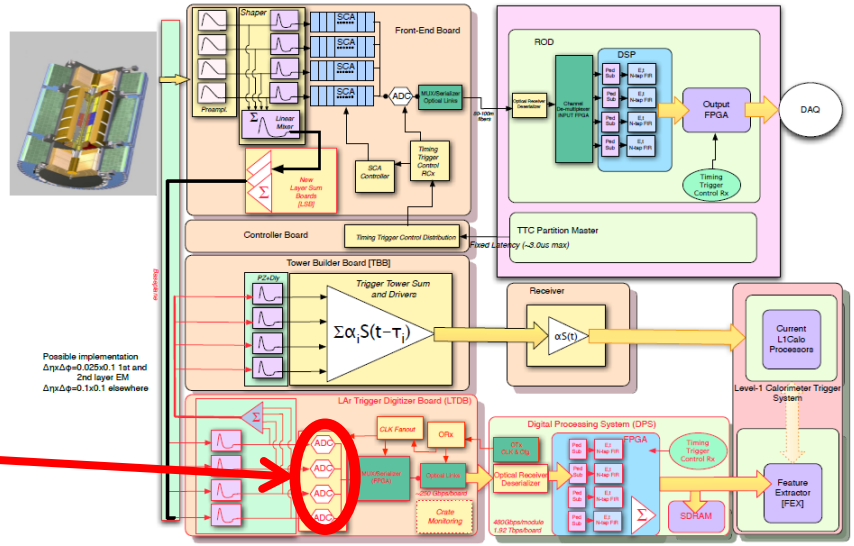
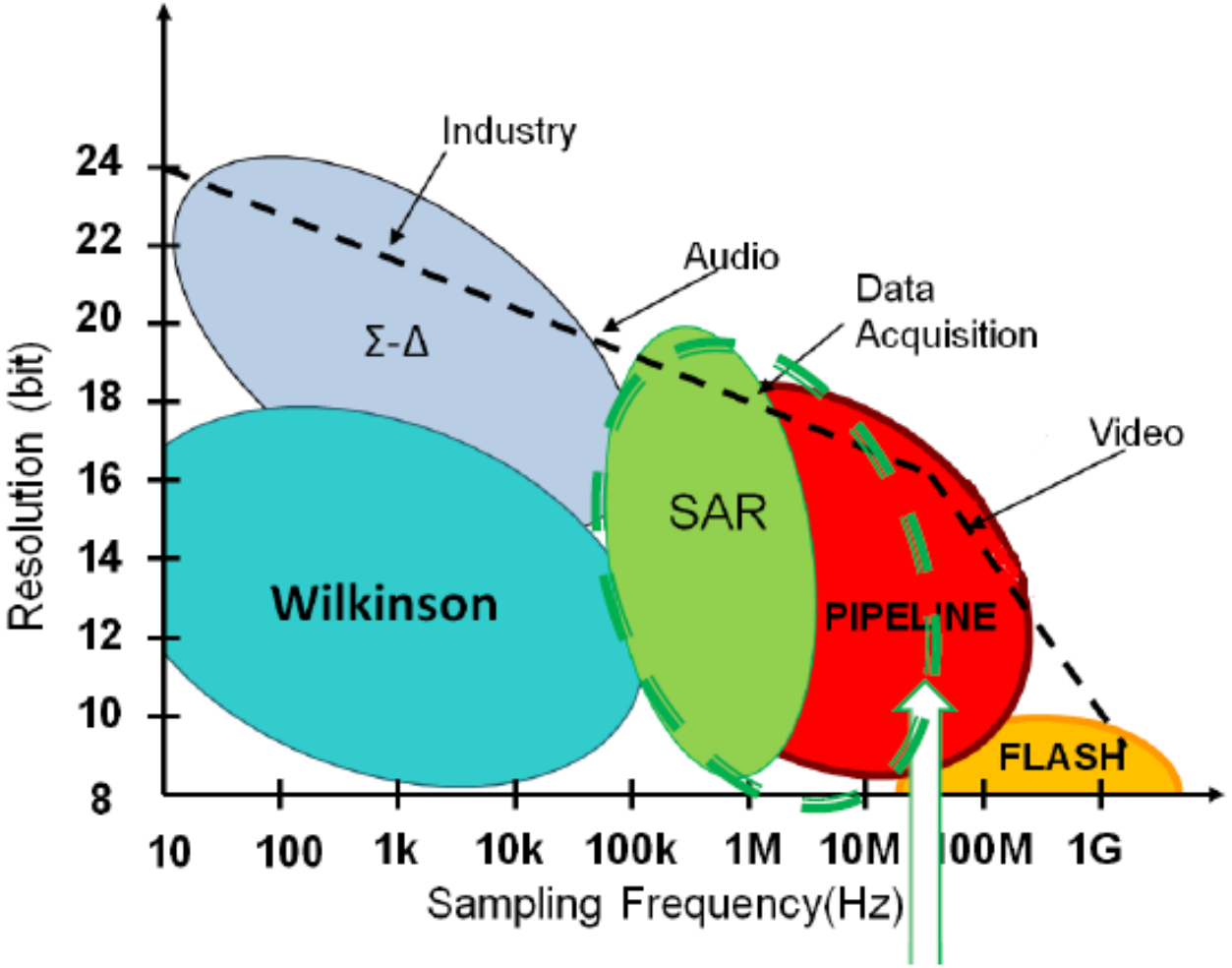
ATLAS-Larg: Phase-I



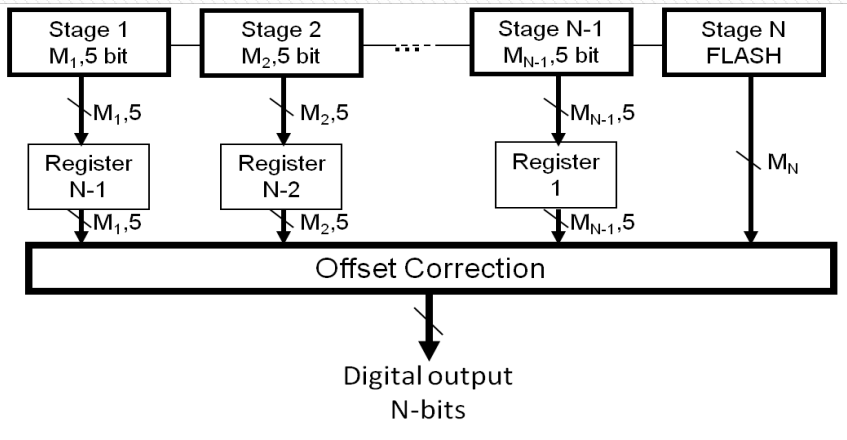


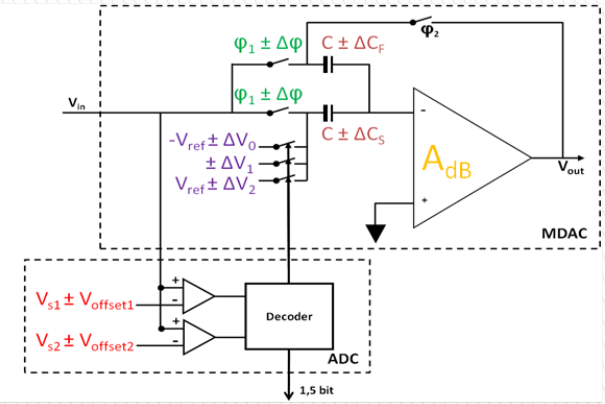
40MSPS, 12b
Low power
Low latency

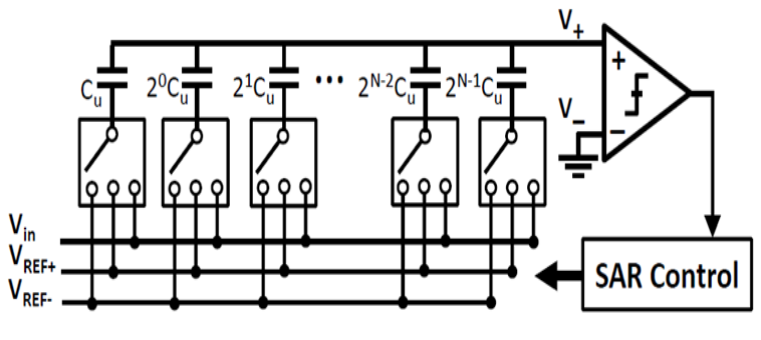
ADC overview



PIPELINE vs SAR ADC







- Binary search algorithm following a binary-weighted capacitive DAC
- DAC nonlinearity limits the INL and DNL of the SAR ADC → N-bit precision requires N-bit matching from the DAC

PIPELINE ADC

SAR ADC

Why moving from PIPELINE to SAR?

- Allow high speed design
- Natural important latency
- Power dissipation (amplifier)
- ΔV_{ref} means more INL
- Mismatch in capacitors (*)
- V_{ref} buffer bandwidth (*)
- Clock frequency (as sampling)
- Sampling time (large: 12.5ns)
- Total die area could be large
- Scaling to future 65nm process

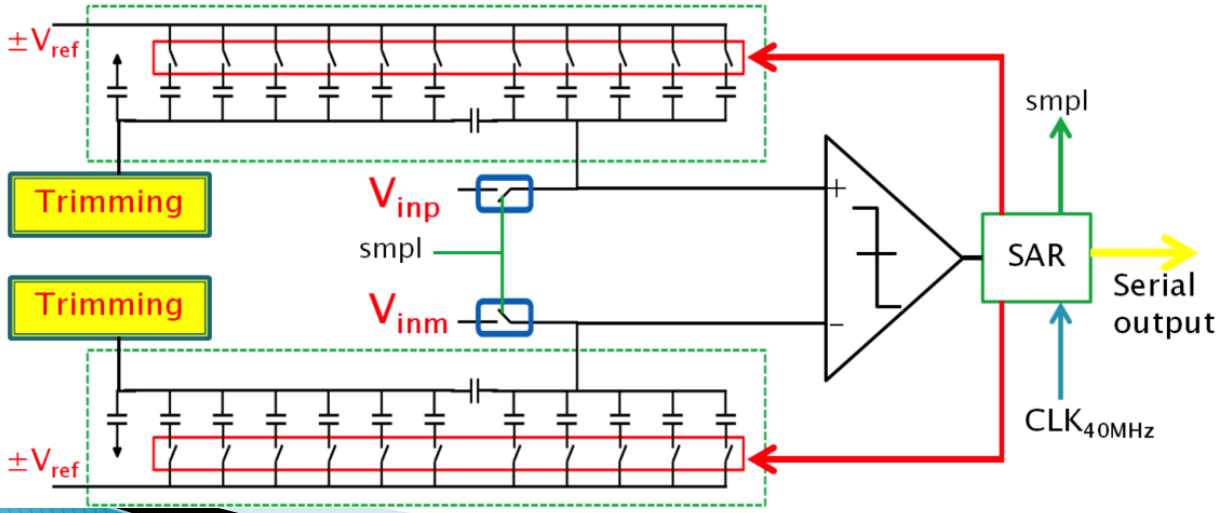
- IBM 130 allows high speed
- The best **latency** (after a Flash)
- The best **power** dissipation
- ΔV_{ref} does not means INL
- Mismatch in capacitors (**)
- V_{ref} buffer bandwidth (**)
- Higher frequency clock (**)
- Sampling time brief➔ 3 or 4ns
- Die area very small
- Ready for scaling to 65nm

PIPELINE Architecture

SAR Architecture

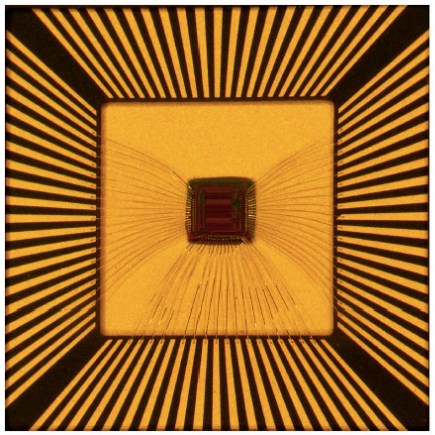
PEALL ADC architecture (1)

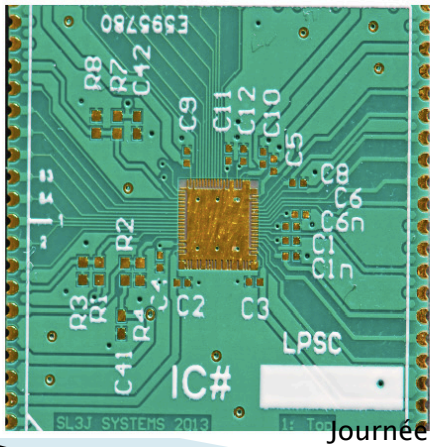
- Power Efficient and Low Latency SAR ADC
- Main features of our PEALL ADC:
  - Asynchronous high speed clock internally generated from the 40MHz clock and the output of the comparators
  - Fully differential configuration: array of capacitors is segmented in 2
    ➔ Small area
  - Trimming feature to compensate from the capacitor mismatch

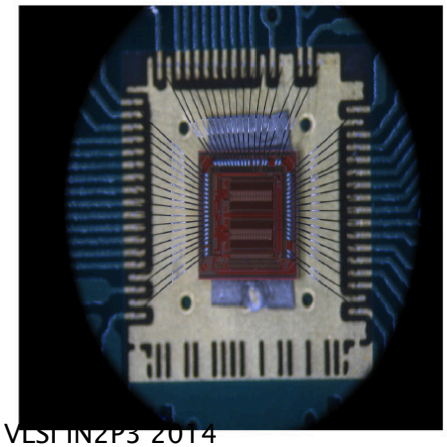


1st SAR ADC Prototype

- 2 channel version with external V_{ref} tested in May 2013
  - Local clock generator was working properly
  - The design suffers from sampling noise at the V_{ref} due to inductance problems caused by the bonding wires from the chip to the package
- A Chip on board made to reduce the inductances from 5nH to 3nH, but we were still limited at 20MSPS and ±4LSB of INL



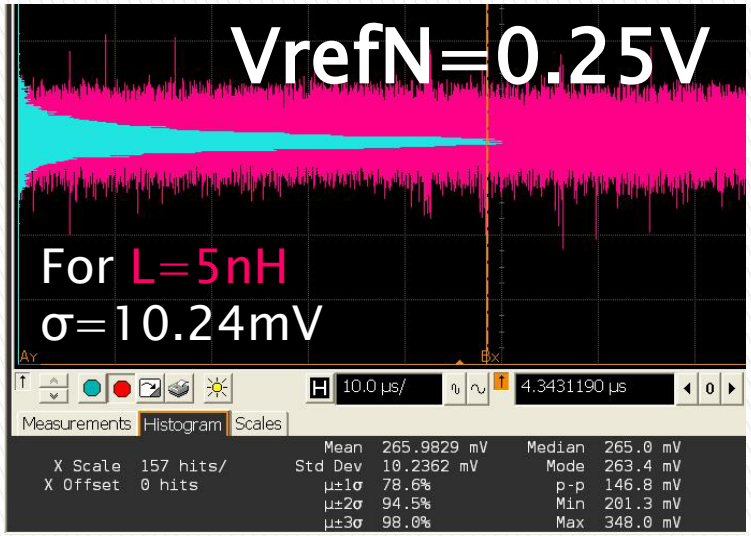


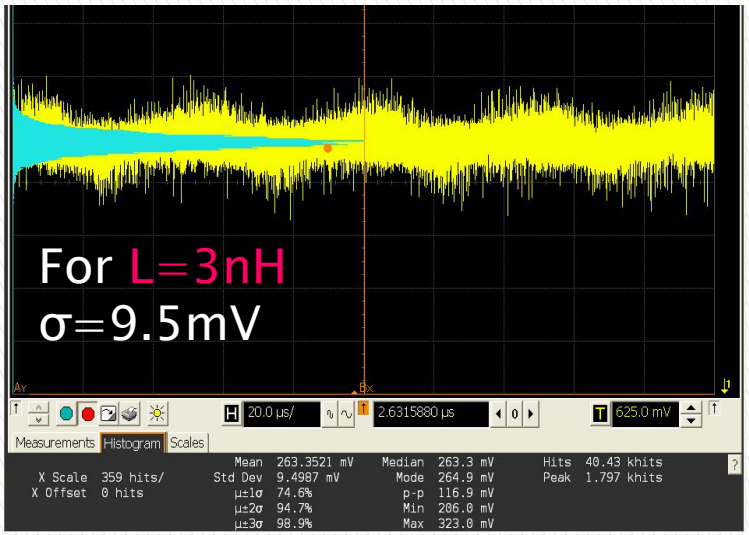


1st Prototype: V_{ref} limitation

Measured noise on both V_{ref} nodes:

V_{ref} never settles properly



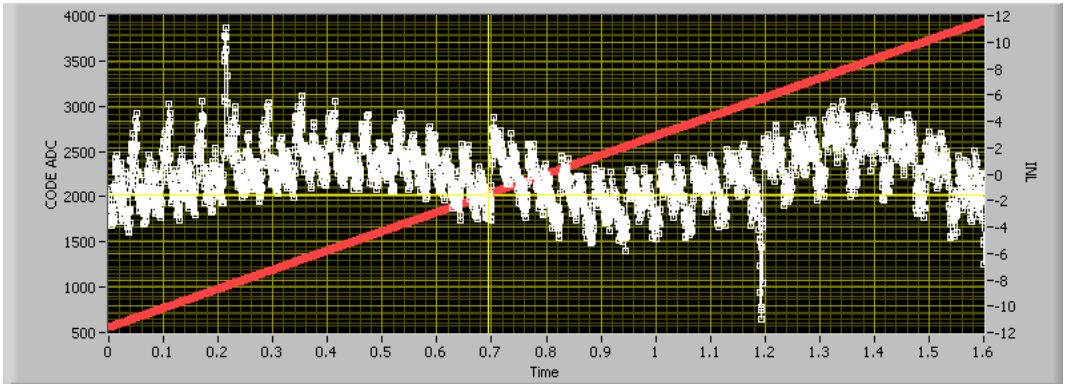


Packaged prototype

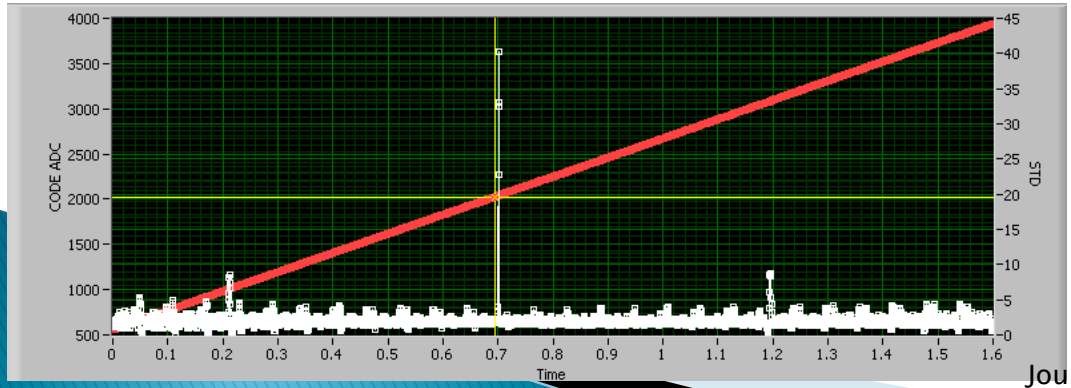
Chip on board

1st Prototype: Testing Results

- Sampling Clock: 20MSPS
- 5mW/ch (external V_{ref})
- INL & noise measurements

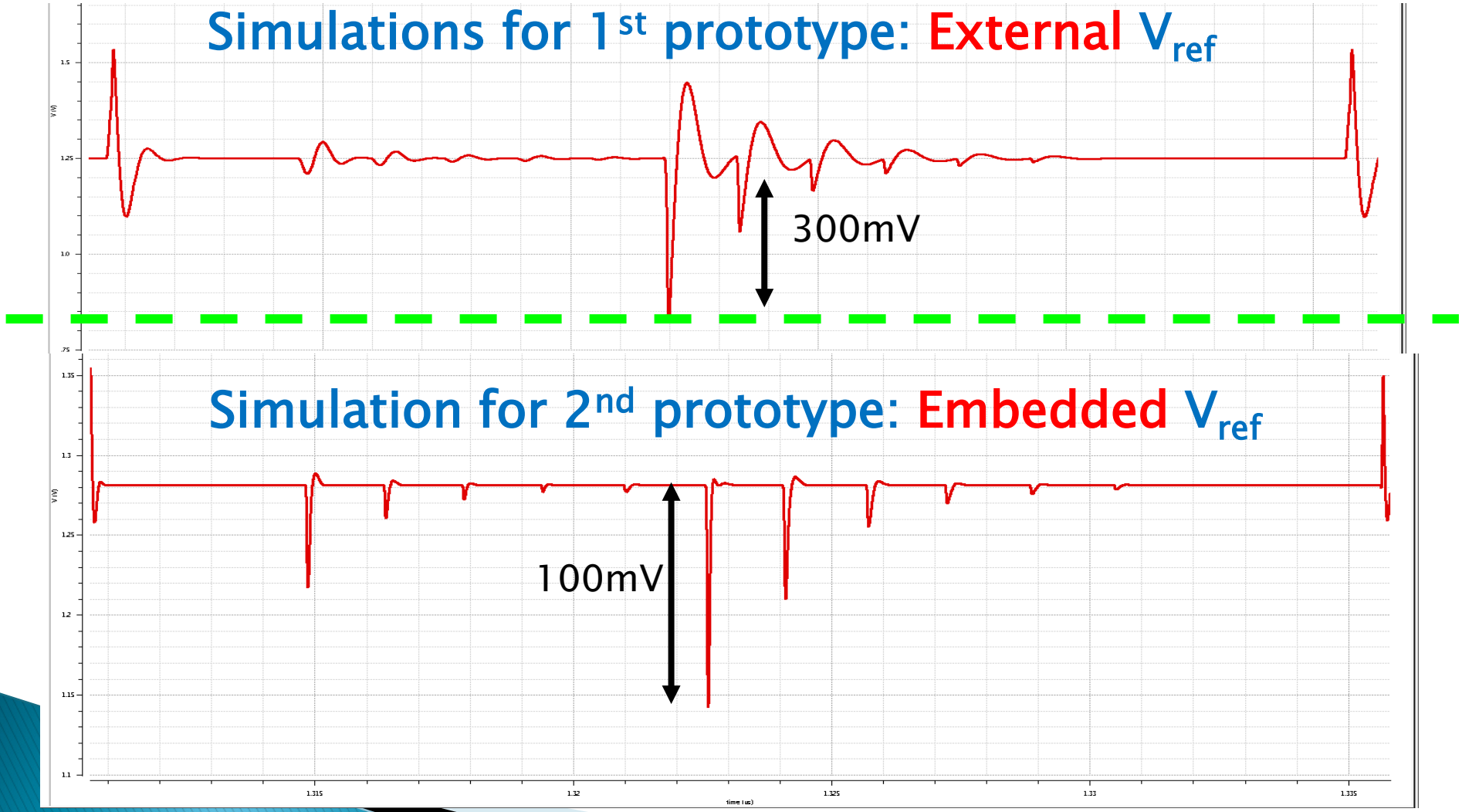


<= INL=±4LSB
BUT some spikes



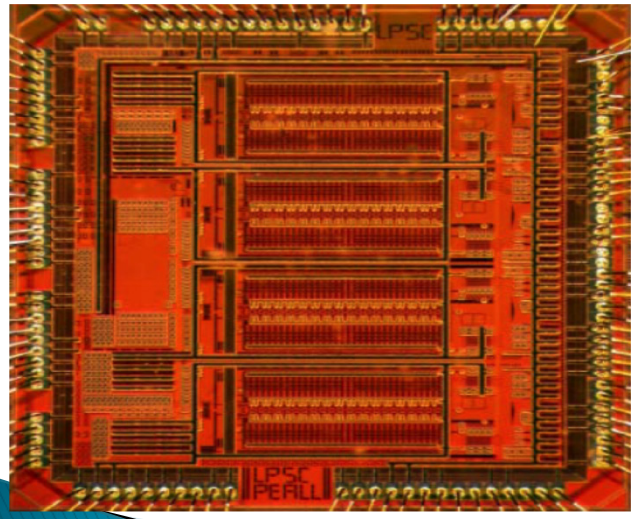
<= RMS noise for each output code

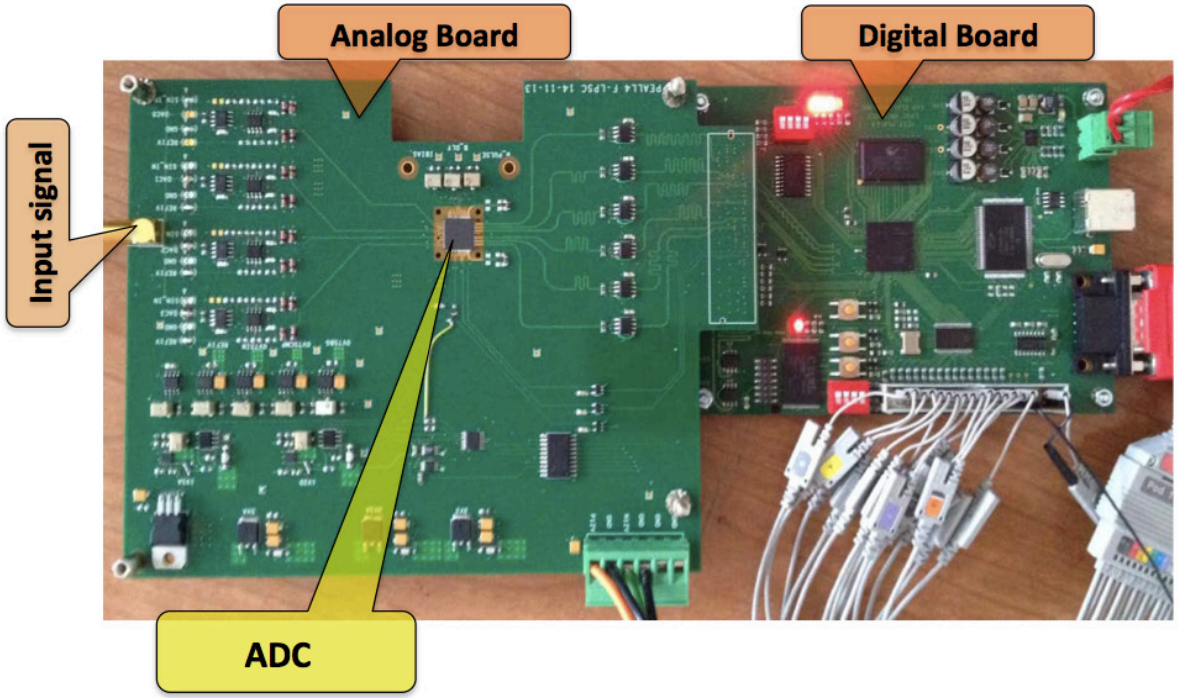
V_{ref} settling solutions



2nd SAR ADC Prototype

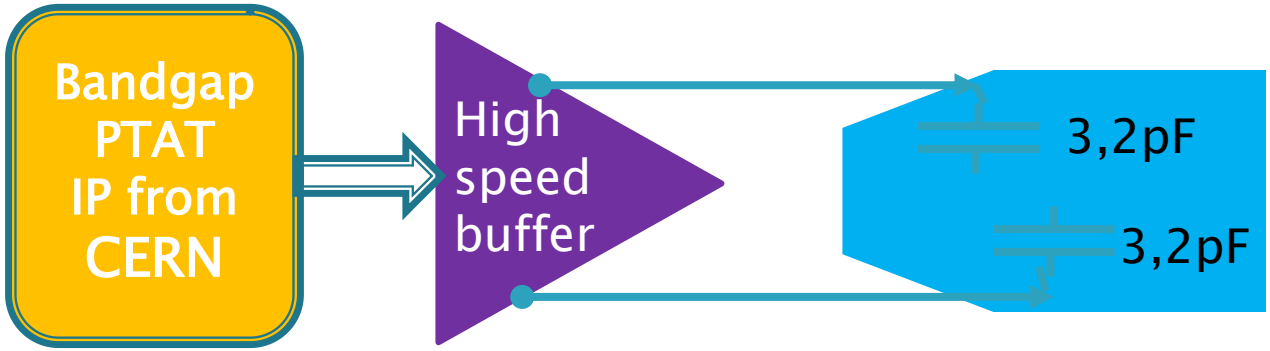
- 2nd prototype with 4 channels and embedded V_{ref}
  - Chip size: 2.8 x 3.4 mm^2 in a QFN 64 package.
  - Power consumption: 5 mW/ch for core ADC,
    27mW/ch with V_{ref} driver and output sLVDS (CERN IP)





Integrated V_{ref} Challenge

- V_{ref} define the dynamic range for the ADC
- It is built from a bandgap cell (CERN IP) followed by a very high speed (5 GHz) and low impedance amplifier designed at LPSC

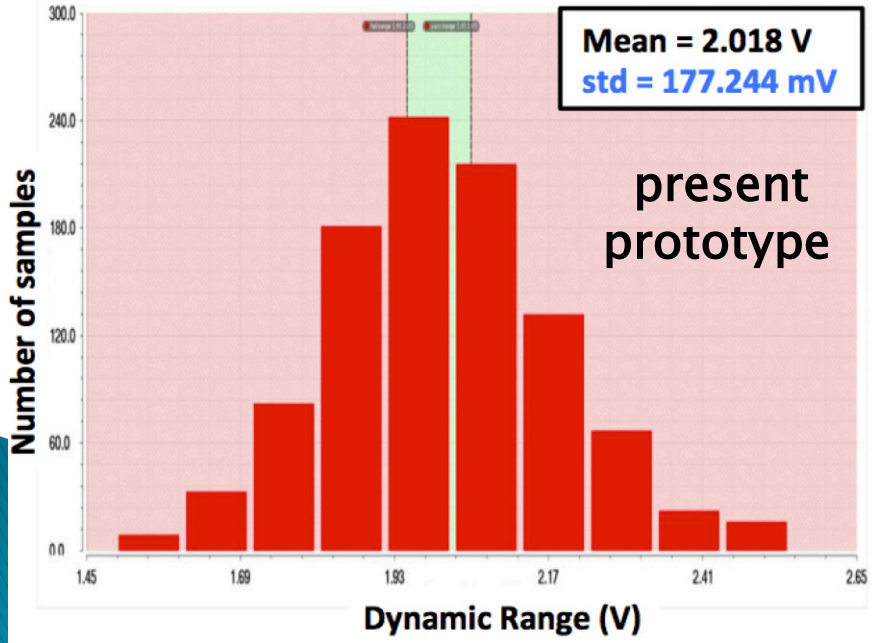


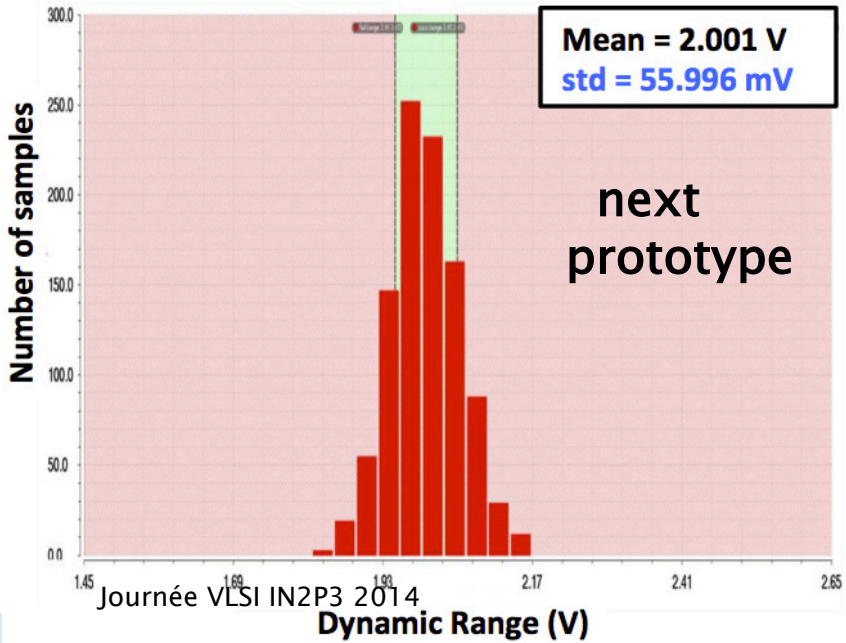
- Our testing results confirms that we succeed with the bandwidth of this buffer.
- ADC works positively at 40MSPS, with the 640 MHz clock generated

V_{ref} testing results

- A reference voltage 15% lower is found
- The cause of the dispersion was identified
  - Mismatch in reference voltage generation

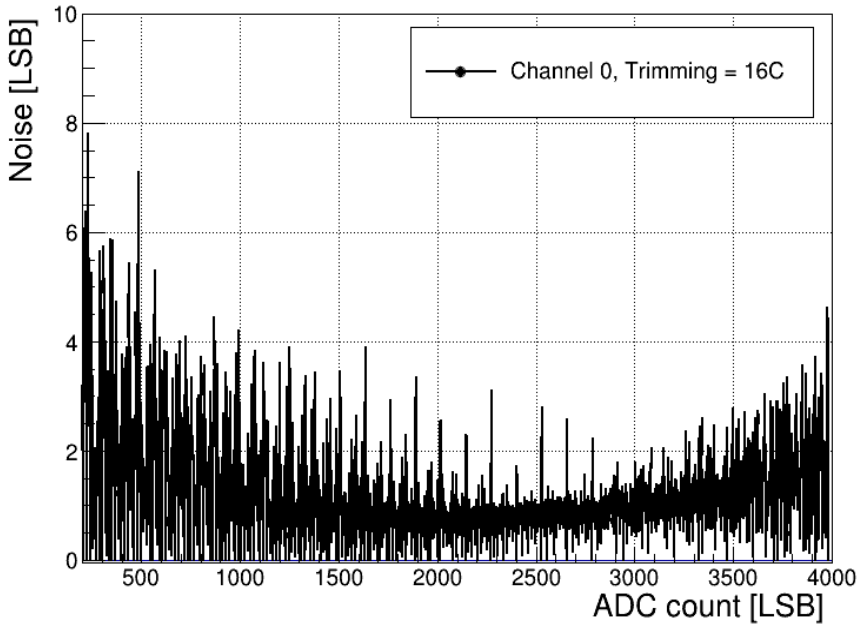
Chip Number	$V_{ref}(V)$
0	1.73
1	1.73
2	1.73
3	1.66
4	1.45
5	1.62
6	1.78
7	1.70
8	1.70
9	1.56
10	1.81

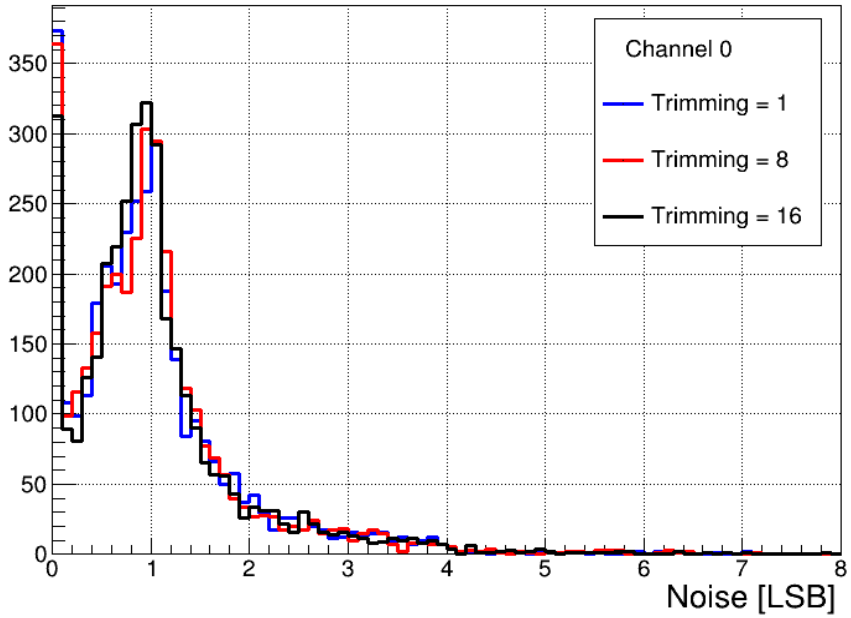




ADC output noise distribution

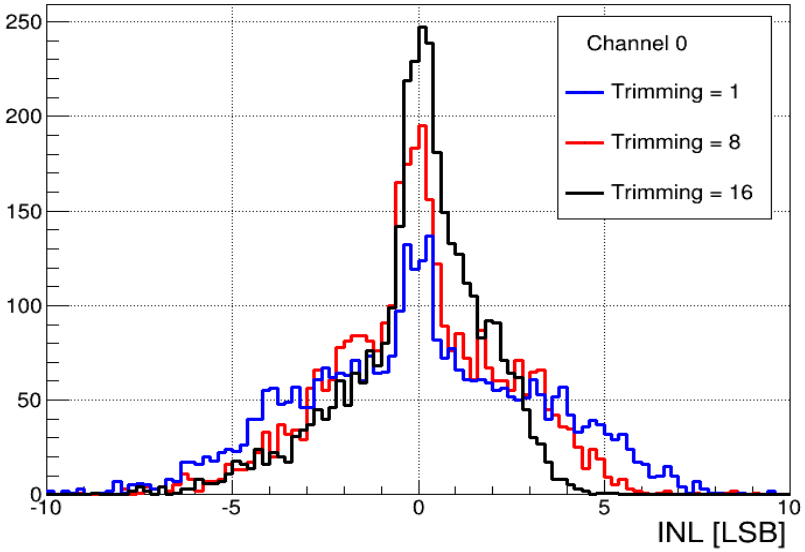
- Spikes appear at regular codes

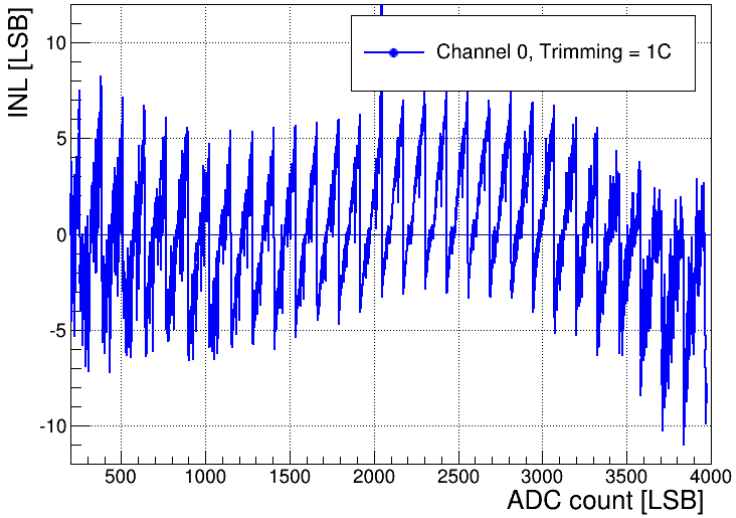


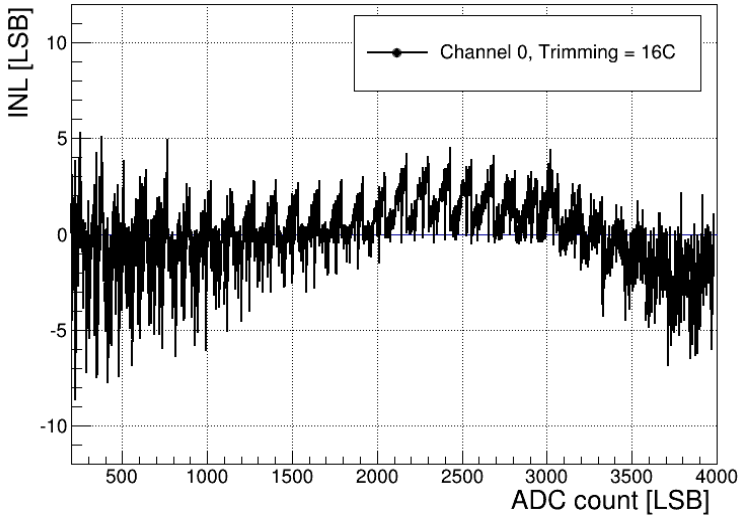


ADC INL

- Trimming feature is working
  - INL is progressively reduced
- Spikes appear at exactly same codes following the noise results

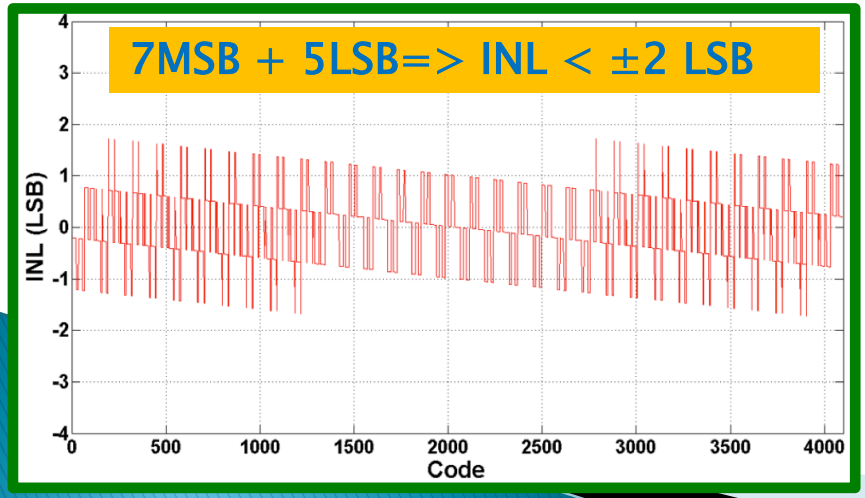


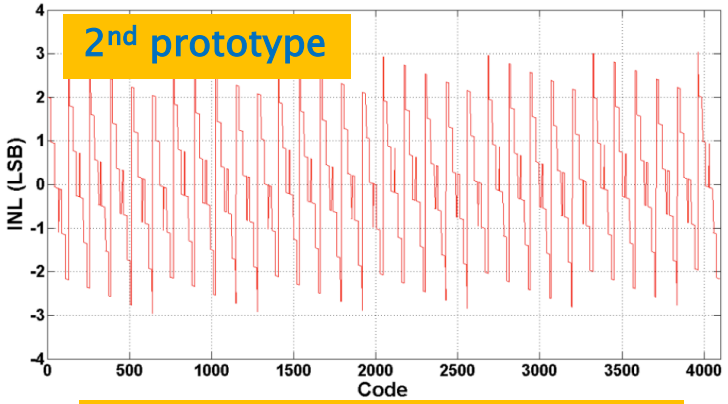




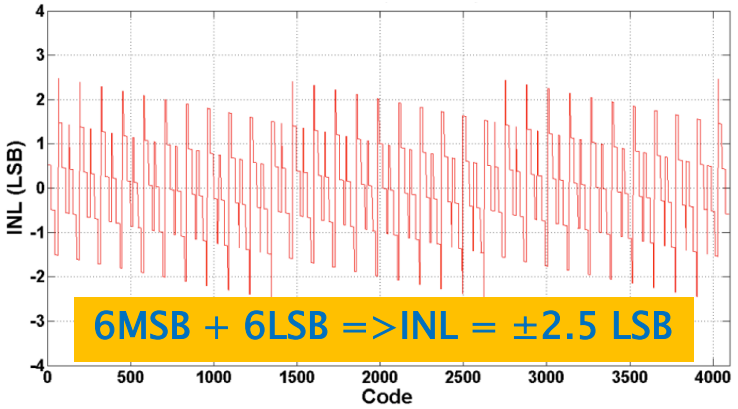
Segmentation impact on INL

- INL could be improved by a better segmentation of the capacitor array
- 3 emulated configurations:
  - Improvement in linearity with 7MSB + 5LSB conf.





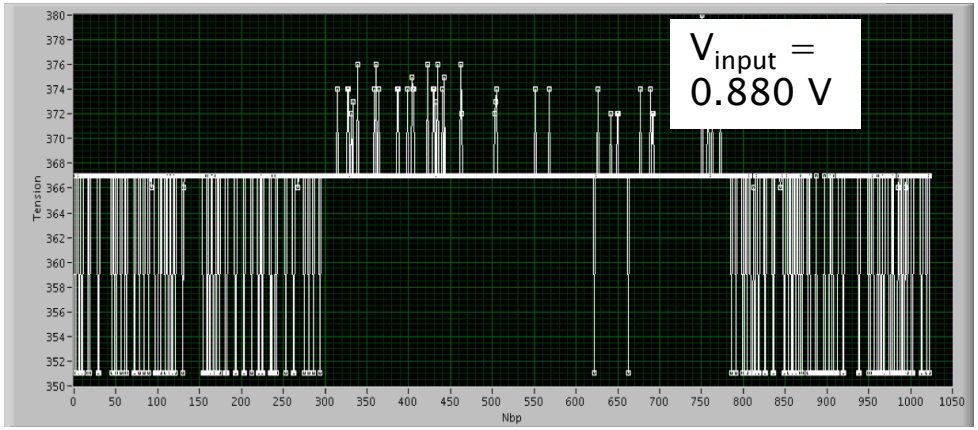
5MSB + 7LSB => INL = ±3 LSB

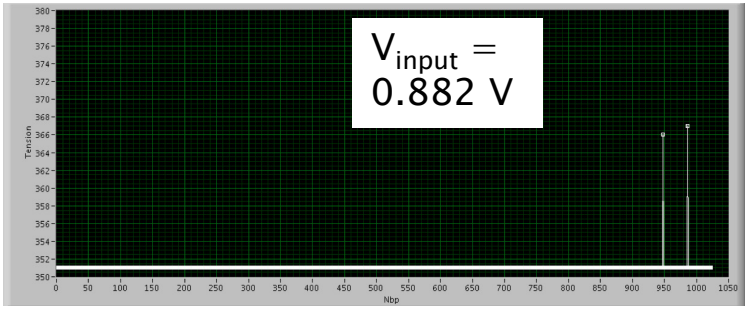


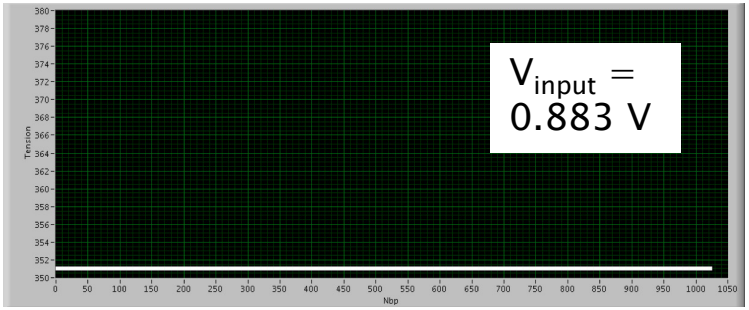
1 LSB of Linearity is saved by segmentation improvement

Spike problems

- Spikes observed for specific input signal always a fraction of V_{ref}
  - It is not a random distribution
  - Obvious correlation between “noise” spikes and INL’s spikes

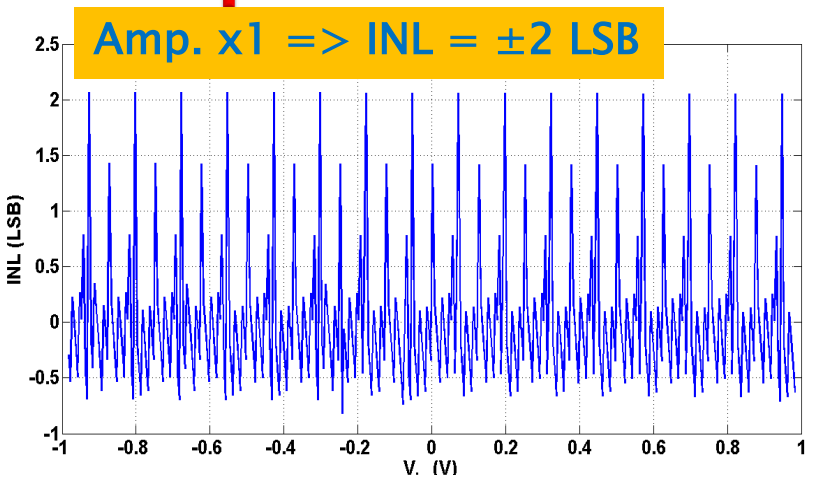


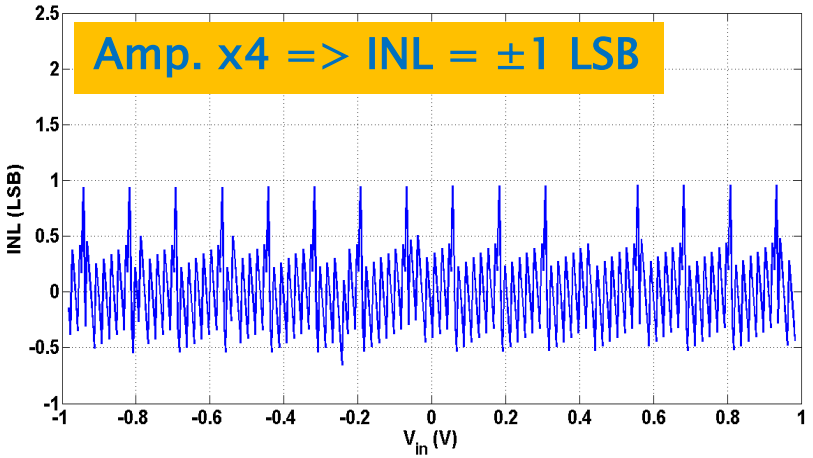


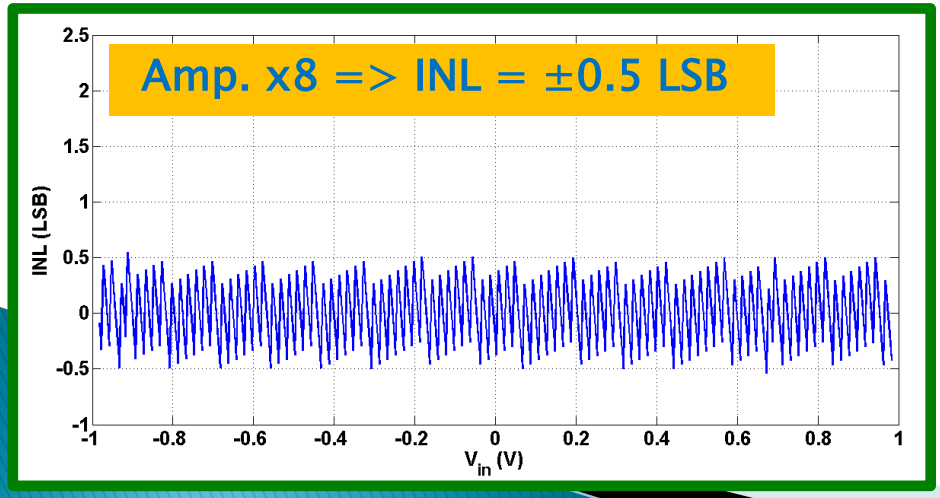


Source & solution for spikes problem

- Source of the spikes problem:
  - Segmentation gives a 2nd order settling time for the DAC
  - Meta-stability of the comparator



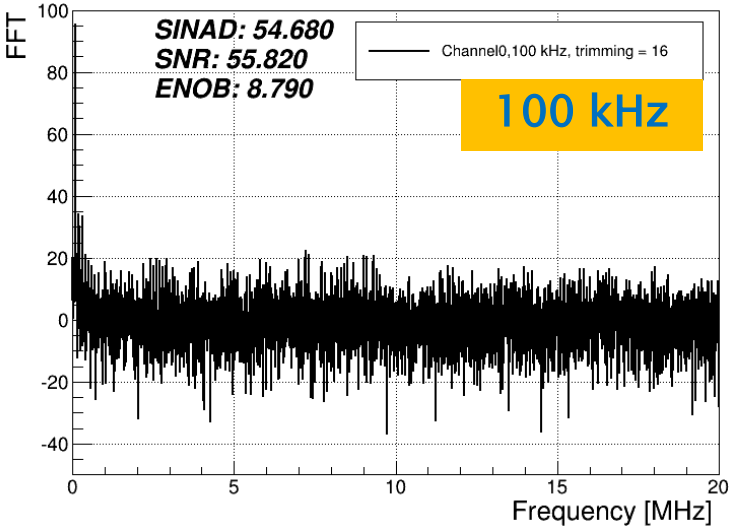


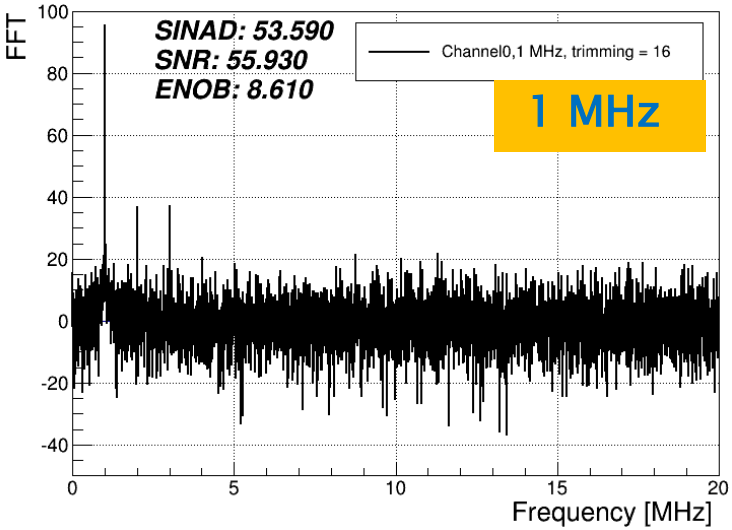


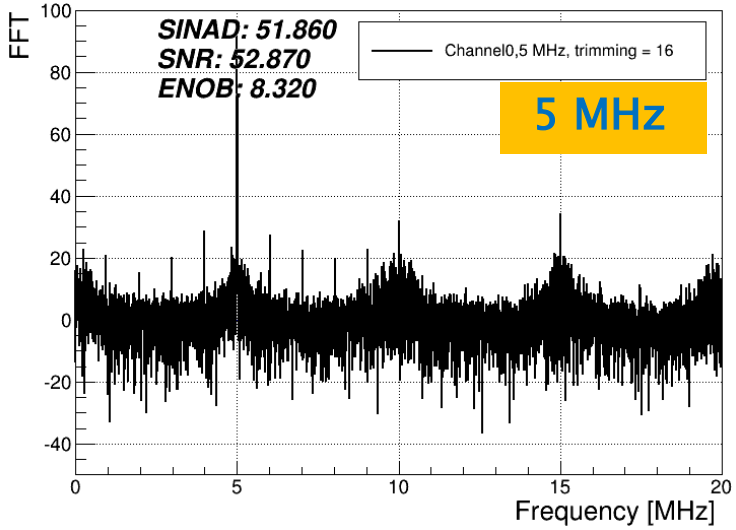
Spikes could be reduced by a better amplification before the latch comparator

Dynamic specifications

- Dynamic performance of the ADC are determined from the FFT for an incoming sinus signal: 100KHz, 1MHz and 5MHz
- These results integrate all the limitations:
  - Reduce dynamic range
  - Spikes
  - Jitter (next slides)

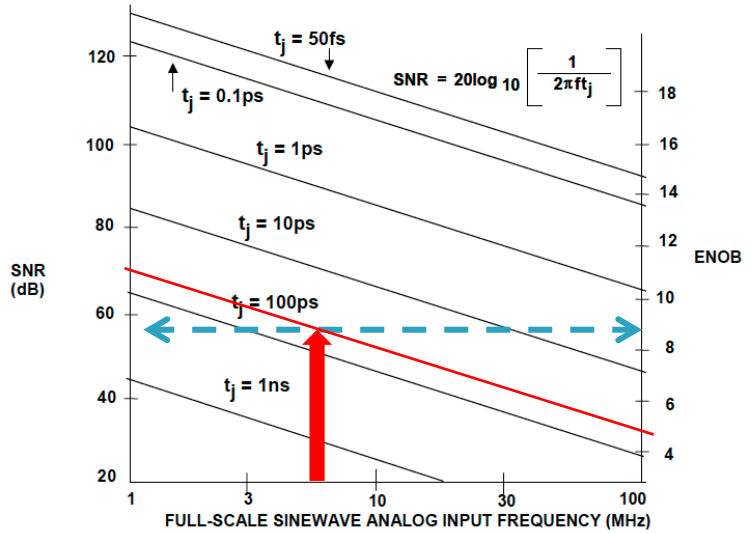




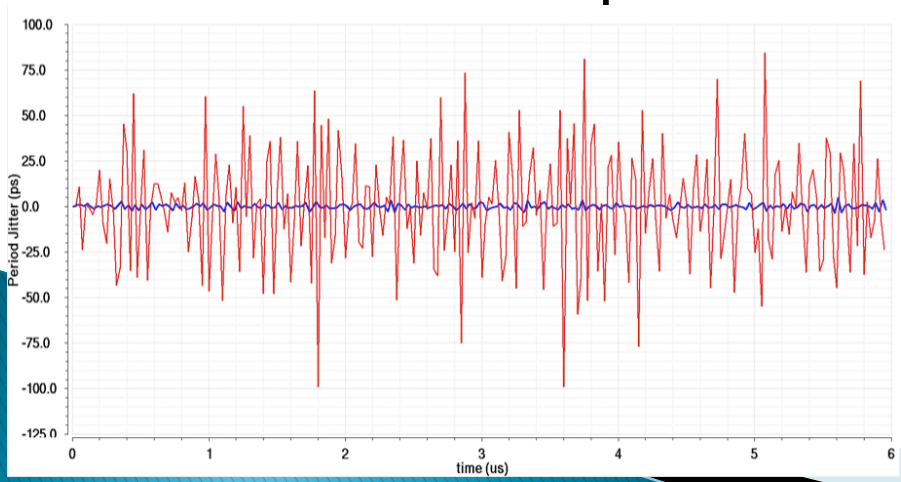


ENOB: Source & Solutions

- Source of ENOB reduction
  - ➔ sampling clock jitter
    - 1 to10 ps jitter is needed to reach expectations
    - Simulation studies of 2nd prototype:
      - RMS jitter **30 ps** or ±100 ps peak to peak
- Solution:
  - Modifying the architecture of the sampling pulse generator inside the chip



Theoretical limitations as a function of jitter



Present problem for jitter
New jitter simulated

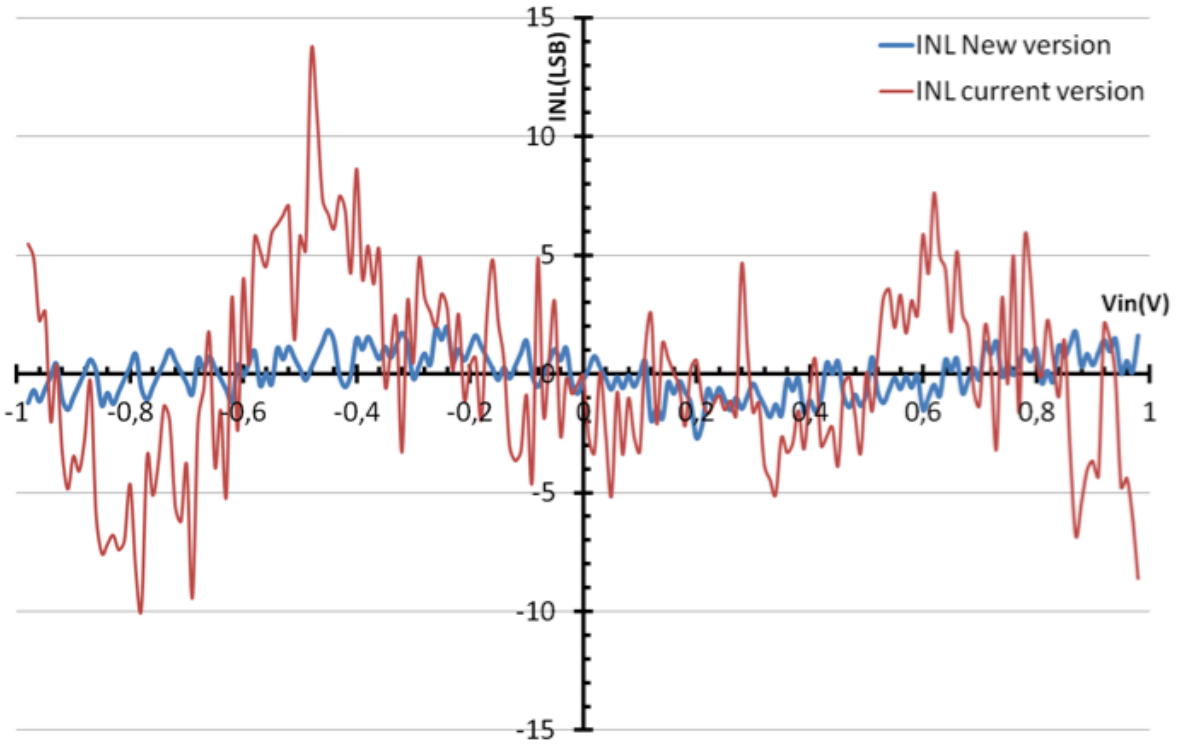
Crosstalk measurement

- To determine the crosstalk between the ADC channels, a 1 and 5 MHz full scale sine-wave was applied to channel 1 while all the others (0, 2 and 3) are grounded

	$F_{in\ CH1}$	1 – 0	1 – 2	1 – 3
Crosstalk (dB)	1 MHz	– 78.9	–76.7	–86.1
	5 MHz	–66.7	–69	–77.2

INL simulation

- New prototype with all improvement:
  - Reference voltage
  - Segmented Cap.
  - Jitter
  - Spikes



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    - PEALL chips
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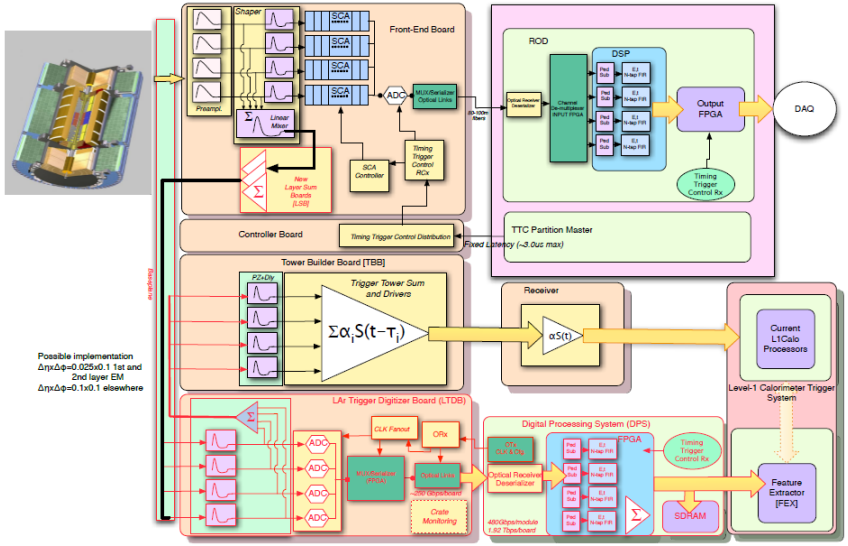
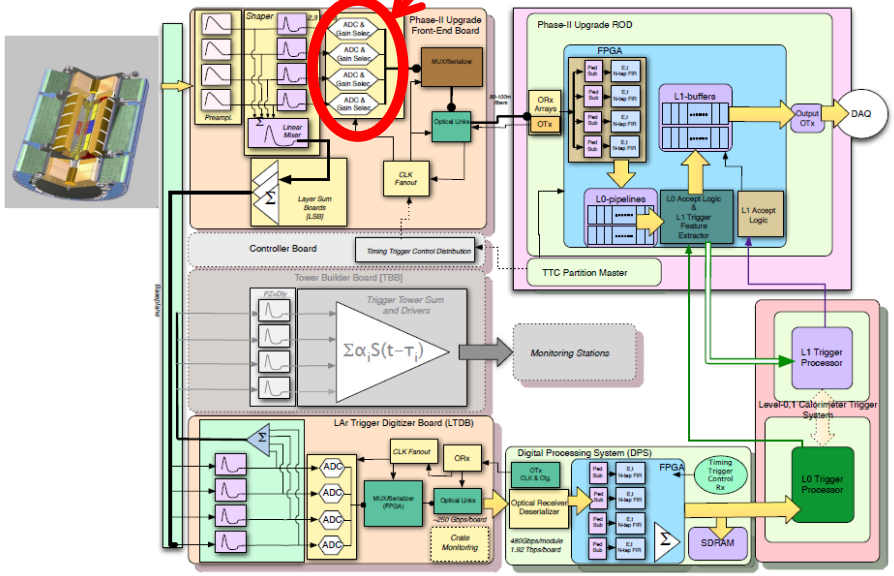
  - Ramp ADC

ATLAS-Larg: Phase-II



40MSPS, 12b
Low power
+ Gain selector

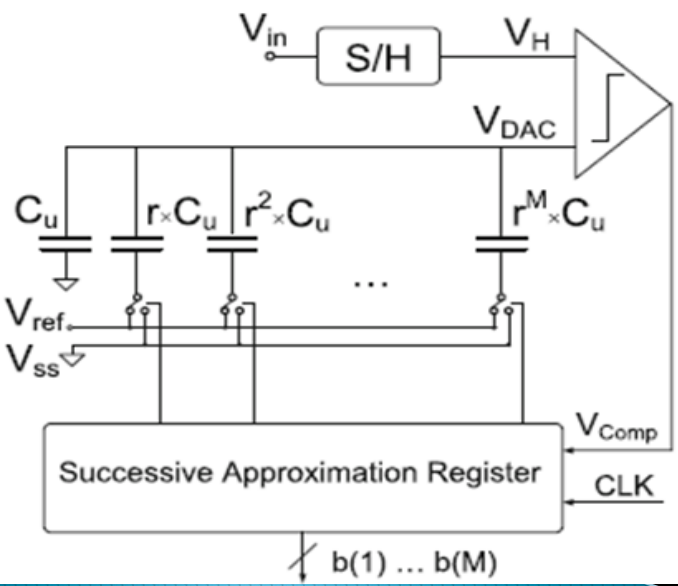


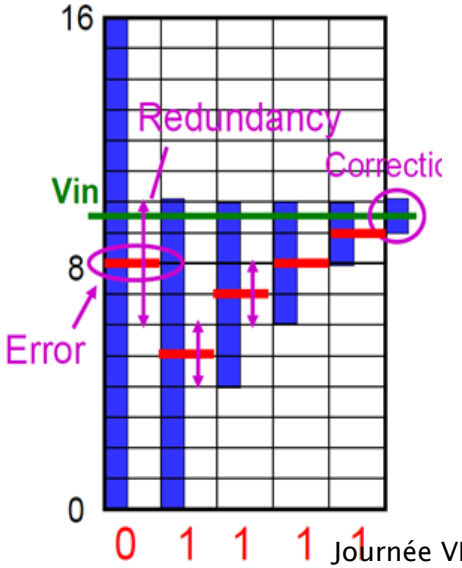
New SAR development

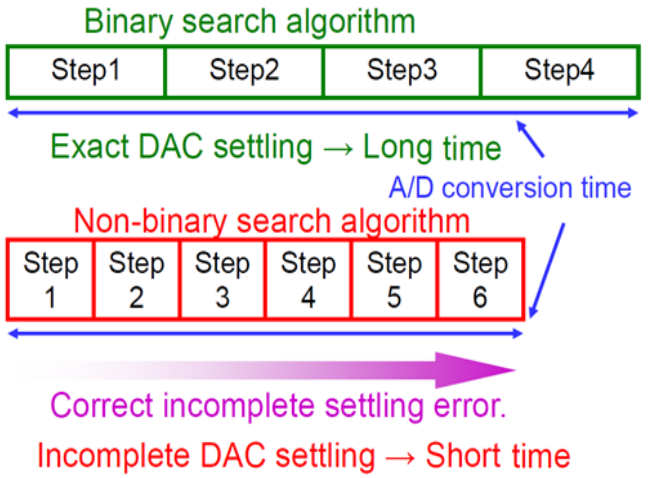
- Binary search is sensitive to intermediate errors made during search:
  - Comparator offset must be constant
  - DAC must settle into ±½ LSB bound within the time allowed (T_{clk} /2)
    - Conversion speed is limited
    - The consumption of the V_{ref} buffers is high
- **Solution:** Non-binary search algorithm can be used => **redundancy**
- CMOS130/CMOS 65nm

SAR with redundancy

- By using overlapped search range:
  - Redundancy increases the tolerance to errors
  - Redundancy helps to reduce the settling time
    - The power consumption of the V_{ref} buffers is reduced
  - Possibility to calibrate the capacitor mismatch
- Algorithm based on a radix $r=2^{N/M}$

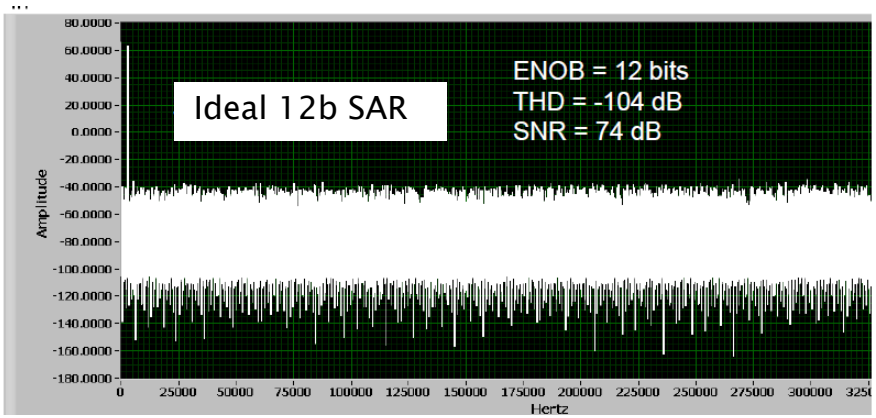


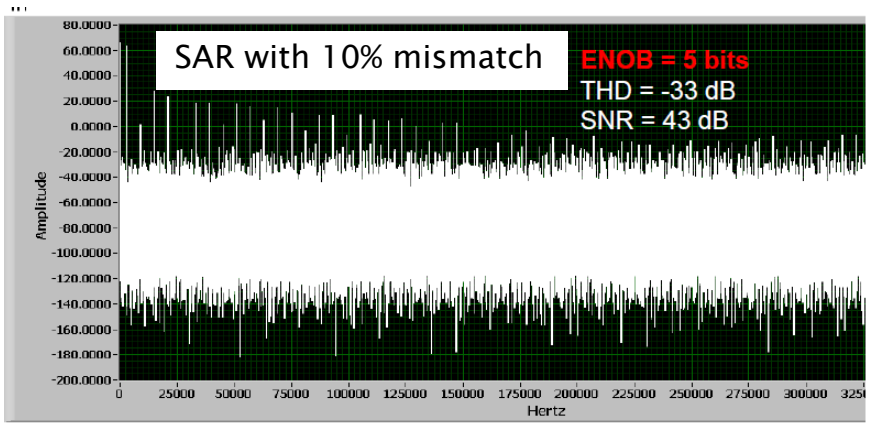


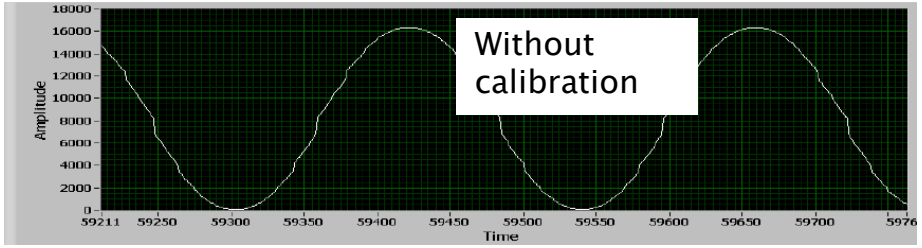


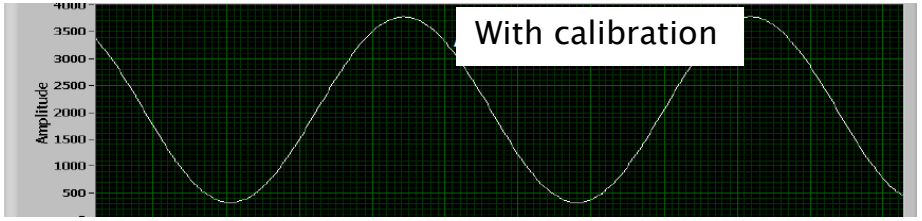
Robustness for redundancy SAR

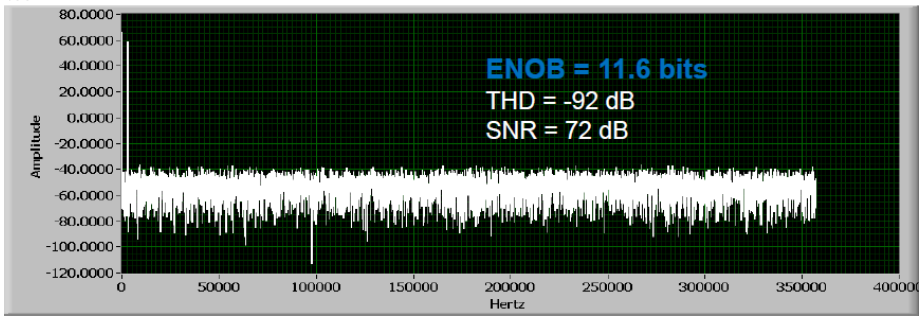
- Binary search vs redundancy architecture











Conclusions

- SAR architecture is a challenging but a good choice, fully compatible with easy scaling to 65nm
- We positively reach the 40MSPS with V_{ref} fully embedded
- This asynchronous 12 bits 40MSPS is a record
- The latency time, power & chip area are optimal
- Minor problems identified and ***solutions found***
- Plans for phase 2 with **a redundancy version** and digital correction

Outline

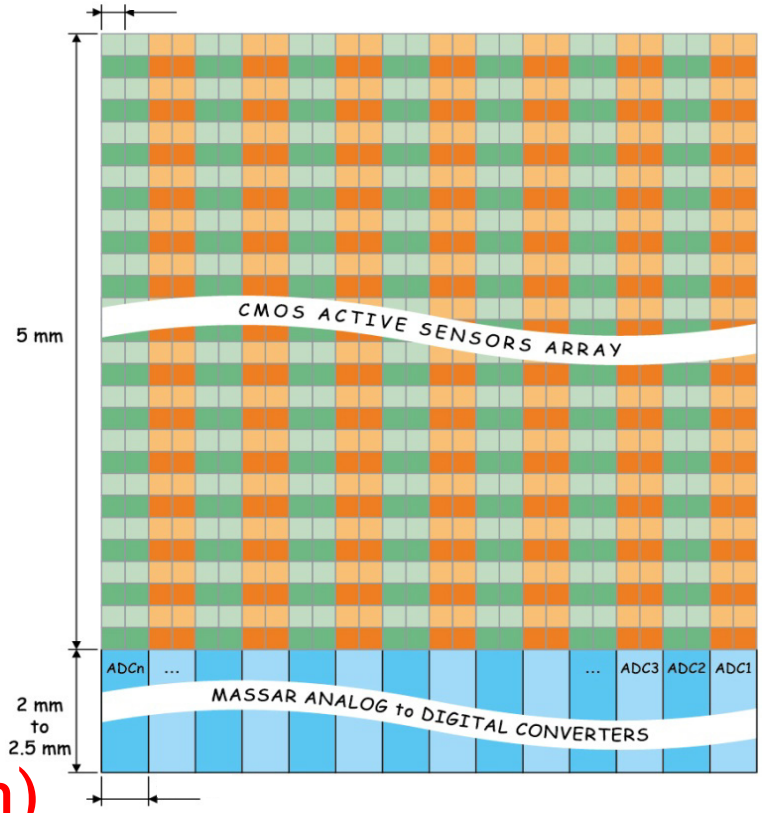
- Physic experiments:
  - ATLAS-Larg: Phase-I
    - PEALL chips
  - ATLAS-Larg: Phase-II
    - New SAR Architecture
- Imaging Read-Out chip:
  - MASSAR
  - Ramp ADC

Application

- Gravit
- New patent SAR architecture
- IR, bolometer, X-ray
- Medical application

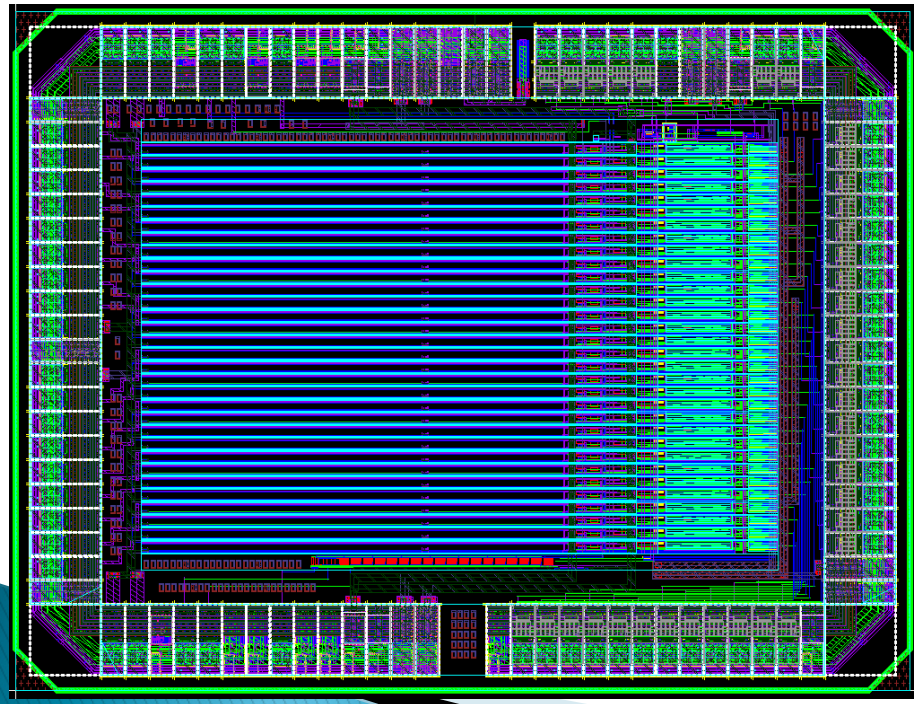
MASSAR Prototype

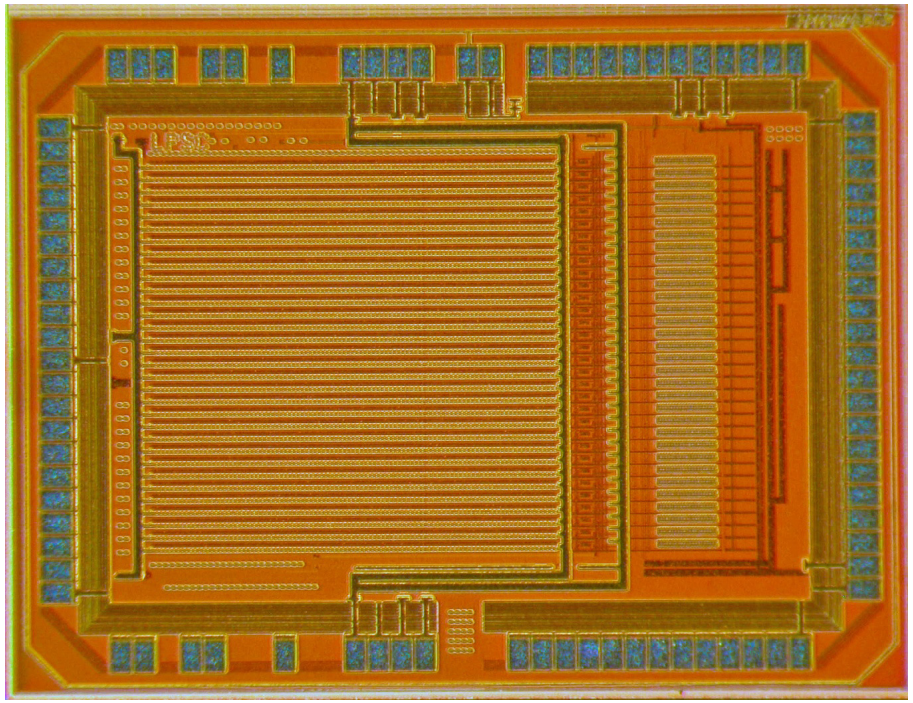
- Converters array based on a new SAR architecture
- 14 bit resolution
- Speed of .5MSPS/column
- CIN ≈3pF
- Power Consumption:
  - <500µW/column
- CMOS 130nm
  - Analog power supply: 1.5V
  - Digital power supply: 1.2V
- Pitch: 30µm (length <2mm)



MASSAR Chip

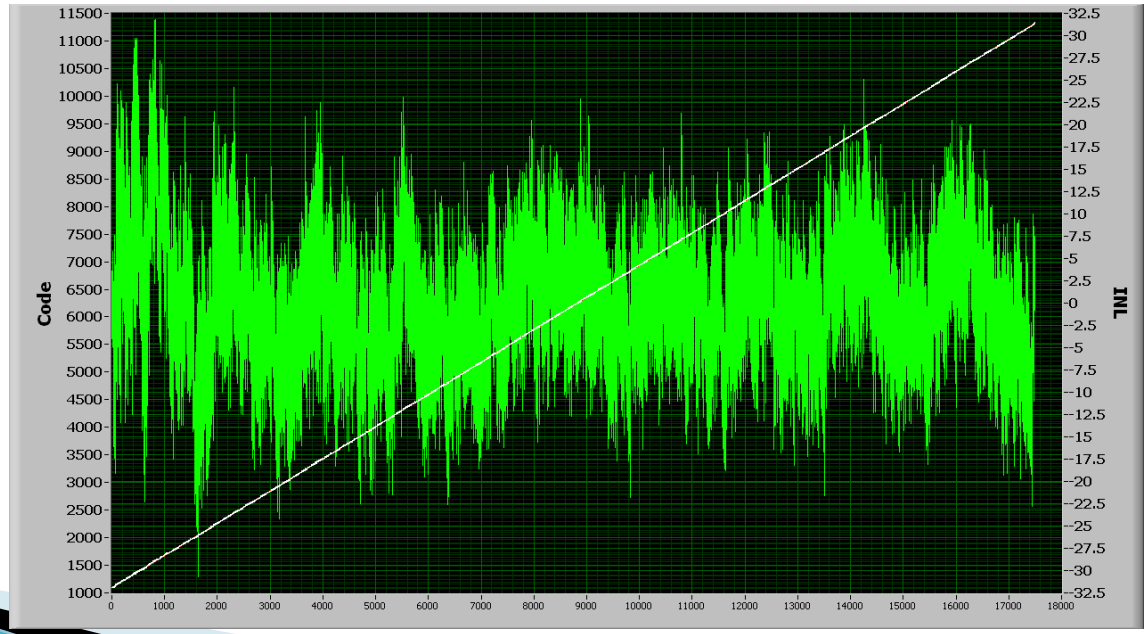
- Pitch about 30µm x 1.93mm
  - Chip: 2.7 x 2.06 mm^2
- Digital serial outputs





MASSAR: DC testing results

- Noise superimposed to the nonlinearity
  - Linearity about ±13LSB
  - Improvement by integrating Ref. voltages



Outline

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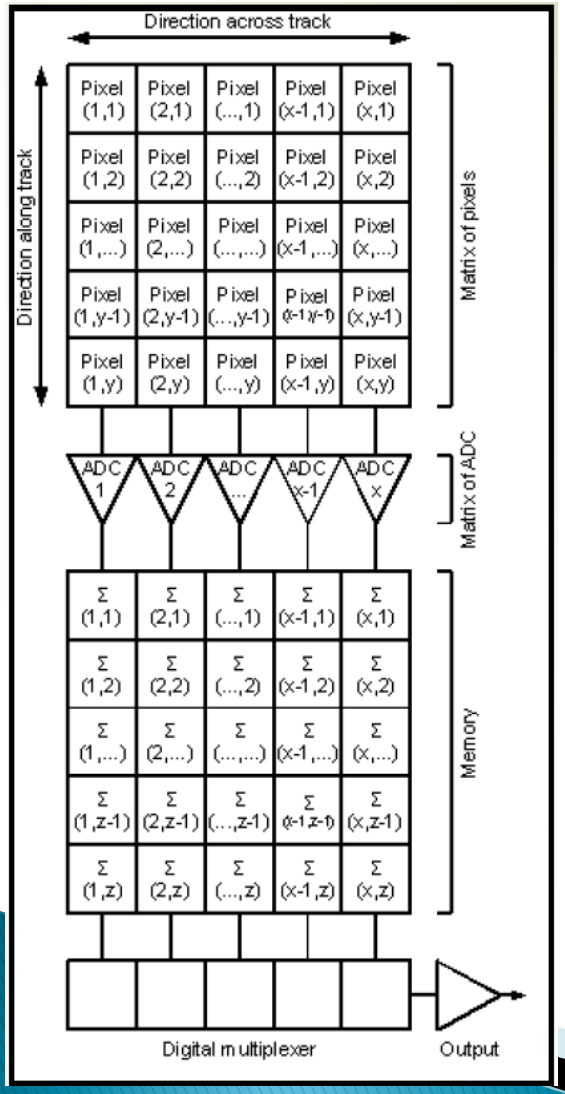
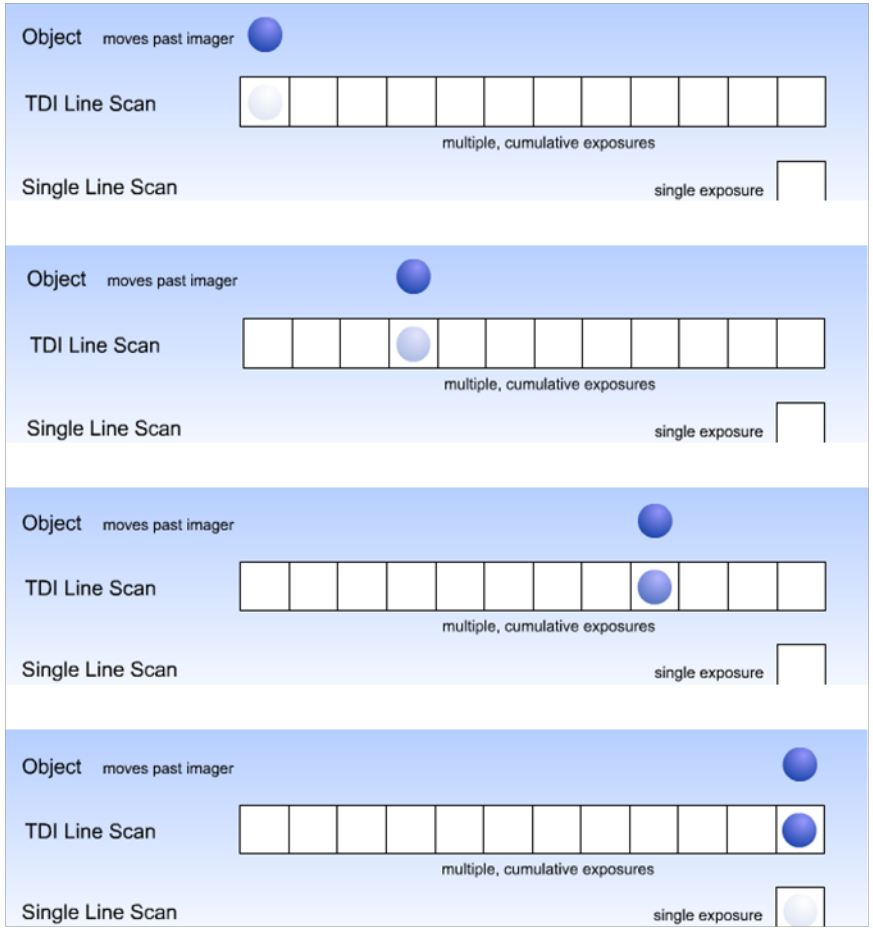
“High-Speed” ramp ADC

- TDI: Technology that captures the image of a moving object with high speed and high sensitivity (HAMAMATSU©)
- TDI imaging with CMOS image sensors
  - Time Delayed Integration or TDI imaging is used to image moving objects
  - Implementations in CMOS have traditionally been difficult because of the lack of a charge addition circuit
- Applied in earth observation instruments

TDI architecture



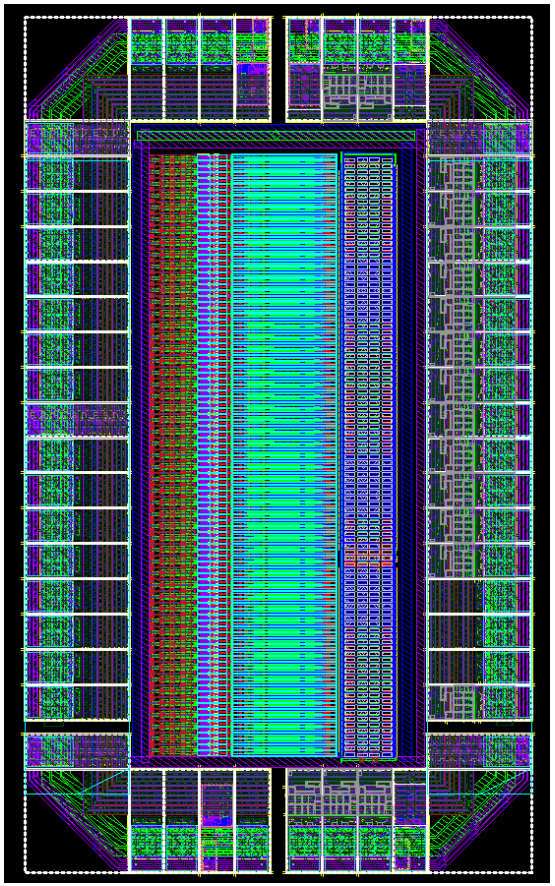
Digital Integration (Accumulation/ Summation)



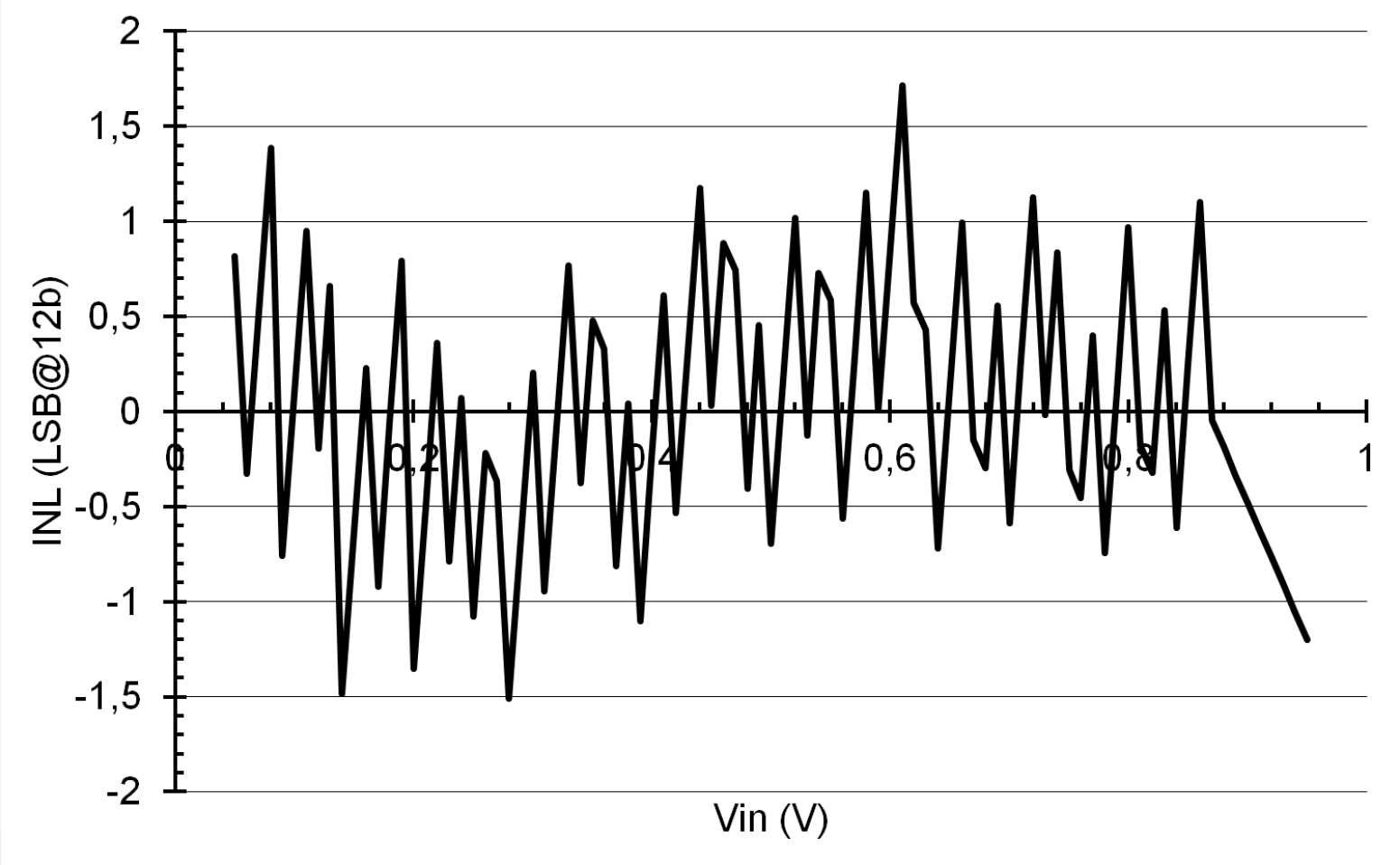
TDI imagers combine multiple exposures synchronized with object motion

“High-Speed” ramp ADC

- Spatial applications (Time Delay Integrator)
- 12b ADC
- 250ksps
- 10µm pitch
- 250µW/ch
- CMOS 130nm
- 100 channels (1st prototype)



Ramp ADC: INL simulation



LPSC Grenoble
Laboratoire de Physique Subatomique et de Cosmologie

Thank you for your attention

Questions?