The application of Silvaco process and device simulation program to the development of silicon detector for the high energy particle detection

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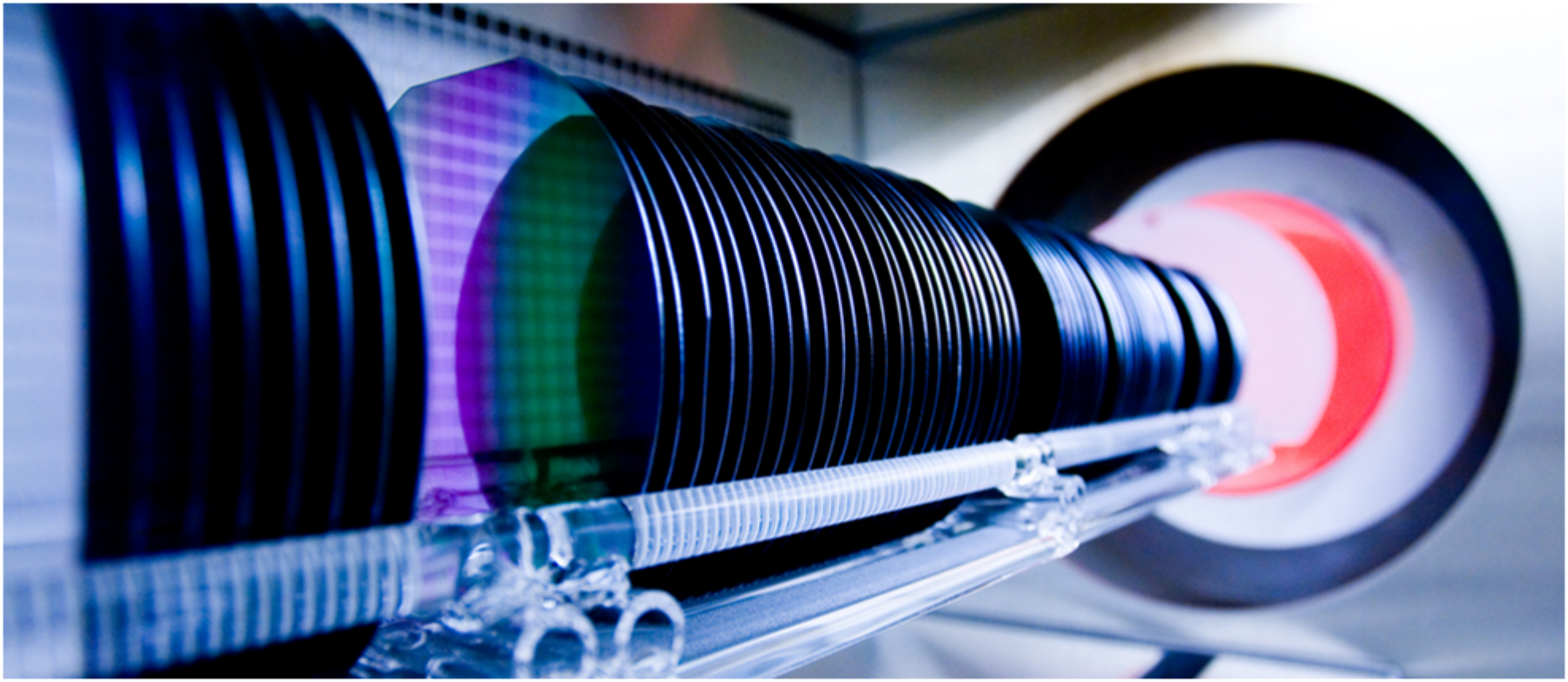
für **Mikrosensorik**
und **Photovoltaik** GmbH



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General presentation of the Institute

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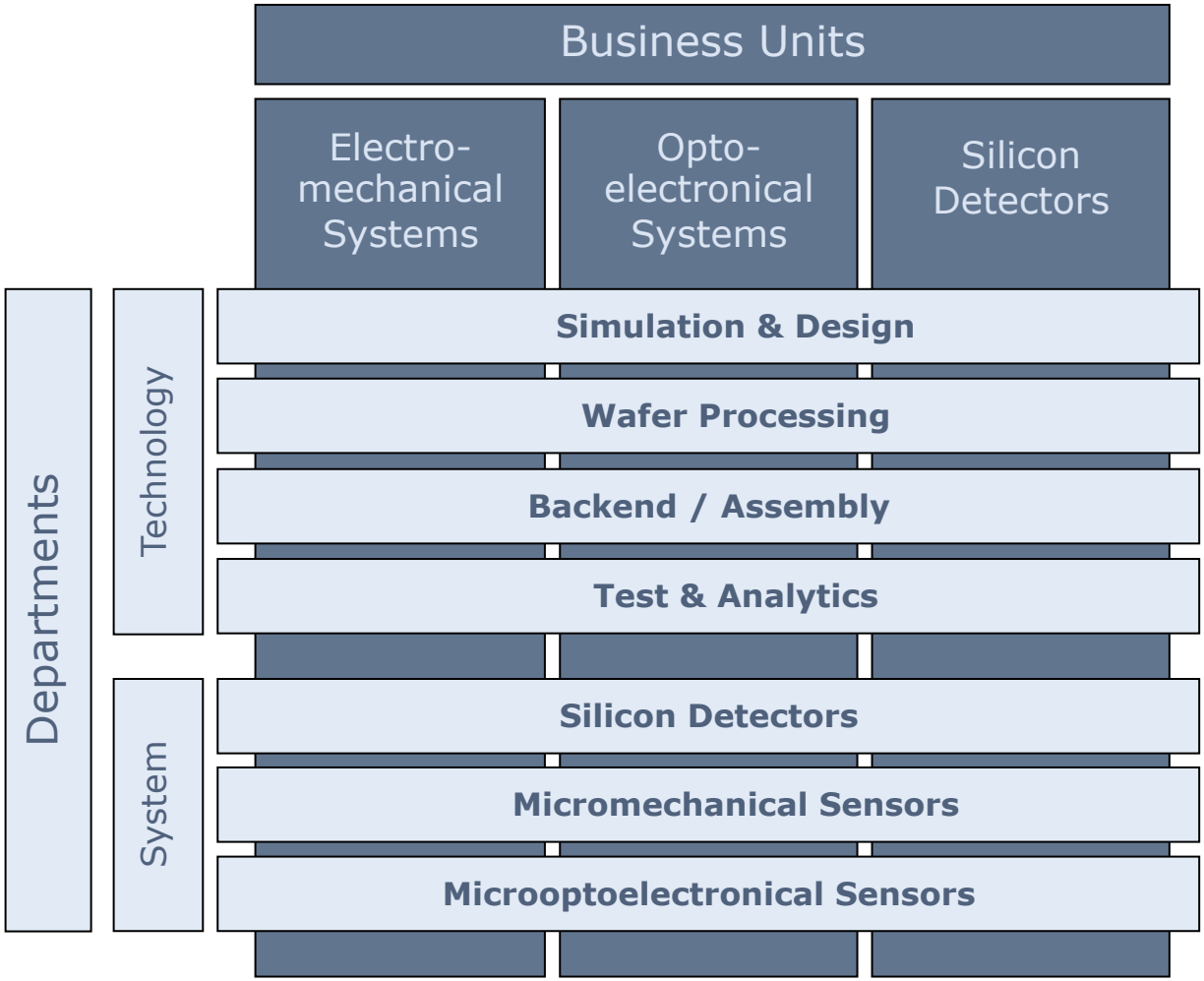
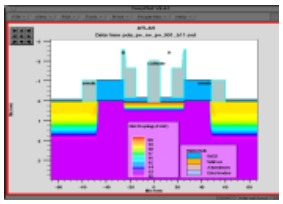
Location

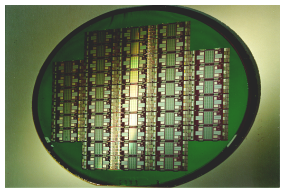


Complete technology chain for R&D and production of high-performance micro-sensor systems

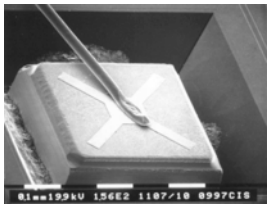


Simulation and design

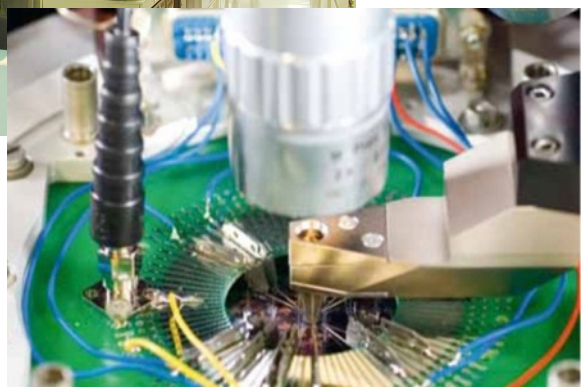
- Layout and DRC– Layed, ICED, Tanner
-FEM-Simulation tools for electrical,
  mechanical and thermal properties ANSYS, COMSOL
-Silvaco program for semiconductor simulation
 Athena 5.21.2.R,ATLAS 5.19.20.R
- SPICE-Simulations (HSPICE, CADENCE pSPICE)

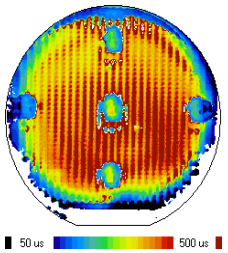


Wafer technology



Assembly and packaging





Device characterization and analysis

Certified QM System DIN EN ISO 9001

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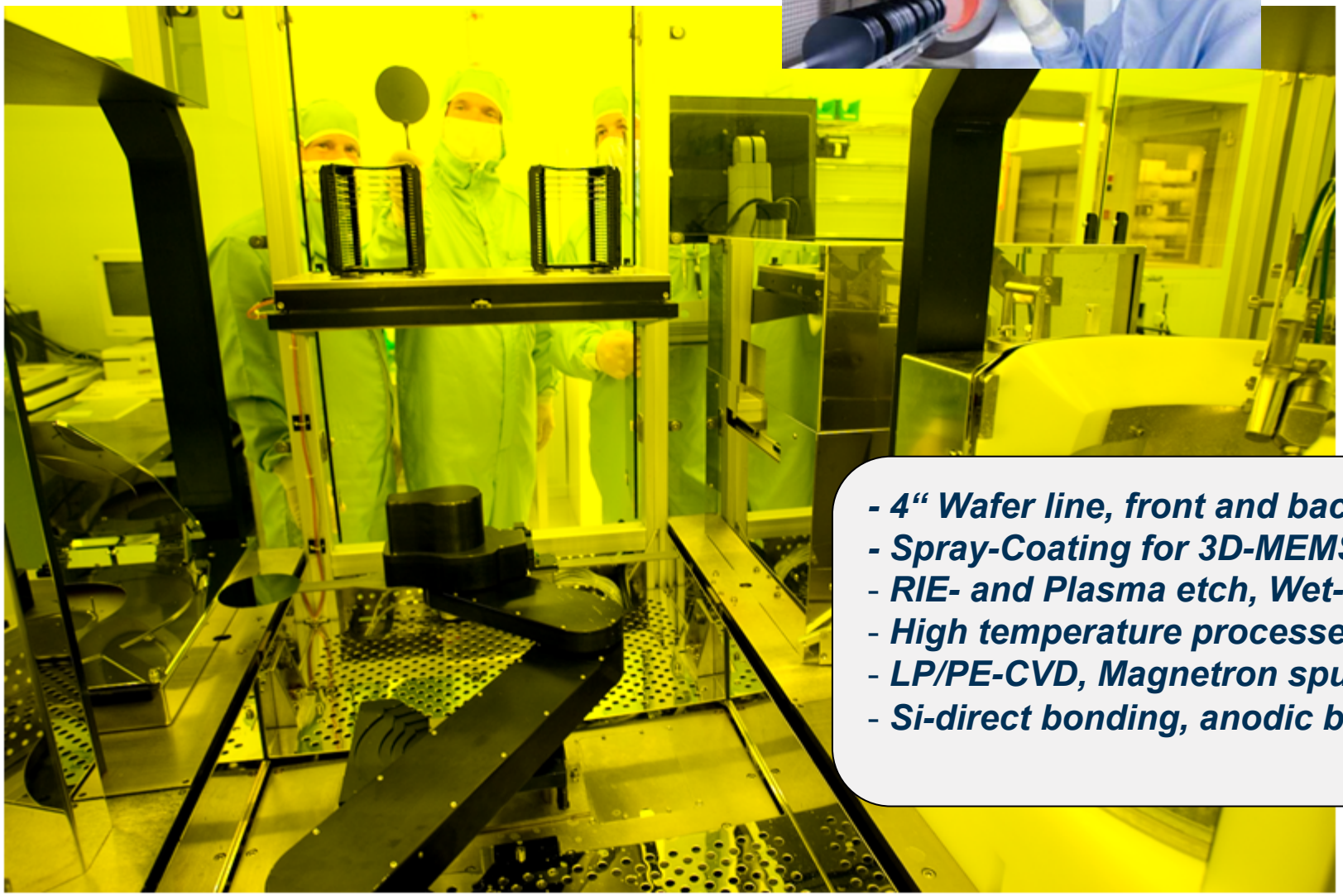
Wafer processing

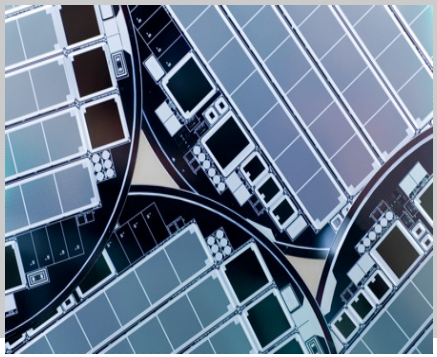


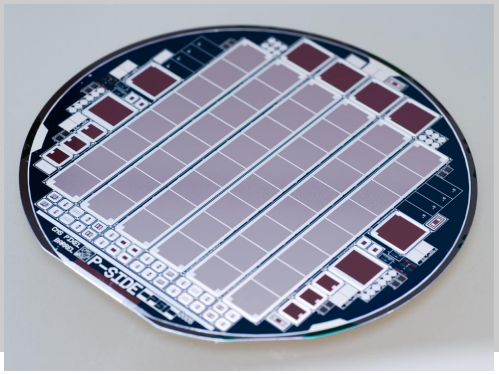
Structuring by using UV-Photolithography <1um

- 4“ Wafer line, front and backside processing,
- Spray-Coating for 3D-MEMS/MOEMS
- RIE- and Plasma etch, Wet-Bench
- High temperature processes
- LP/PE-CVD, Magnetron sputtering
- Si-direct bonding, anodic bonding

Radiation- and Particle-Detectors for HEP

- Micro-strip detectors
- Micro-pixel detectors
- X-Ray detectors
- Beta ray detectors
- Ion detectors
- Silicon photomultiplier
- HV CMOS detectors





Silicon detectors for HEP

Silicon detectors for particle detection

1. High granularity: high spatial resolution, micro strip, pixel, single or double sided
2. Big sensitive volume: full depletion
3. Low mass: thin substrate
4. Small dead area: edge region should be small
5. Low noise: low inter strip capacitance, high coupling capacitance for ac coupling
6. Good channel isolation
7. High operation voltage: sensitivity
8. Radiation hard: $10^{15}cm^{-2}$ Fluence of 1MeV equivalent neutron
9. Good CCE, MIPS pulse height distribution

Specifications

1. Low leakage current and homogenous leakage current over all channels
2. Very few hot or defect channels, dielectric pin hole, defect poly resistor or metal line
3. High breakdown voltage and no micro discharge
4. High dielectric breakdown voltage for ac coupling(double sided sensor)

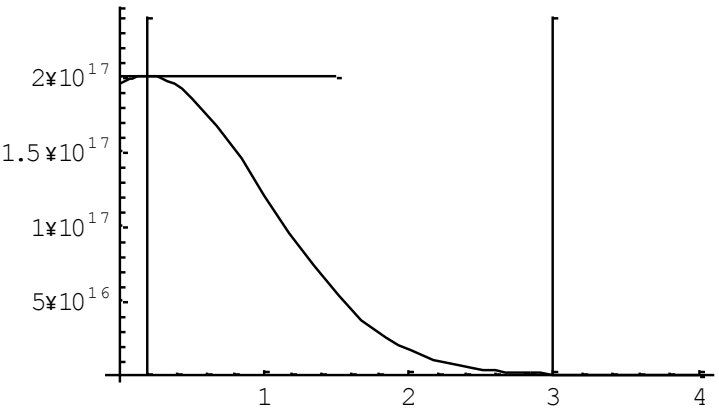
Design rules and robust design

1. Patterning size limitation and mask alignment precision: Minimal structure size, minimal structure distance and overlap
2. Statistical deviation of film growth or deposition: Safety margin of process parameters

Process simulation

Fixed positive charge in Si/SiO2 interface results in conductive channel between neighboring strips or pixels, Isolation is required.
Pspray or Pstop are used.
They have effect on interstrip resistance, capacitance breakdown voltage and CCE.

Pstop profile
peak concentration 2.0E17, peak position 0.13um, depth 2.8um.



Deckbuild Optimizer

Deckbuild: Optimizer - (NONE)

Mode Parameters e View Edit Print Optimize Properties...

Line number	Parameter name	Response type	Optimized value	Initial value	Minimum value	Maximum value
5	set ozthick	linear	0.149743	0.15	0.075	0.225
6	set pdose	log	1.5776e+13	5e12	5e+11	5e+13
7	set penergy	linear	130.271	130	65	195
34	set time0	linear	44.241	30	15	45
35	set temp0	linear	1100	1100	550	1650

Deckbuild: Optimizer - (NONE)

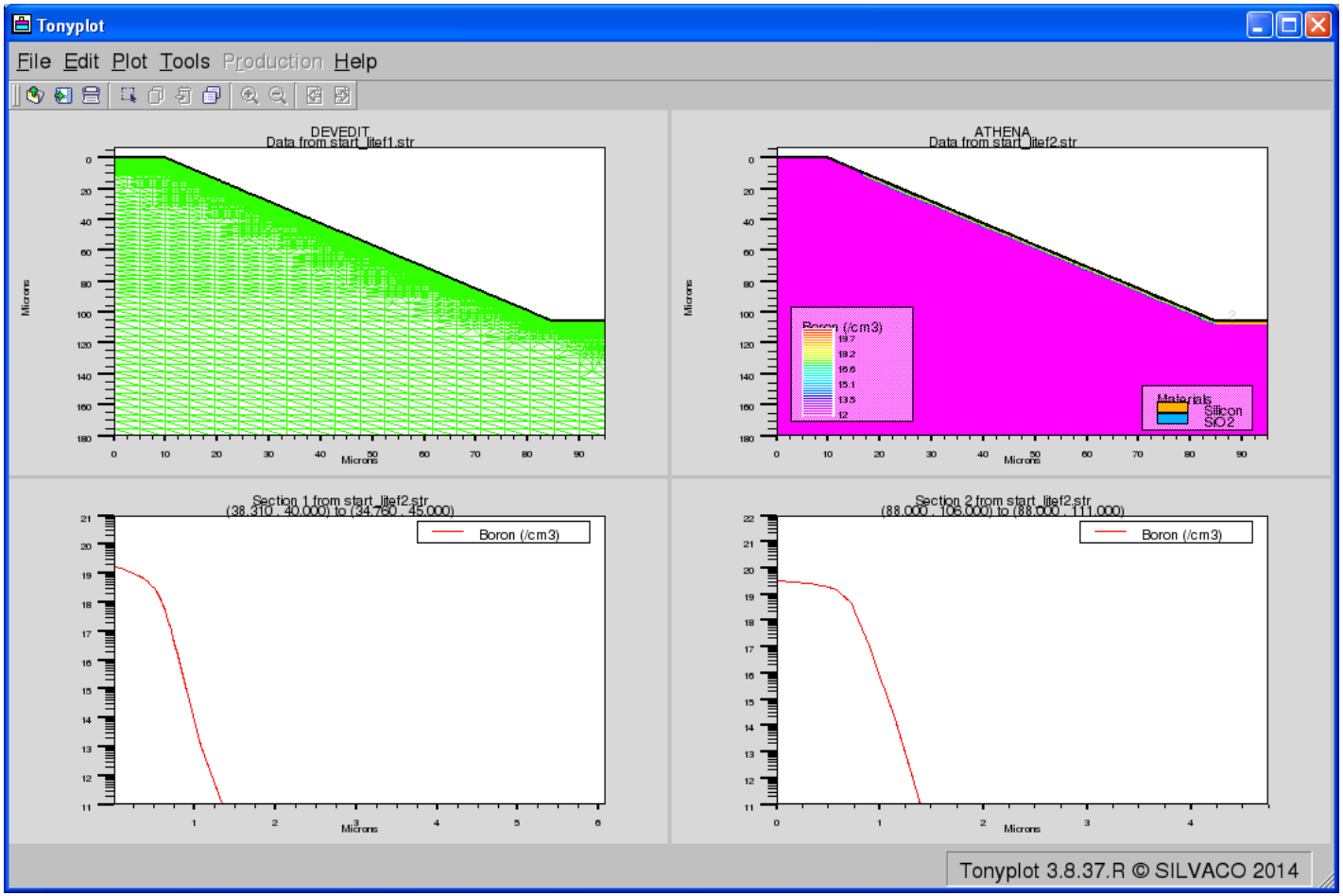
Mode Targets e View Edit Print Optimize Properties...

Line number	Target name	Target type	X value	Target value	Optimized value	Error (%)	Weight
138	j1 depth	linear	---	2.8	2.80998	0.356544	1.0
139	j1 max.c	linear	---	2e17	2.00508e+17	0.254169	1.0
140	j1 peak	linear	---	0.13	0.129845	-0.119002	1.0

Process simulation

Ion implant on KOH etched cavity

1. Deveidt structure
2. Athena



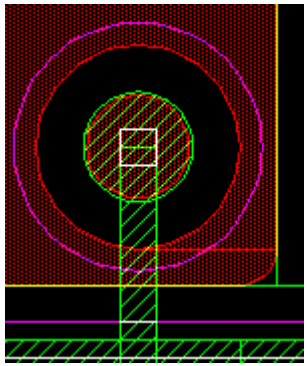

```
go athena
init infile=start_litef1.str
method fermi
deposit oxid thick=0.15 divisions=8
deposit photores thick=2 divisions=8
etch photores right p1.x=17
implant boron dose=2.0e15 energy=70 crystal
diffus time=60 temp=975 nitro press=1.00
diffus time=180 temp=975 nitro press=1.00
etch photores all
struct outfile=start_litef2.str
```

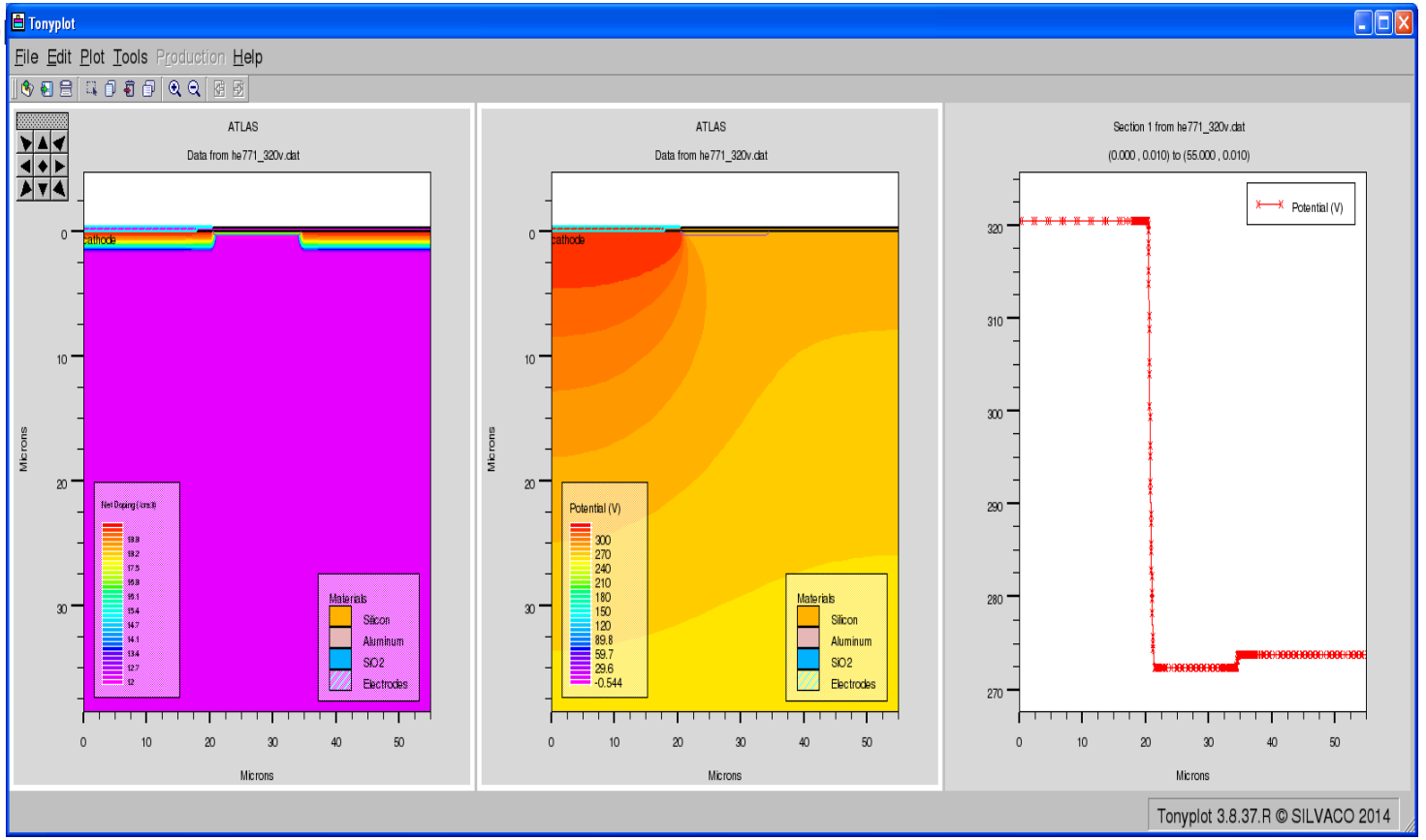
slope 5.42E14/cm2
Flat 1.65E15/cm2

Device simulation, Bias grid

One possible method to bias the sensor is the punch through, it does not need any additional mask.
It is also a protection to the dielectric against possible surging event, if poly silicon is used as biasing resistor. But the gap should be selected through simulation.
Pixel detector need biasing fo

Bias grid dots design for n-in-n pixel test. In the following results we use:
doping 1E12cm^{-3}
oxide charge qf=1E10cm^{-2}
lifetime1E-4s



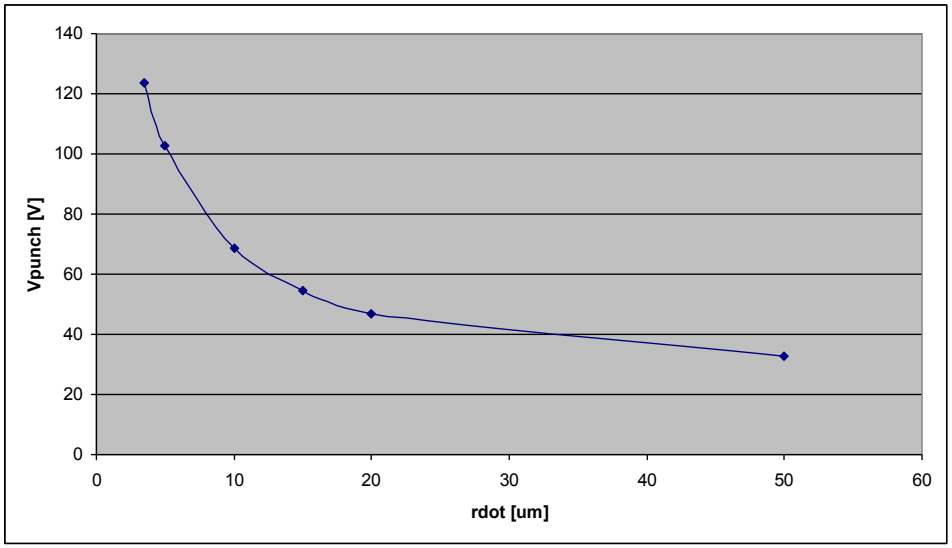


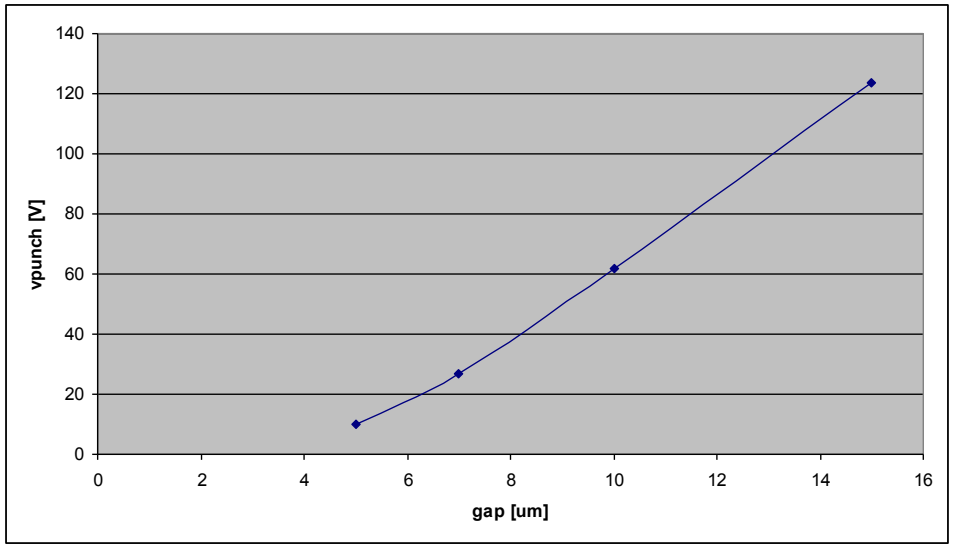
The Doping profile and potential distribution for biasing 320V. Vpunch is voltage difference.

Bias grid

The punch through voltage vs. Implant dot radius (rdot) for gap=15um left plot,

The punch through voltage vs. implant separation (gap) for rdot=3.5um right plot.
Pspray available, bias 320V .





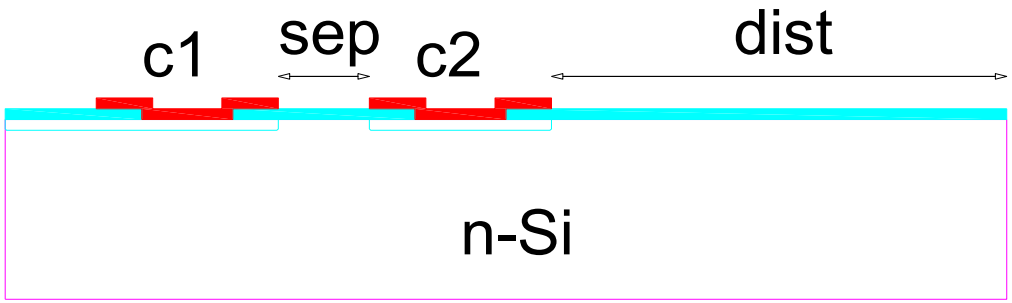
Big radius and small gap lead to smaller vpunch.

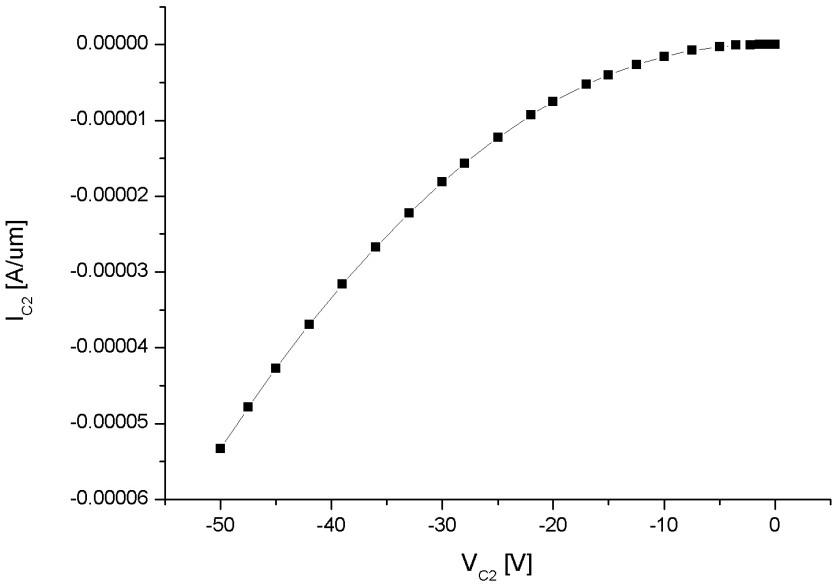
Punch through

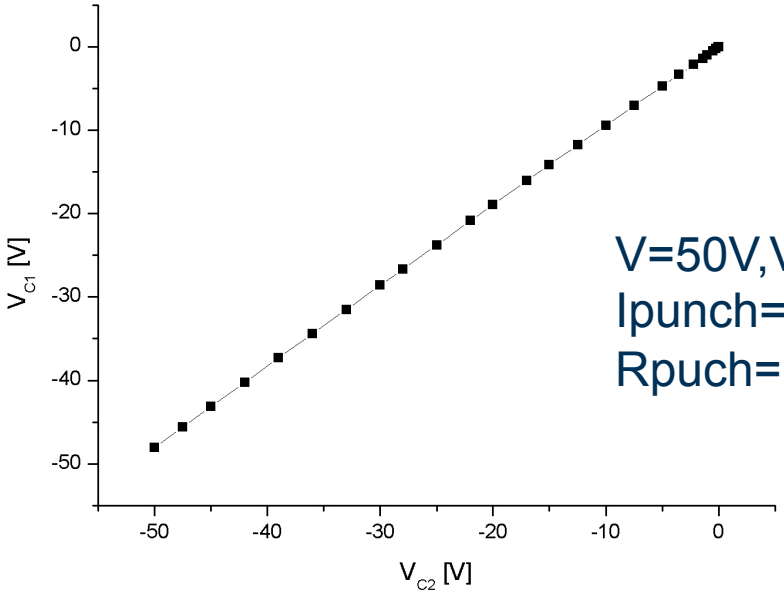
Punch through resistance for p-in-n strip detector
c2 models the bias ring and c1 the strip.
The gap between this two is denoted as sep.
c1 length=150 c2 length=50 sep variable dist=100.

1. Substrate floating c1 grounding ic2~vc2
2. Substrate grounding, c1 floating vc1~vc2

For sep=10um, V=50V the punch through current and punch through voltage vs. biasing voltage .



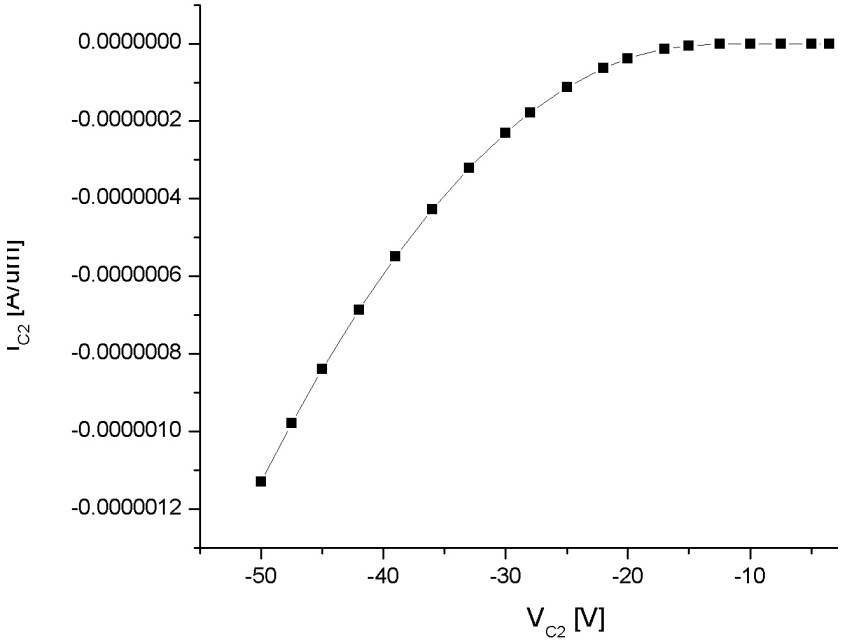


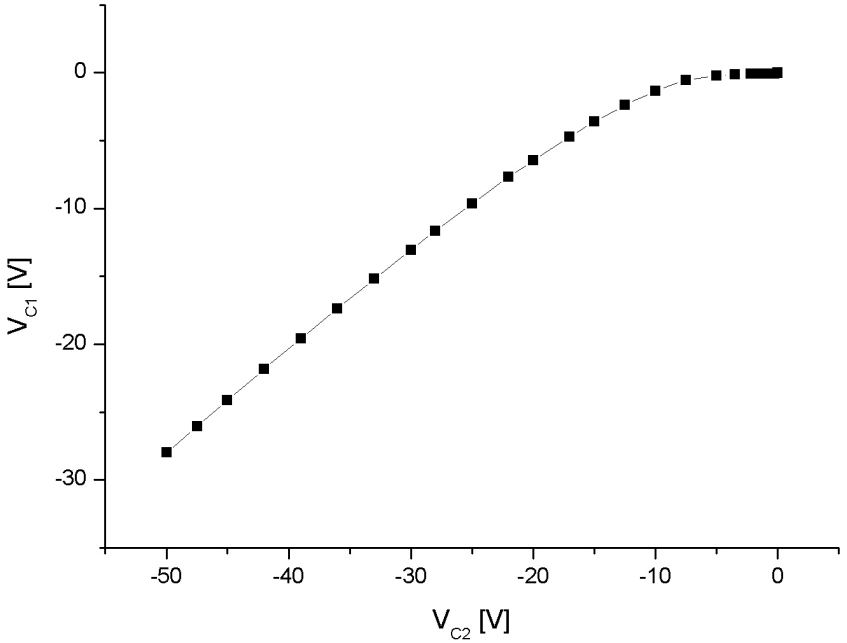


V=50V,Vpunch=1.98V
Ipunch=1.4E-8A/u
Rpuch=1.4E8Ωu

Punch through

The punch through current and punch through voltage vs. biasing voltage

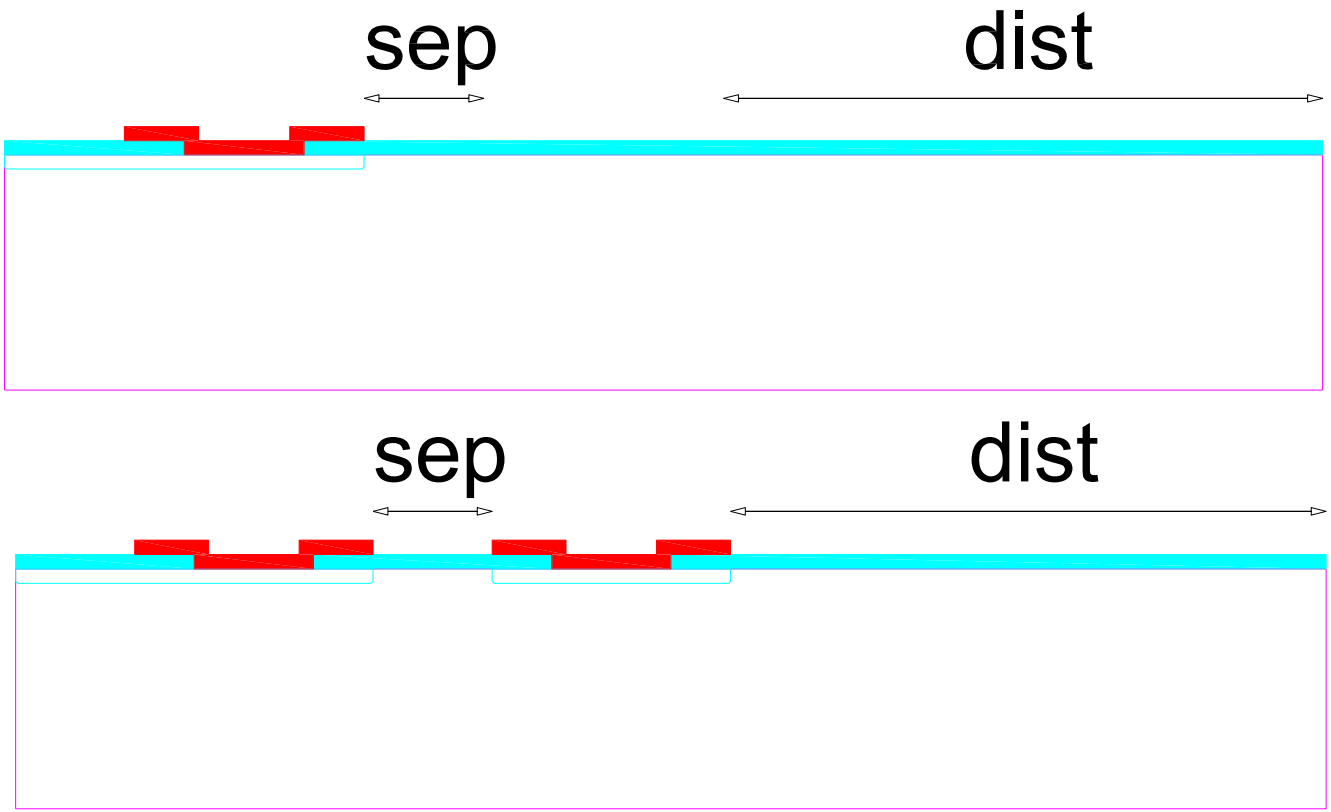




Sep=40um
V=50V,Vpunch=22.02V
Ipunch=6.29E-8A/u
Rpuch=3.5E8Ωu

Dicing edge

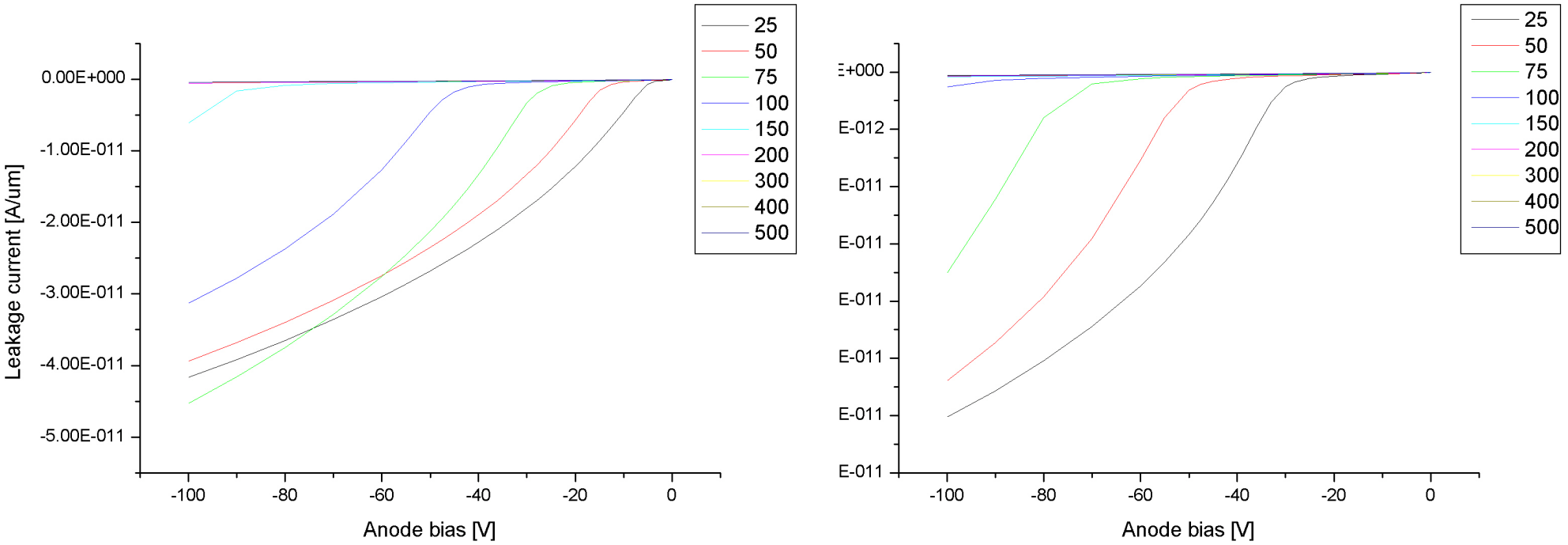
On dicing edge there are a lot of deep defects. If the space charge region touches the cutting edge the leakage current will increase rapidly. The effect of dicing edge is simulated with this modeling structure.



To compare the effect of a floating implant we use a model with and without floating implants. Dist is the distance to the dicing edge, sep=20um,strip=50um.

Dicing edge

Leakage current vs. biasing voltage for different distances



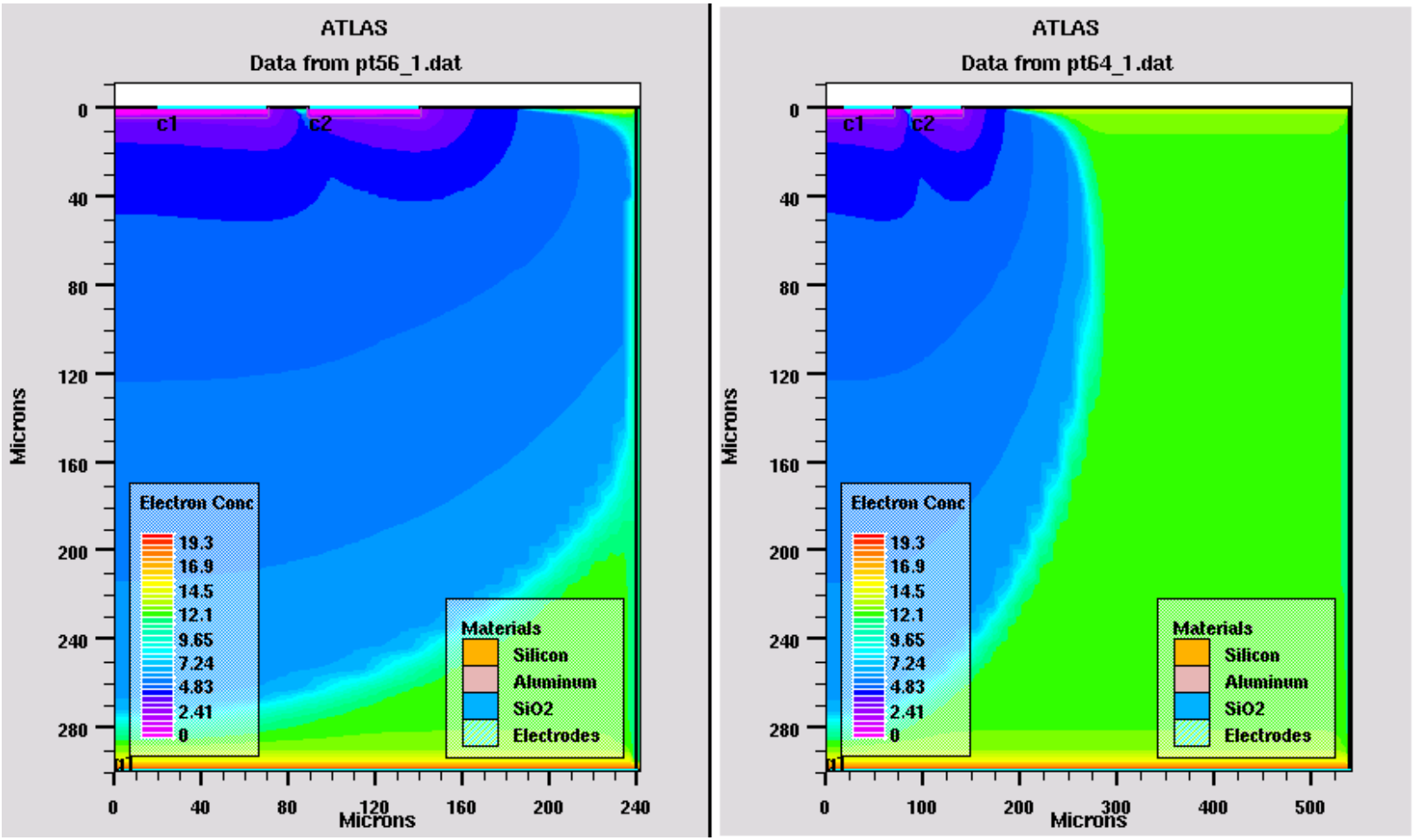
The left plot is for structure without floating implants, the right plot is for structure with floating implant. .dist are shown on legend

.Active zone too close to the dicing edge results in larger leakage, if the edge is not passivated

.Inserting a floating strip makes the required distance to the edge short.

Dicing edge

Electron concentration distribution for two distances



Distance to dicing edge 100um

Distance to dicing edge 400µm.

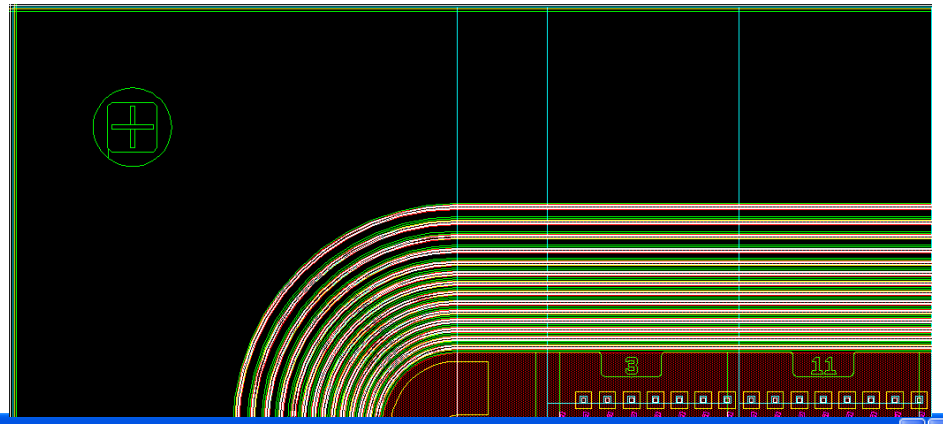
For 100µm distance the space charge region touches the edge.

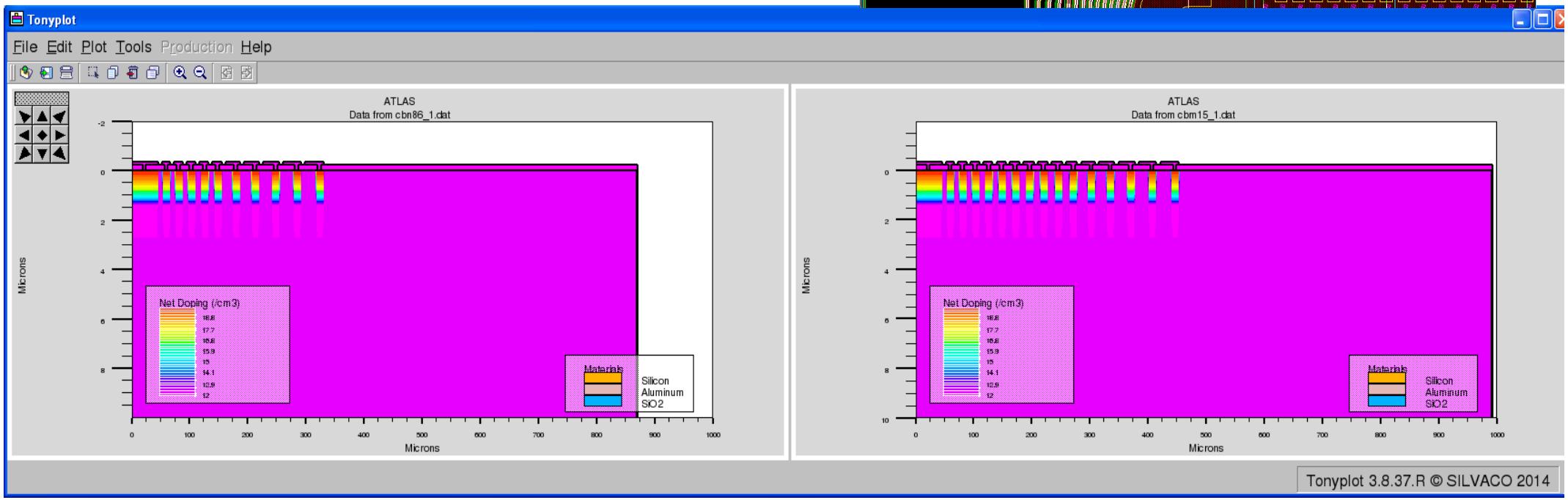
For 400µm distance the leakage current remains small.

Multi guard ring

Multi guard ring structure is designed to relax the elecrtric field on strip edge and to limit the space charge region.
This structure reforms the potential distribution around the implant edge, so that field strength peak is reduced.

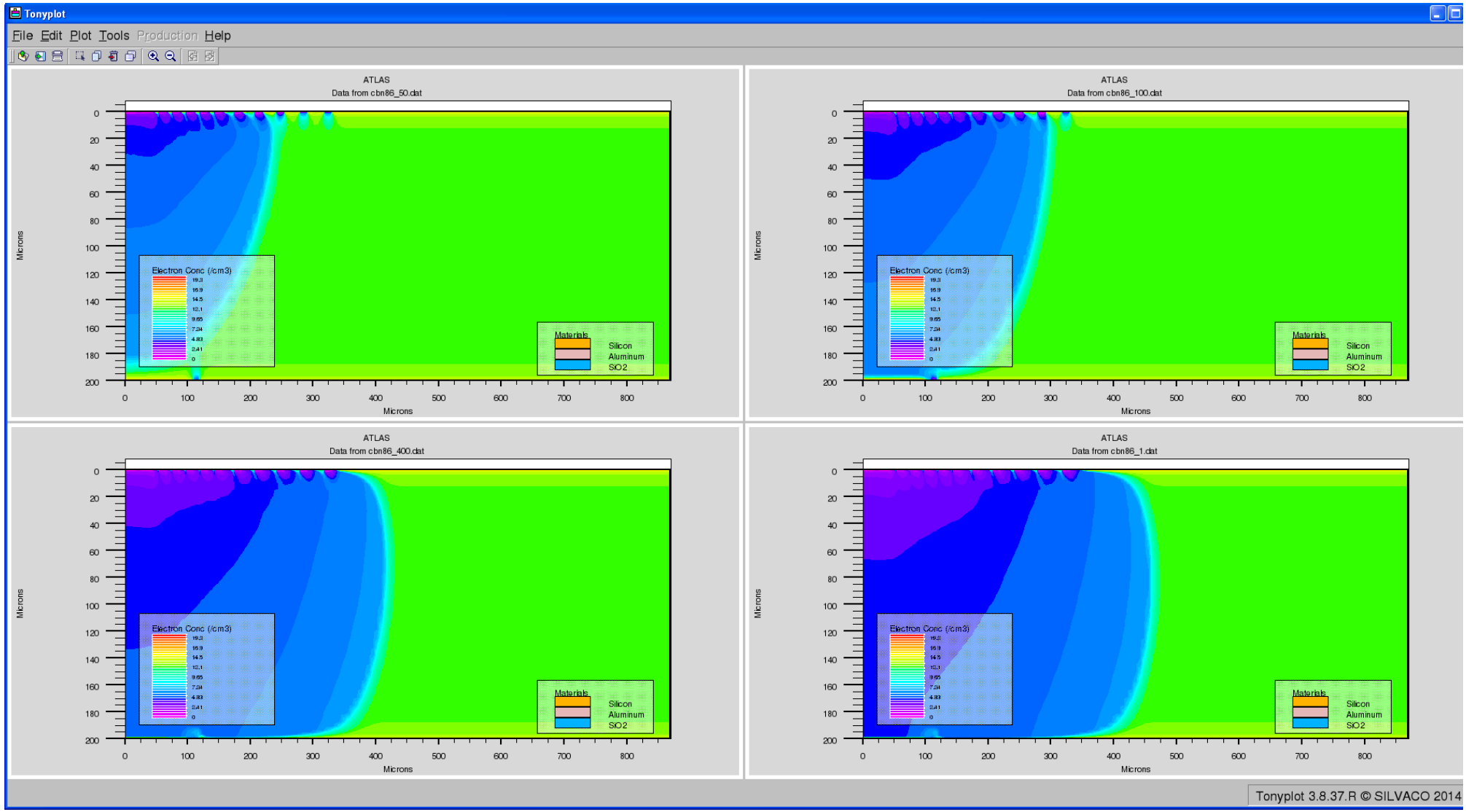
Two guard ring structures 10 rings and 15 rings





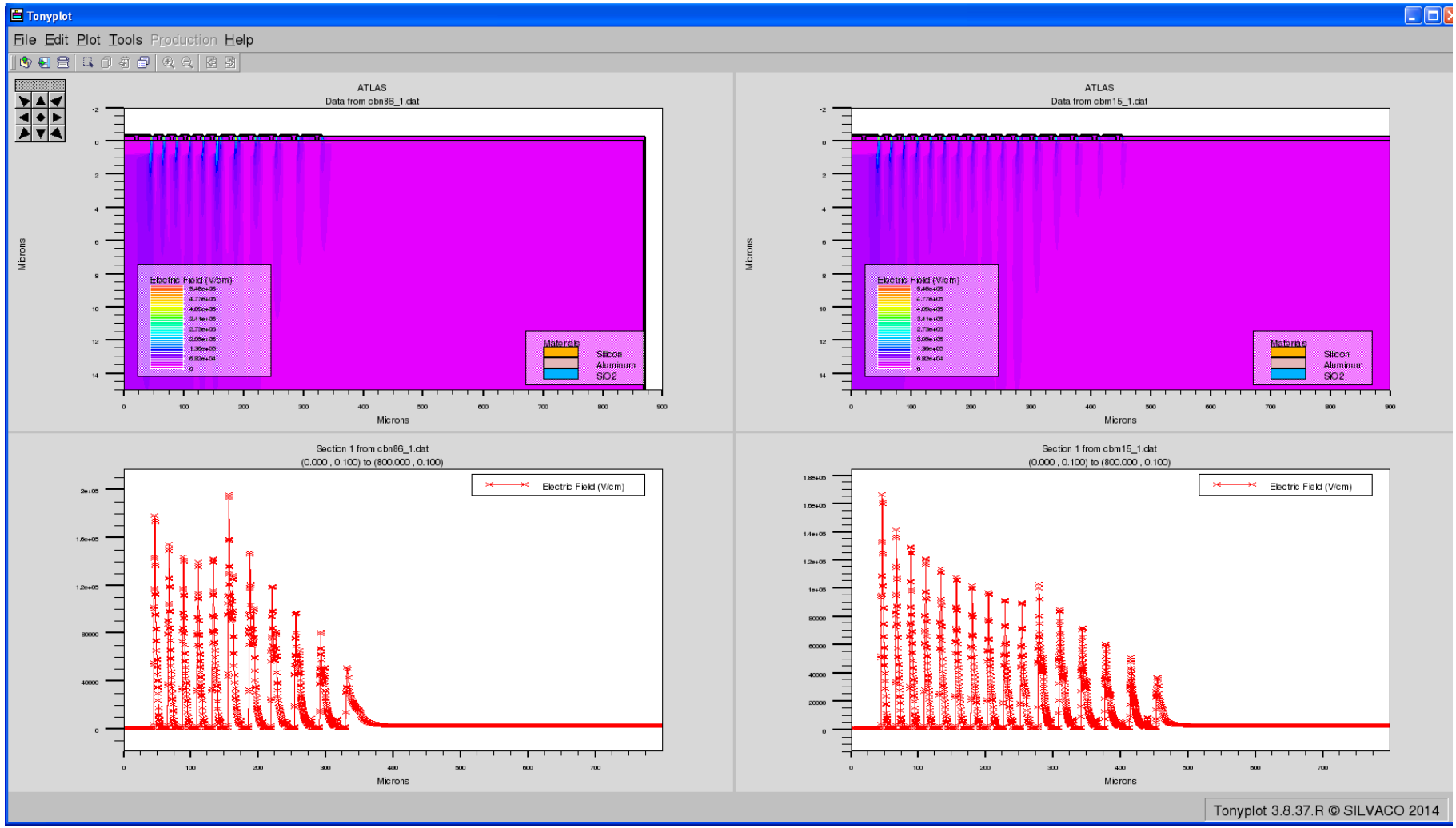
Multi guard ring

The electron concentration distribution for biasing of 50, 100, 400, 1000v for 10 rings



Multi guard ring

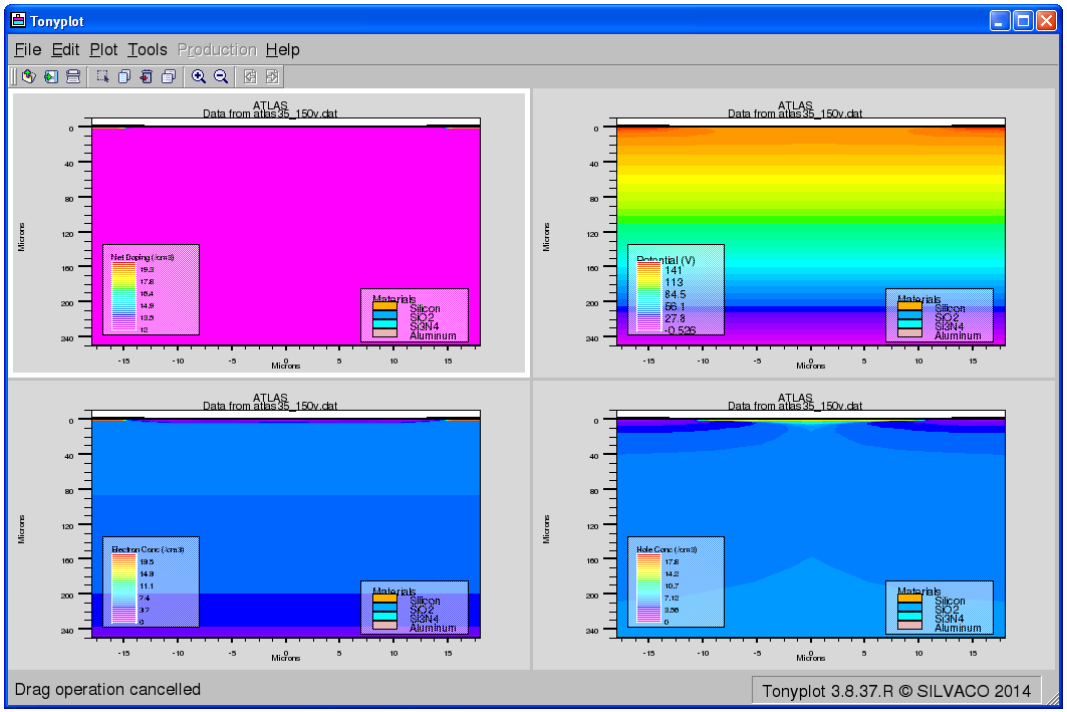
The electric field distribution by 1000V for 10 rings and 15 rings guard ring structures

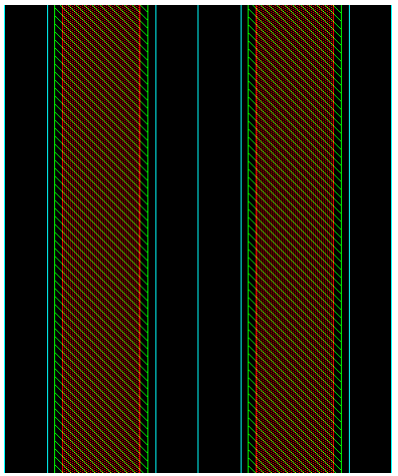


Guard ring with 15 rings has smaller field peak.
Strongly mesh dependent.

Inter strip isolation

N-in-p microstrip silicon sensor of gap=30um, with pspray dose 3.5E12/cm2

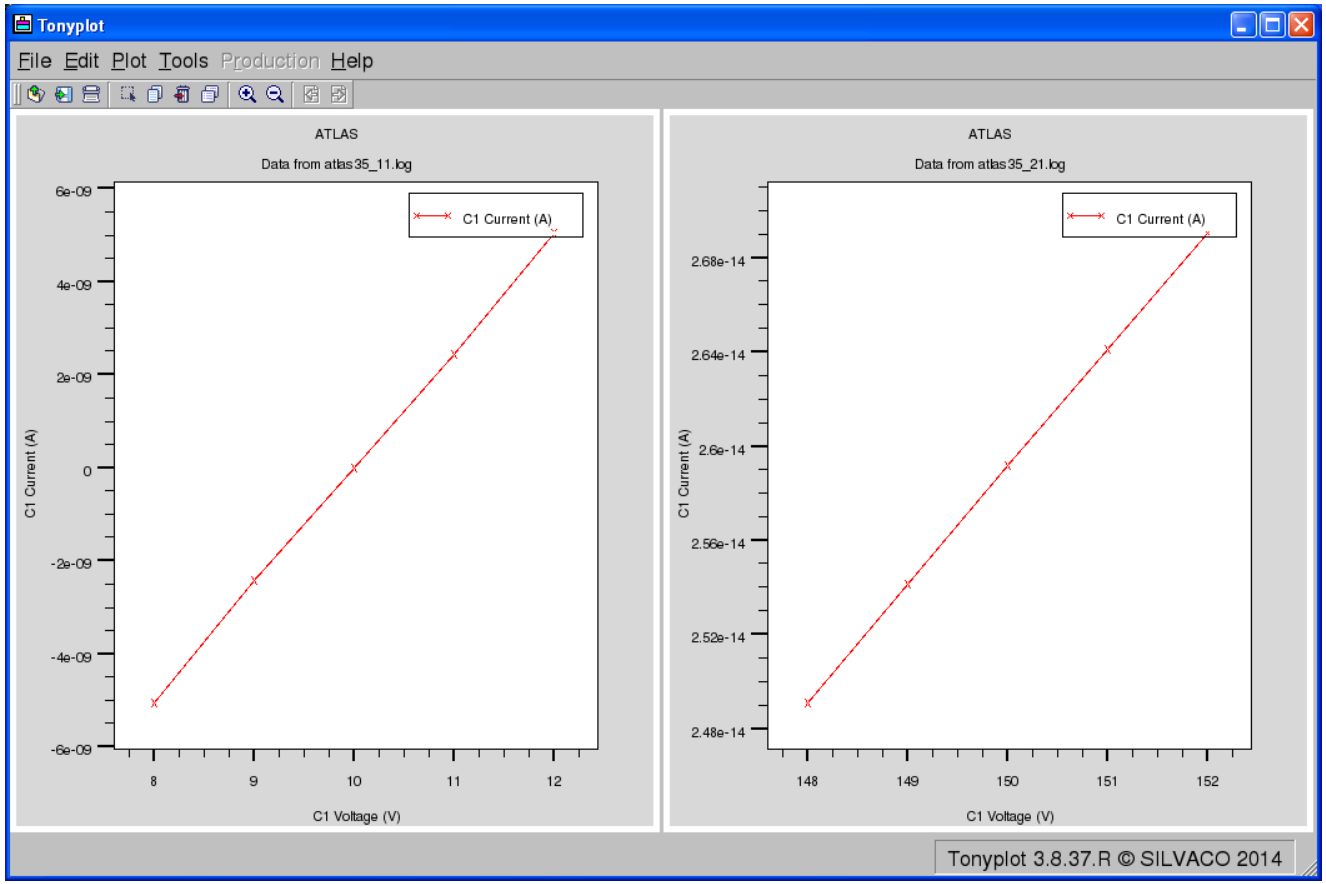




The net doping, electrons, holes und potential distribution at biasing 150V.

Inter strip isolation

The dc characteristic of the neighboring strips



V=10V V=150V

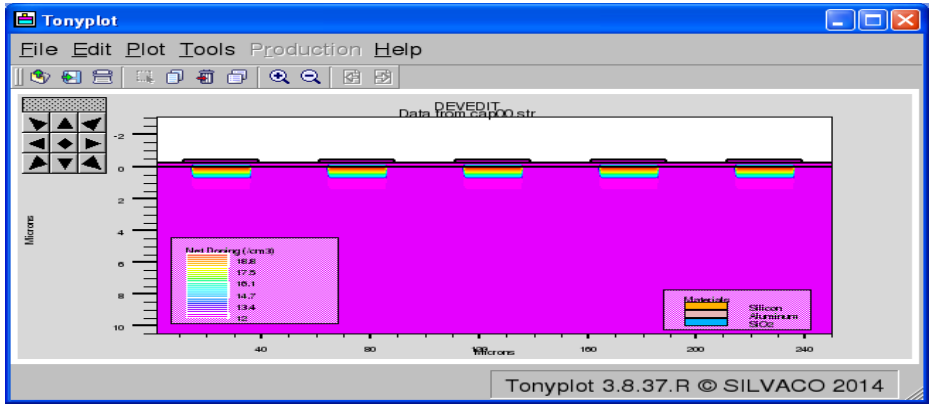
Pspray dose 3.5E12/cm2
From dc simulation with ΔV=1V
R=4.10E8Ωum V=10V
R=1.00E15Ωum V=150V

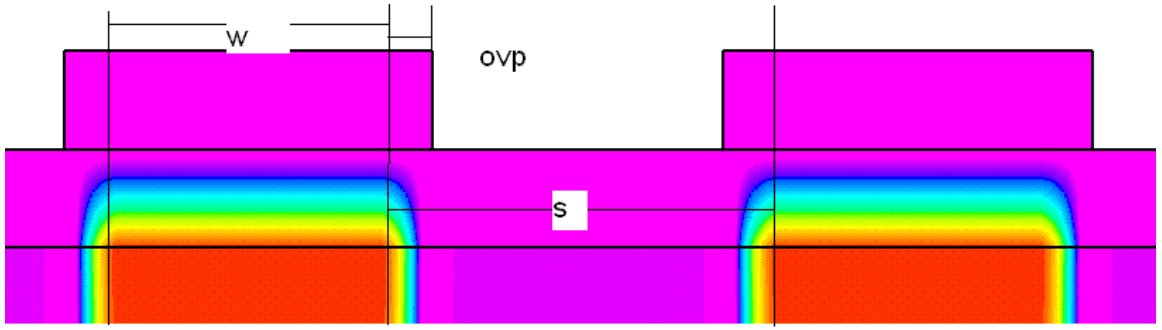
From ac simulation with f=1E5Hz
R=4.08E8Ωum V=10V
R=2.11E15Ωum V=150V

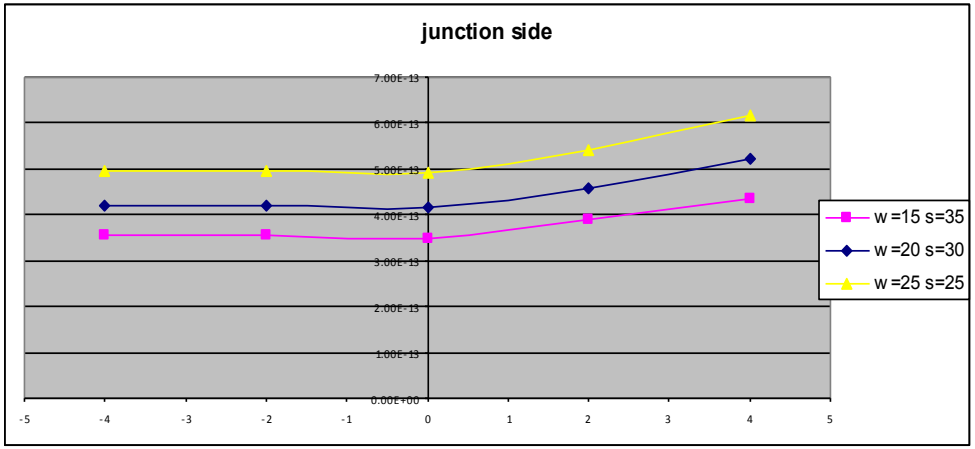
No pspray
From ac simulation with f=1E5Hz
R=1.25E6Ωum V=10V
R=1.69E6Ωum V=150V

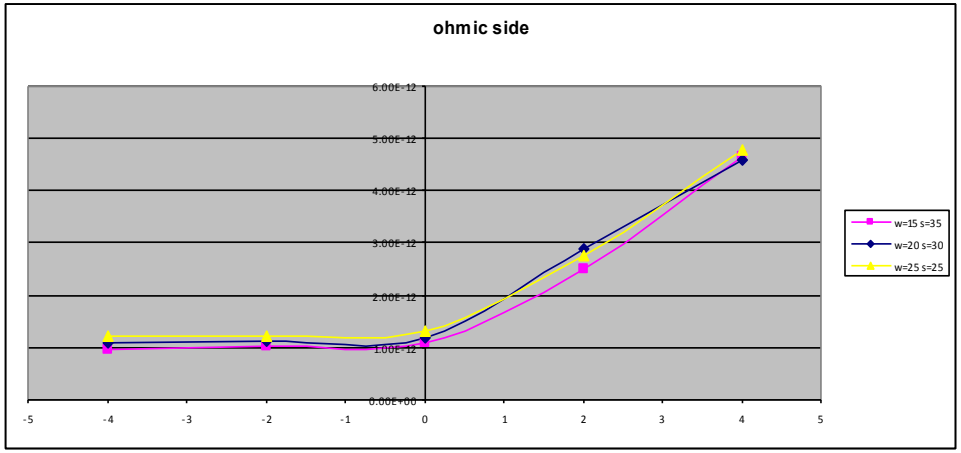
Inter strip capacitance

Above full depletion the inter strip capacitance is the main contributor to amplifier noise.
P-in-n micro strip silicon detector with ac coupling, back side with pspray.



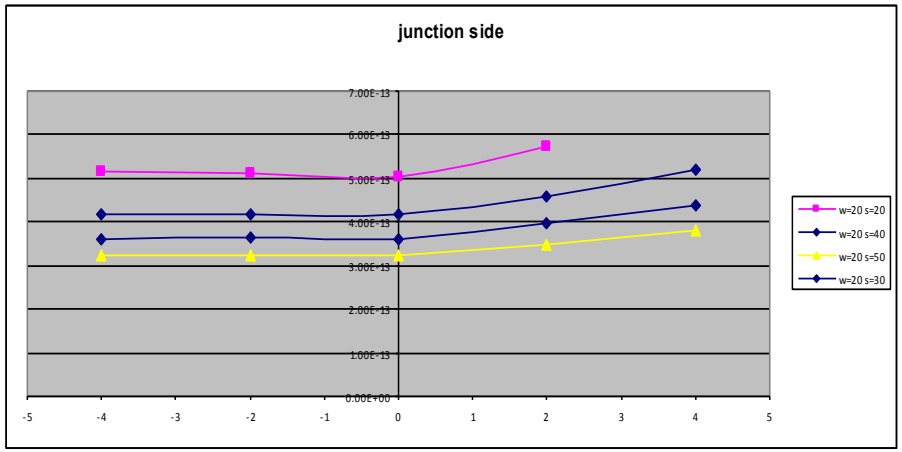


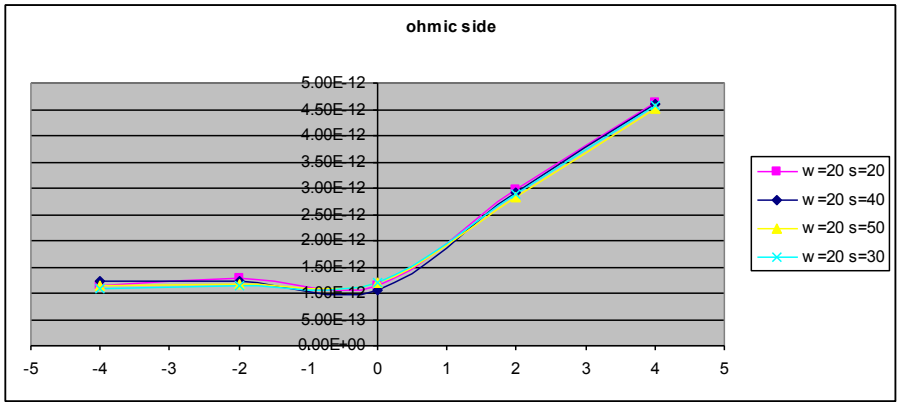


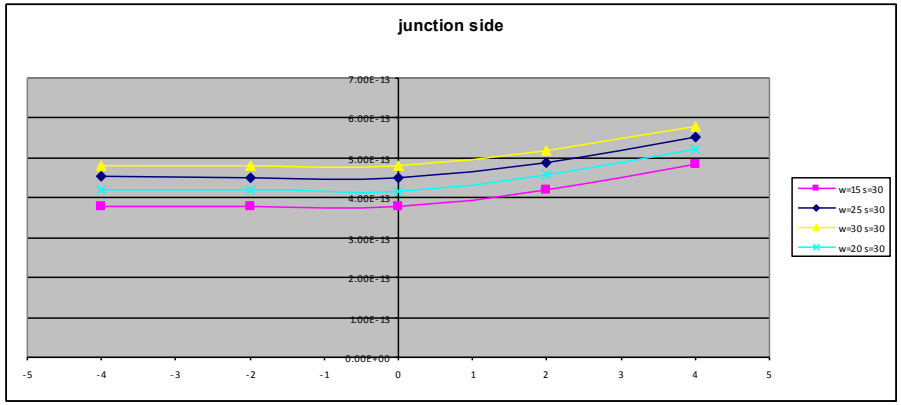


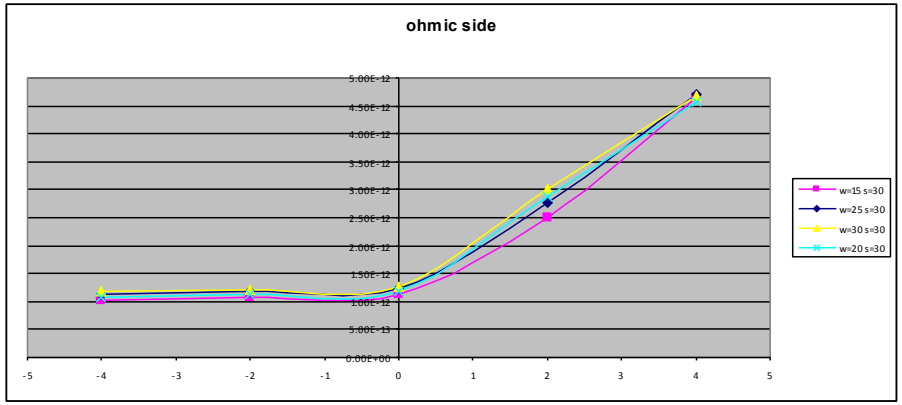
y axis the inter strip capacitance [F/cm], x axis the metal overlap in [microns].

Inter strip capacitance







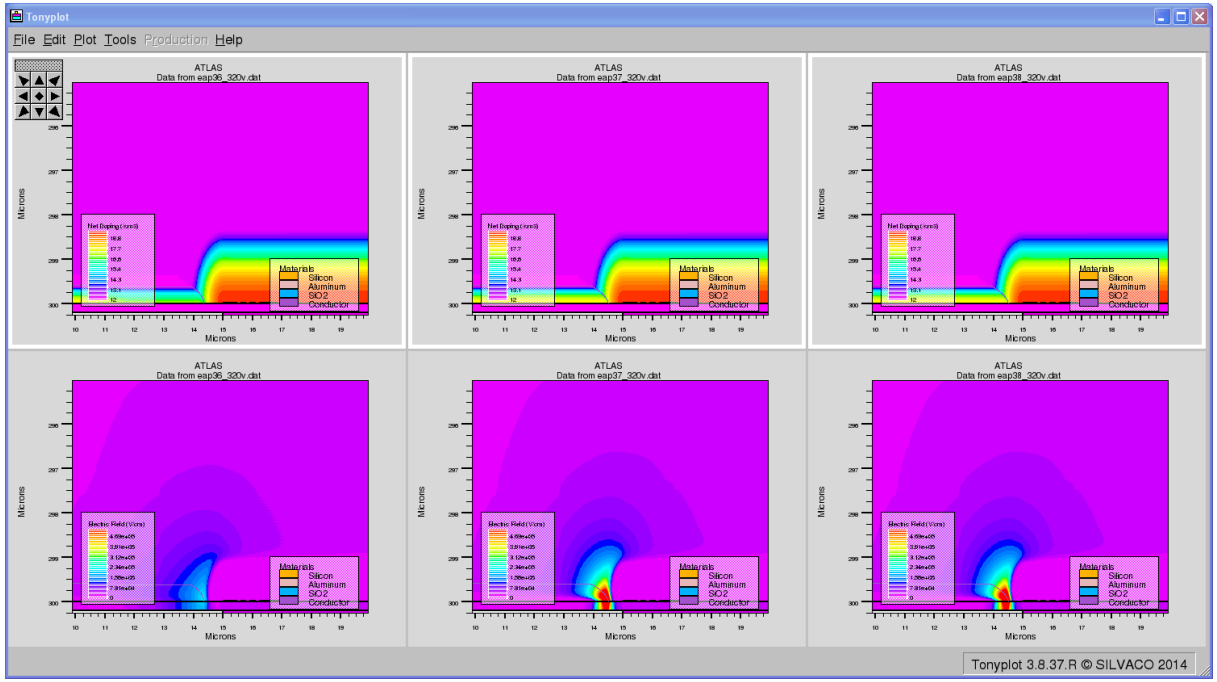


The interstrip capacitance is plotted as a function of different geometrical parameter to provide information for design.

The ohmic side interstrip capacitance is much larger than that of junction side.

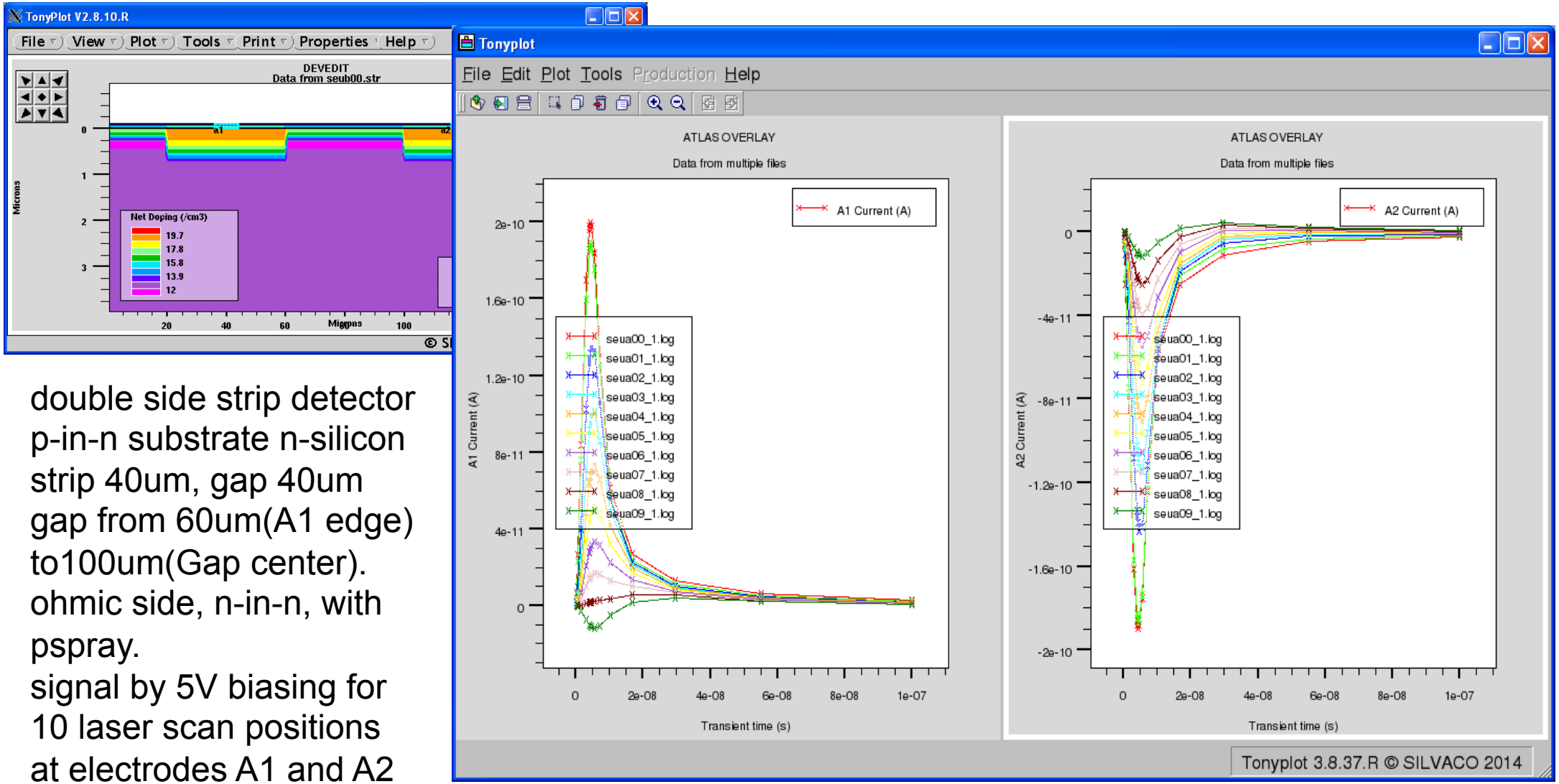
Pspray

Pspray is used as channel isolation for n-in-n structure.
The field strength depends on the structure.



ovb=4um bmax320=198062 V/cm
ovb=0 bmax320=709930 V/cm
ovb=-2um bmax320=709930 V/cm

Signal formation

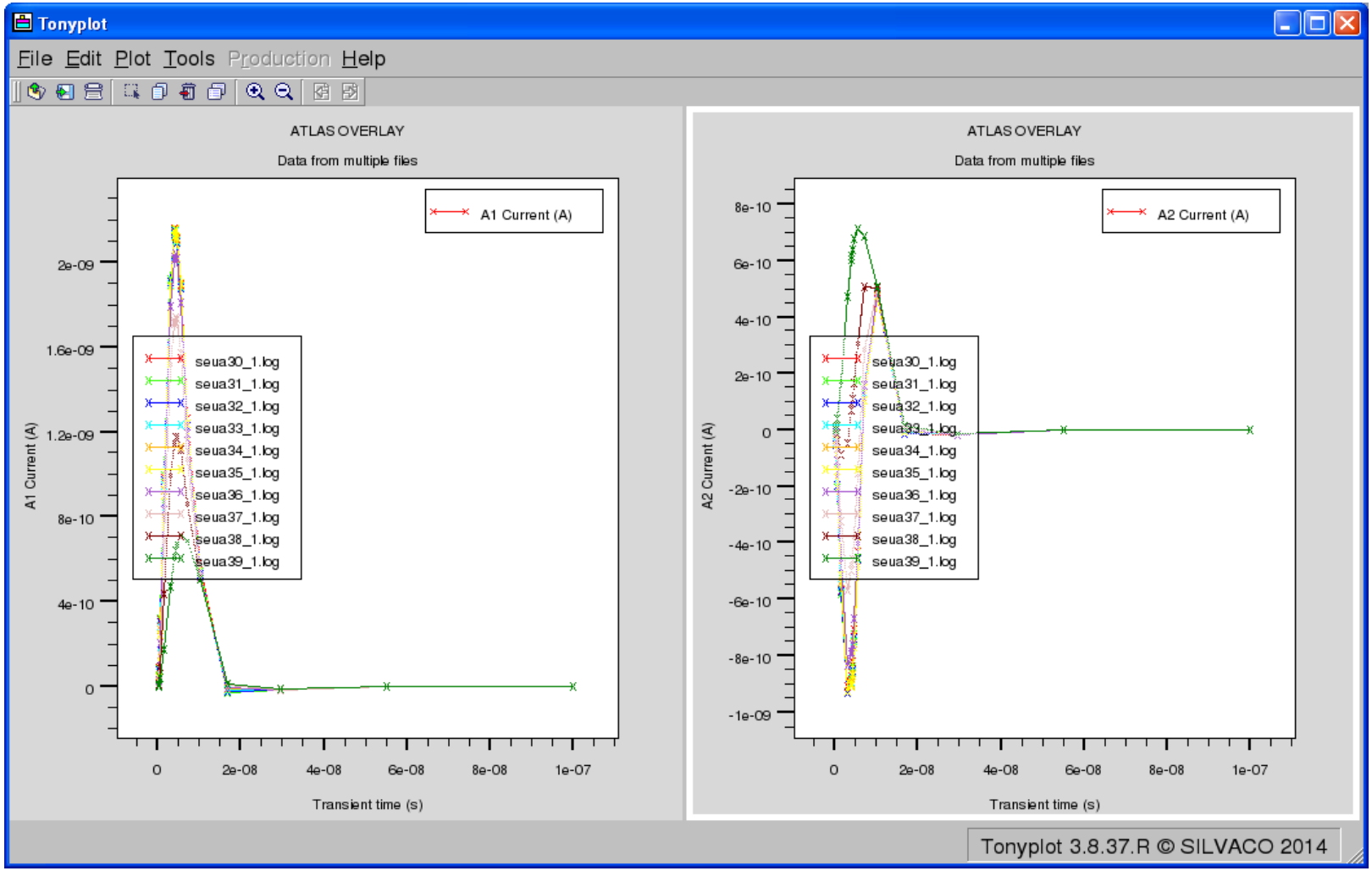


double side strip detector
p-in-n substrate n-silicon
strip 40um, gap 40um
gap from 60um(A1 edge) to100um(Gap center).
ohmic side, n-in-n, with pspray.
signal by 5V biasing for 10 laser scan positions at electrodes A1 and A2

curve	0	1	2	3	4	5	6	7	8	9
position	60	63	66	68	70	72	74	76	78	80

Charge sharing

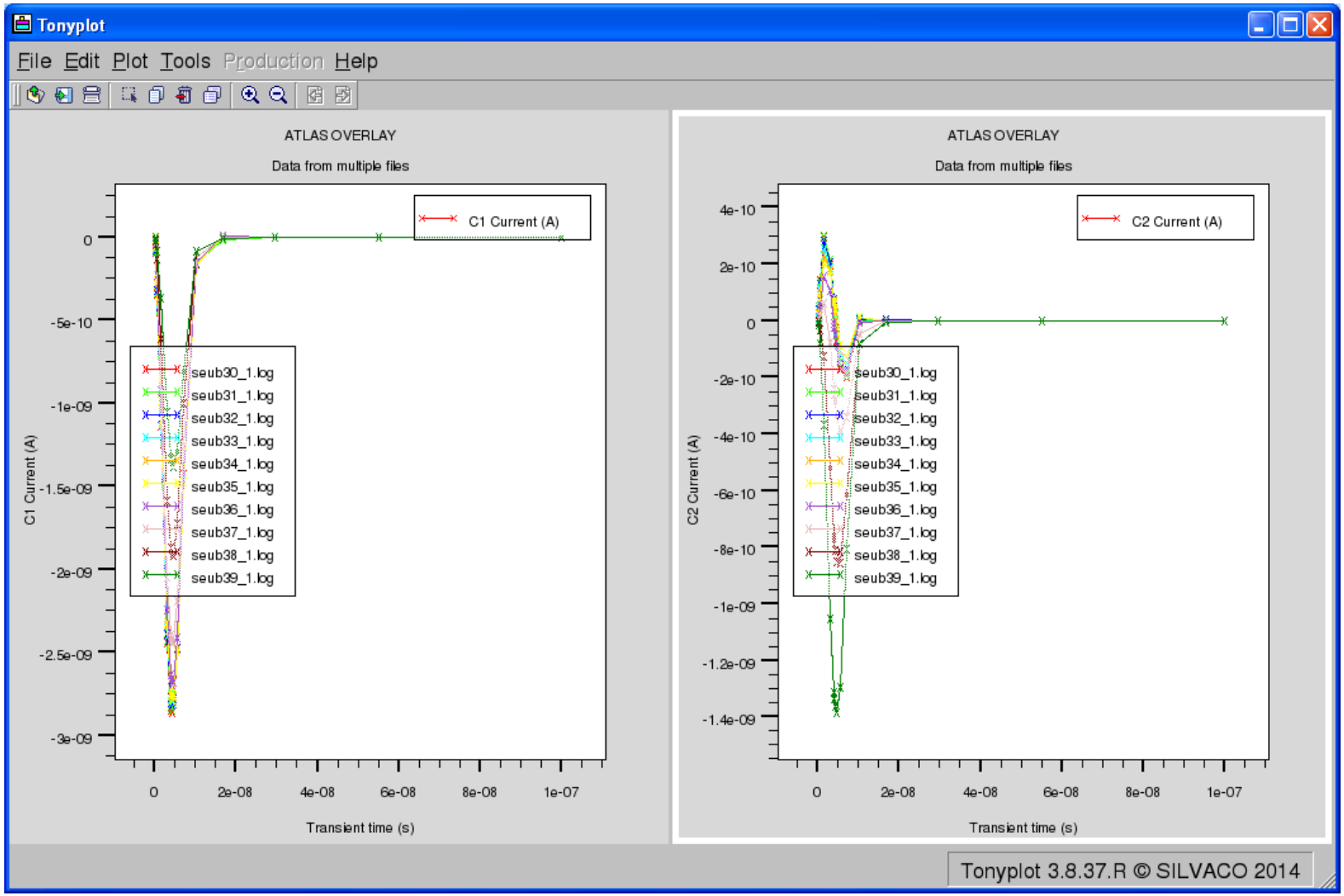
Signal 200V on ohmic side, with pspray



For bias 200V the signal is faster and the amplitude is bigger. The signal will be smaller if laser is moved away from the A1 strip, the signal of neighboring A2 strip is getting bigger.

Charge sharing

Signal 200V on junction side



The signal is faster and bigger than that of the ohmic side.

Conclusion

- The numerical simulation is helpful for the process and design and possible failure analysis
- Silvaco input deck script is for most case OK
- Electrical simulations agree well with tests if lifetime is scaled
- Process simulation and SIMS profile need fine tuning
- We have produced high quality micro pixel and strip sensor for ATLAS CMS CBM ...
- Poly resistor and punch through basing
- Single or double side
- Double metal possible
- Pspray and pstop isolation
- FZ-n or FZ-p silicon substrate
- Detector on thin membrane

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