R&D Activities at IN2P3 for a Vertex Detector suited to ILC

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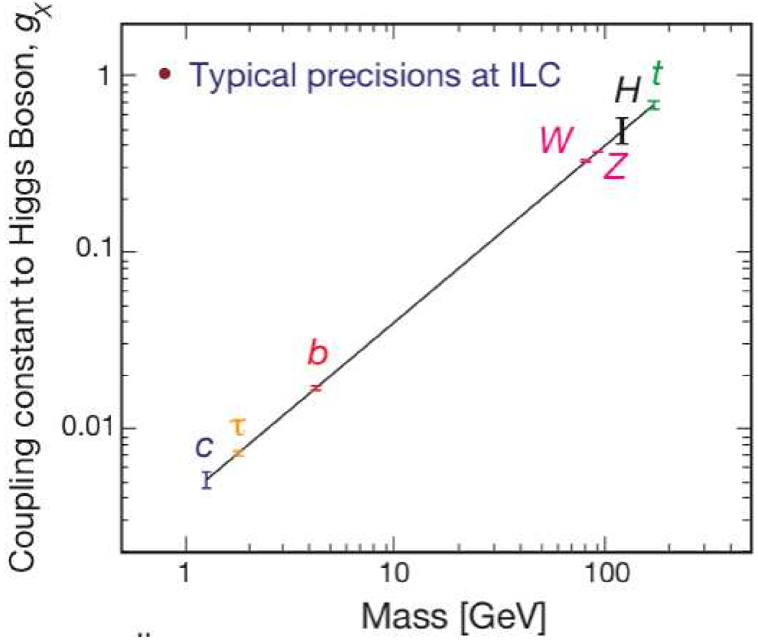
Outline

- *Requirements and topics addressed*
- *Status of CPS development for running at $\sqrt{s} \lesssim$ 500 GeV* (0.35 μm process)
- *Improvements coming from 0.18 μm CMOS process*
  - $\hookrightarrow$ *fast CMOS sensor (AROM) with μs level timestamping*
- *2-sided ladder developments*
- *Plans for the coming years*
- *Summary*

ILC Vertexing Performance Goals

- **Specific hierarchy of requirements for an ILC vertex detector :**
  - ⋇ unprecedented granularity & material budget (very low power)
  - ⋇ much less demanding running conditions than at LHC
    - $\Rrightarrow$ alleviated read-out speed & radiation tolerance requests
  - ⋇ ILC duty cycle $\sim$ 1/200
    - $\Rrightarrow$ power saving by power pulsing sub-systems

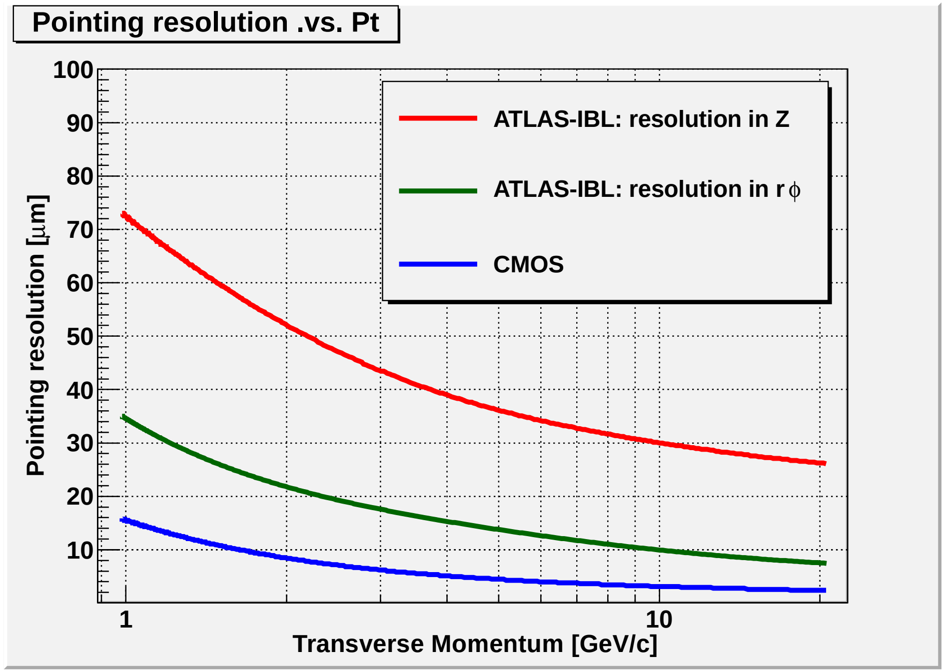


- **Vertexing goal :**
  - ⋇ achieve high efficiency & purity flavour tagging
    - $\rightarrowtail$ charm & tau, jet-flavour !!!

$\hookrightarrow$ $\sigma_{R\phi,Z} \leq 5 \oplus 10/p \cdot sin^{3/2}\theta \;\; \mu m$

- $\triangleright$ LHC: $\sigma_{R\phi} \simeq 12 \oplus 70/p \cdot sin^{3/2}\theta$

$\triangleright$ Comparison: $\sigma_{R\phi,Z}$(ILD) with VXD made of ATLAS-IBL or ILD-VXD pixels $\rightarrowtail$



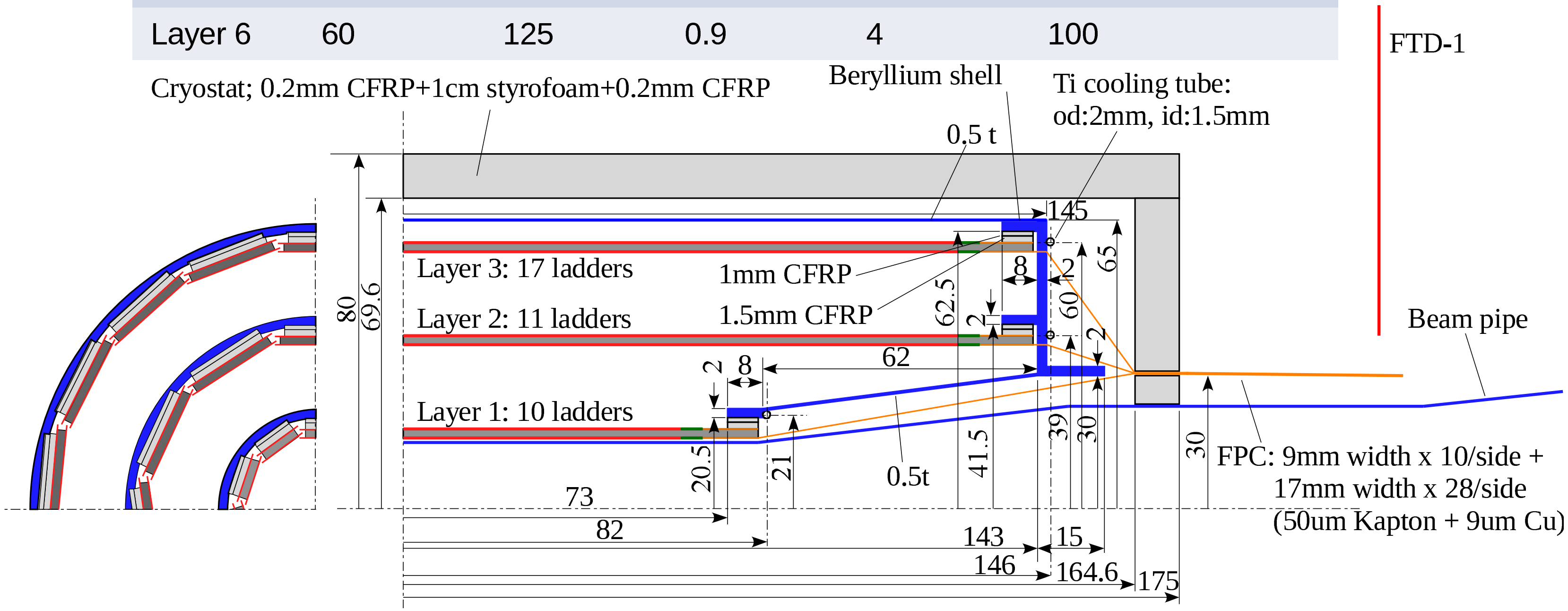
- ⋇ Concrete requirements :

$\sigma_{sp} < 3 \;\mu m$; $\quad < 0.15\%\ X_0$/layer

Vertex detector in DBD

- Baseline design

	R (mm)	|z| (mm)	|cosθ|	σ (μm)	Readout time (μs)
Layer 1	16	62.5	0.97	2.8	50
Layer 2	18	62.5	0.96	6	10
Layer 3	37	125	0.96	4	100
Layer 4	39	125	0.95	4	100
Layer 5	58	125	0.91	4	100
Layer 6	60	125	0.9	4	100



The Central Conflict of Vertexing

- A COMPLEX SET OF STRONGLY CORRELATED ISSUES :

  ⋇ **Charged particle sensor technology :**

  highly granular, thin, low power, swift pixel sensors

  ⋇ **Micro-electronics :**

  highly integrated, low power, SEE safe, r.o. μcircuits

  ⋇ **Electronics :**

  high data transfer bandwith (no trigger), some SEE tol.

  low mass power delivery, allowing for power cycling

  ⋇ **Mechanics :**

  rigid, ultra-light, heat but not electrical conductive,
  mechanical supports, possibly with $C_{\Delta t} \simeq C^{Si}_{\Delta t}$

  very low mass, preferably air, cooling system

  micron level alignment capability

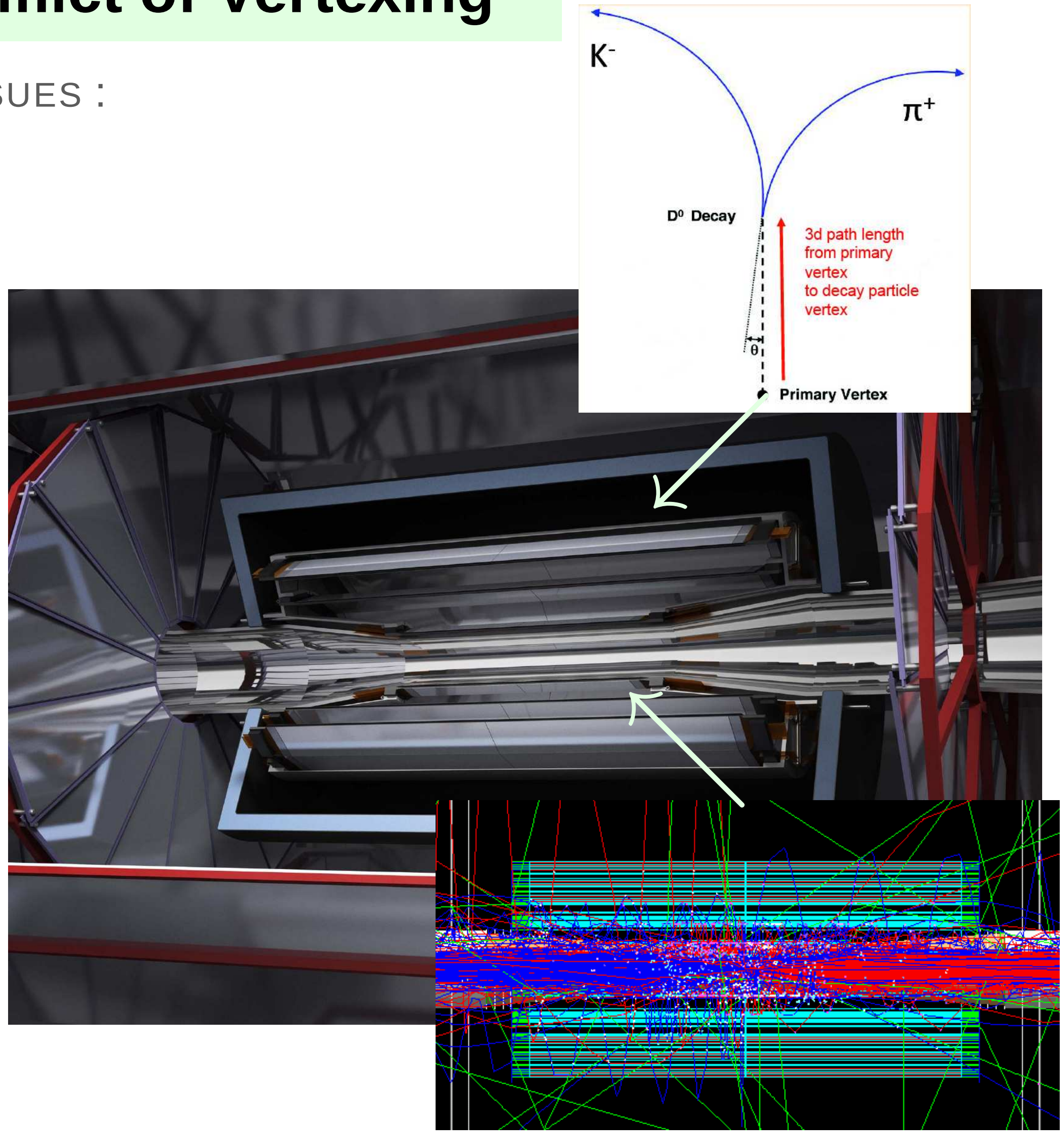
  ⋇ **EM compliance :**

  power cycling in high B field $\Rrightarrow$ F(Lorentz)

  higher mode beam wakefield disturbance $\Rrightarrow$ pick-up noise ?

  ⋇ **Radiation load and SEE compliance at T_{room}**

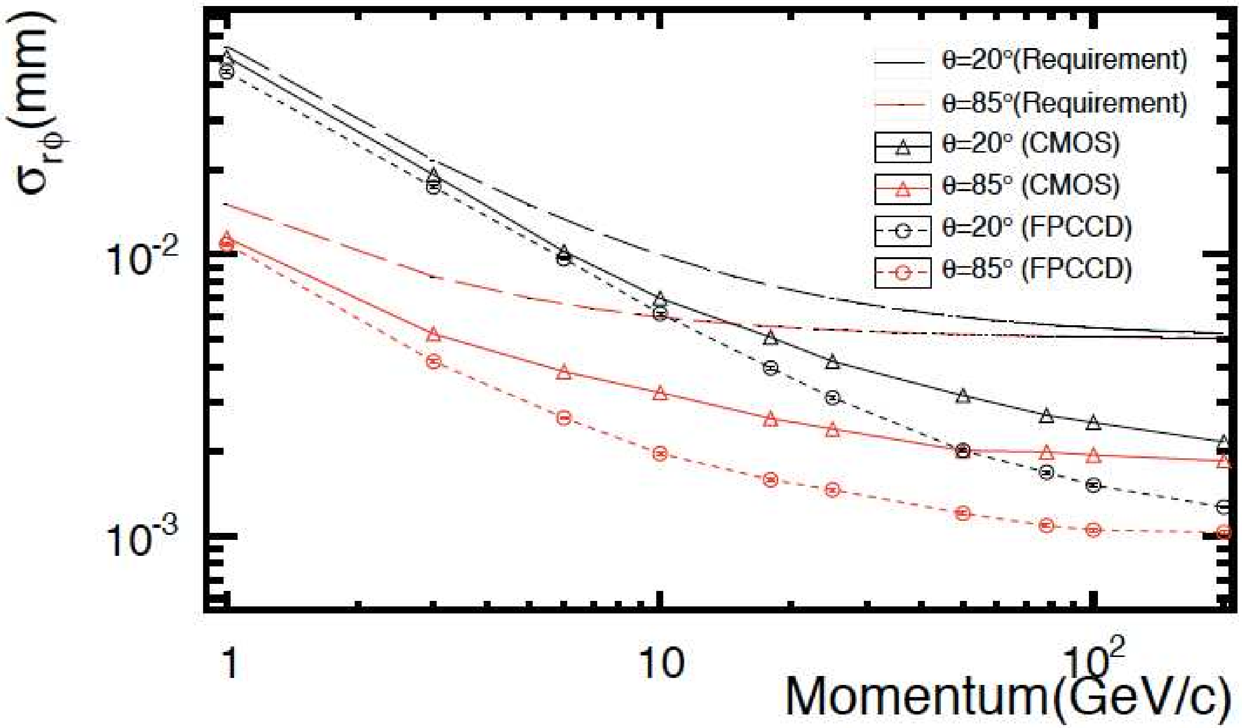
  $\Rrightarrow$ reduced material budget



Fine versus High Precision Pixels

- 5 μm VS 17 μm PITCH :

  $\equiv$ **delayed vs continuous read-out**



- FINE PIX. OFFRE SEVERAL ADVANTAGES:
  - improved impact parametre accuracy
  - no power pulsing required
  - less challenging read-out

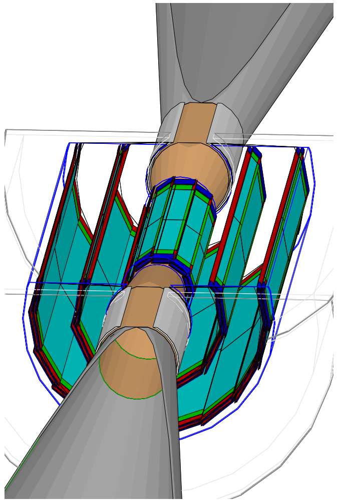
    than continuous option
  - mitigated risk of EMI
  - occupancy may be an issue

    $\hookrightarrow$ presumably not at 250 GeV (reduced beam BG)

    $\gtrsim$ 500 GeV: combine FP with fast, continous, read-out sensors on opposite face of ladder ?
  - may not be restricted to CCDs $\Rrightarrow$ radiation tolerance & cooling issues alleviated ?

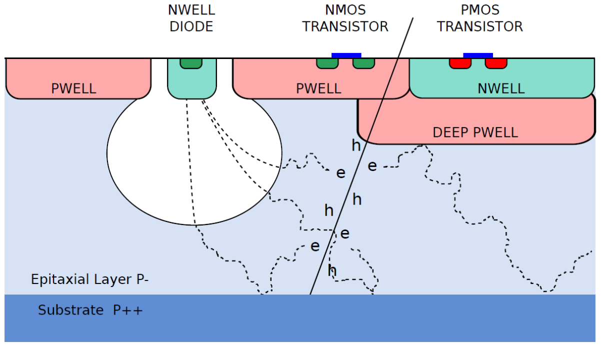
$\Rrightarrow$ CLARIFY THE PHYSICS CASE OF "FINE PIXELS"

Topics Addressed by the R&D

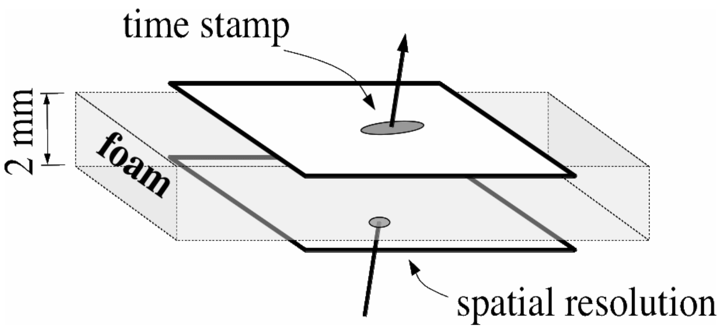


- VERTEX DETECTOR CONCEPT :
  - Cylindrical geometry based on 3 concentric 2-sided layers
  - Layers equipped with 3 different CMOS Pixel Sensors (CPS)

- PIXEL SENSOR DEVELOPMENT:
  - Exploit CPS potential & IPHC expertise
  - R&D performed in synergy with other applications
    $\hookrightarrow$ EUDET-BT, STAR, ALICE, CBM, ...
  - CPS $\equiv$ unique technology being simultaneously
    granular, thin, integrating full FEE, industrial & cheap
  - Address trade-off btw spatial resolution & read-out speed



- DOUBLE-SIDED LADDER DEVELOPMENT:
  - Develop concept of 2-sided ladder using 50 μm thin CPS
  - Develop concept of mini-vectors providing
    high spatial resolution & time stamping
  - Address the issue of high precision alignment
    & power cycling in high magnetic field

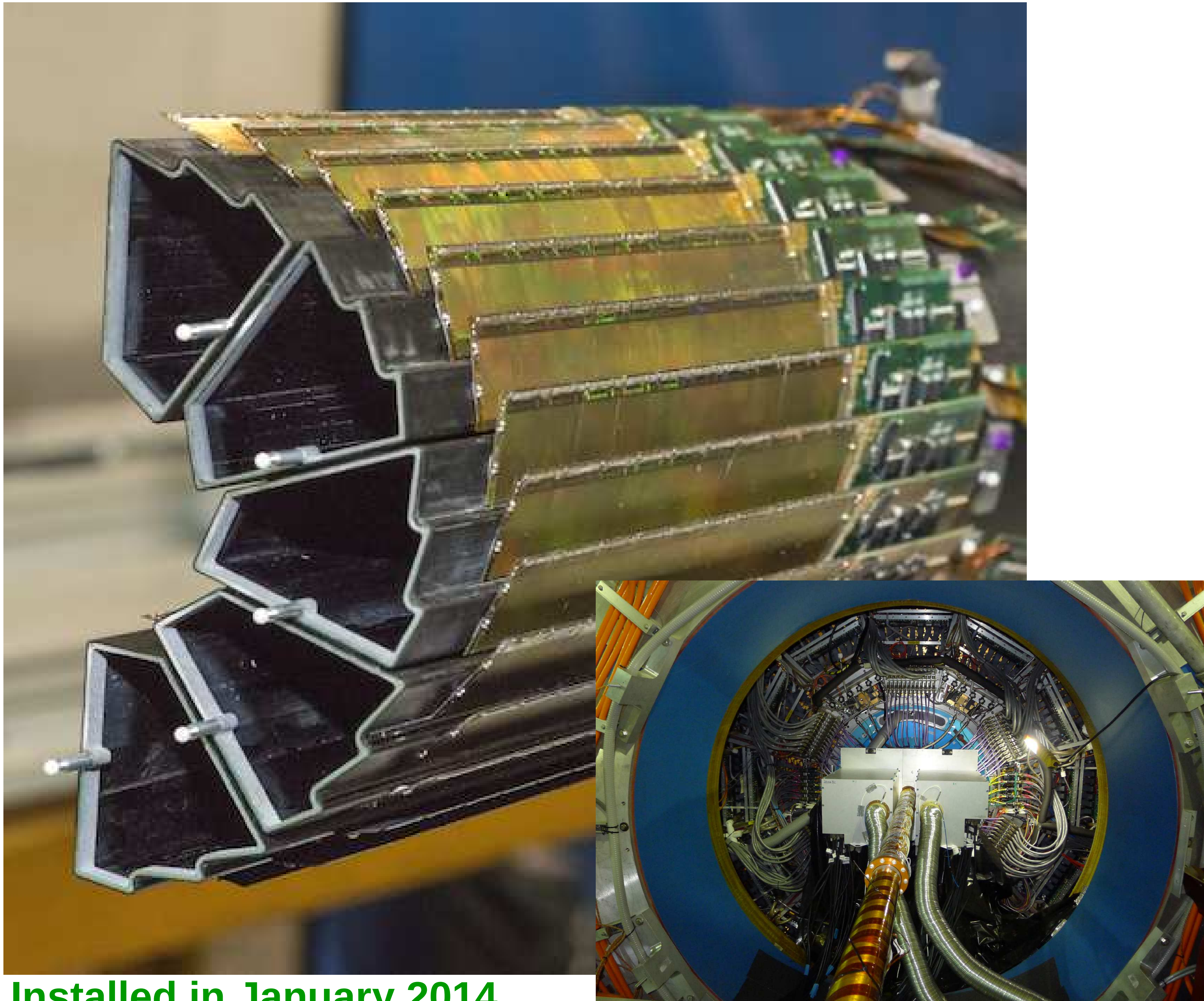


DEVELOPMENT OF CMOS SENSORS

STAR-PXL

HALF-BARREL :

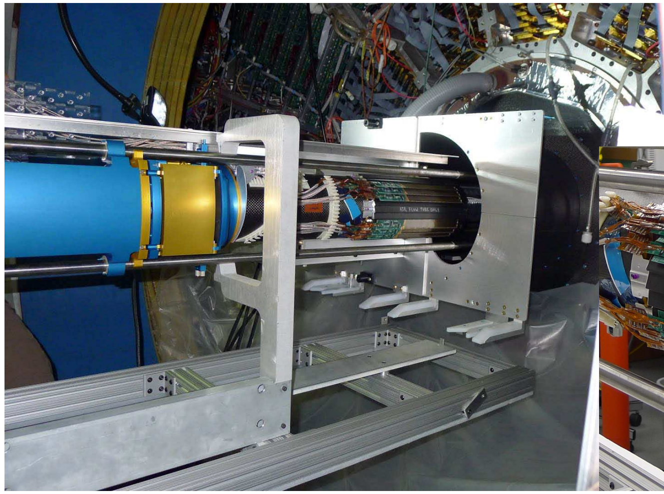
- **20 ladders (0.37% X_0)**
- **200 sensors**
- **$180 \cdot 10^6$ pixels**
- **air flow cooling :**
  $T \lesssim 35^\circ C$
- $\sigma_{sp} < 4\ \mu m$
- **rad. load $\gg$ ILC values**
- **$t_{r.o.} \simeq 190\ \mu s$**
  $\hookrightarrow$ **ILC : O(10) μs !**



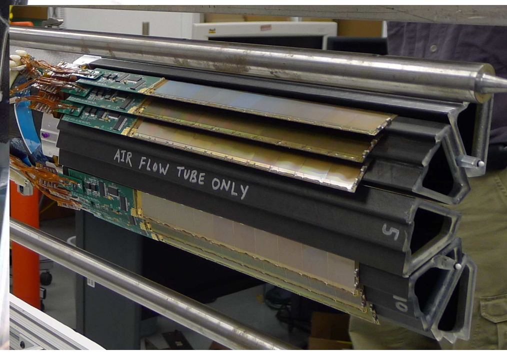
Installed in January 2014

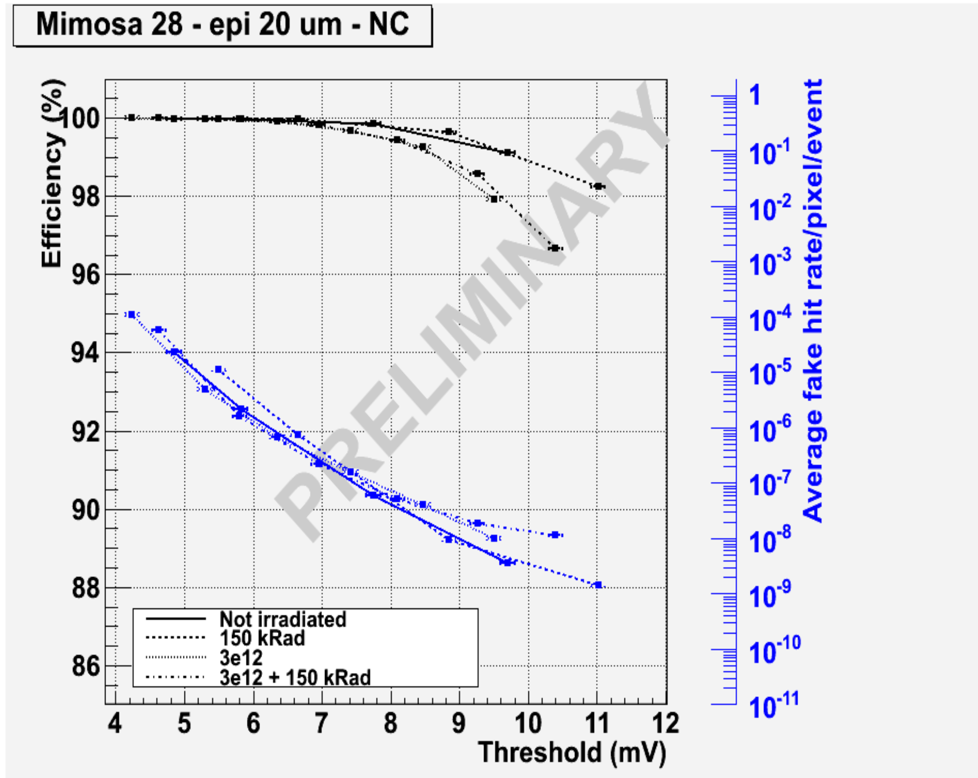
State-of-the-Art: MIMOSA-28 for the STAR-PXL

- Main characteristics of ULTIMATE ($\equiv$ MIMOSA-28):
  - rolling shutter read-out derived from EUDET BT chip: MIMOSA-26
  - 0.35 μm process with high-resistivity epitaxial layer
  - column // architecture with in-pixel cDS & amplification
  - end-of-column discrimination & binary charge encoding
  - on-chip zero-suppression
  - active area: 960 colums of 928 pixels (19.9$\times$19.2 mm^2)
  - pitch: 20.7 μm $\rightarrowtail$ $\sim$ 0.9 million pixels
    $\hookrightarrow$ charge sharing $\Rrightarrow$ $\sigma_{sp} \gtrsim$ 3.5 μm
  - JTAG programmable
  - t$_{r.o.} \lesssim$ 200 μs ($\sim$ 5$\times$10^3 frames/s) $\Rrightarrow$ suited to $>$10^6 part./cm^2/s
  - 2 outputs at 160 MHz
  - $\sim$ 150 mW/cm^2 power consumption
  - N $\lesssim$ 15 e$^-$ ENC at 30-35°C
  - ϵ_{det} versus fake hit rate $\rightarrowtail$ $\rightarrowtail$ $\rightarrowtail$ $\rightarrowtail$
  - Radiation tolerance : 3$\cdot$10^{12}n$_{eq}$/cm^2 & 150 kRad at 30-35°C
  - Detector construction under way (40 ladders made of 10 sensors)



8 May 2013





$\triangleright\triangleright\triangleright$ 1st step: Commissioning of 3/10 of detector completed at RHIC with pp collisions in May-June 2013

$\triangleright\triangleright\triangleright$ **next step: Start of physics with full detector in February 2014**

CMOS Pixel Sensors for the ILD-VXD (1/3)

- **Two types of CMOS Pixel Sensors :**

※ **Inner layers** ($\lesssim$ 300 cm^2) :

Priority to read-out speed & spatial resolution

↪ small pixels (16×16 / 80 μm^2)

with binary charge encoding

↪ $t_{r.o.} \sim$ 50 / 10 μs; $\sigma_{sp} \lesssim$ 3 / 6 μm

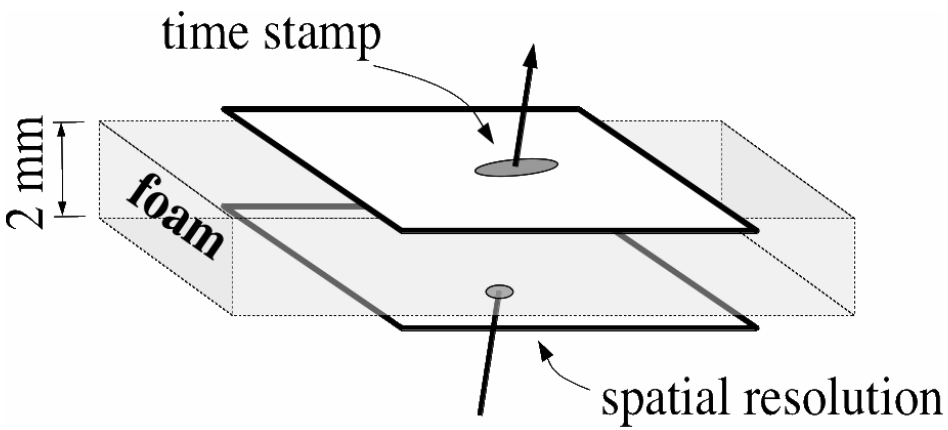
※ **Outer layers** ($\sim$ 3000 cm^2) :

Priority to power consumption and good resolution

↪ large pixels (35×35 μm^2)

with 3-4 bits charge encoding

↪ $t_{r.o.} \sim$ 100 μs; $\sigma_{sp} \lesssim$ 4 μm



※ Total VXD instantaneous/average power $<$ 600/12 W (0.18 μm process)

- **2-sided ladder concept for inner layer :**

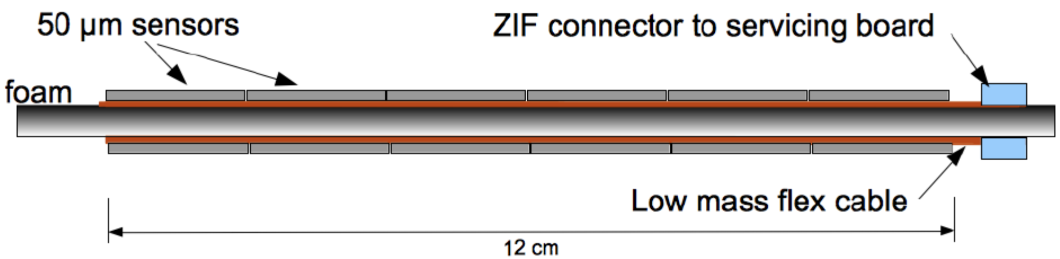
↪ PLUME collaboration

※ **Square pixels** (16×16 μm^2)

on internal ladder face ($\sigma_{sp} < 3\ \mu m$)

※ **Elongated pixels** (16×64/80 μm^2)

on external ladder face ($t_{r.o.} \sim$ 10 μs)



CMOS Pixel Sensors for the ILD-VXD (2/3)

- **From the STAR-PXL to the ILC-VXD :**

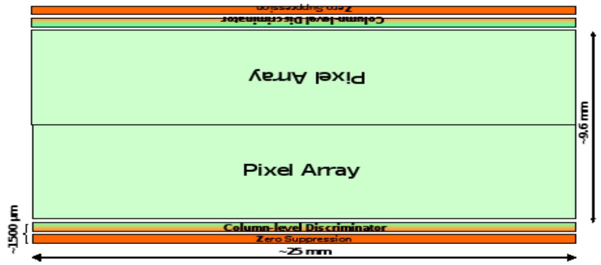
Detector	σ_{sp}	t_{int}	**Dose** (30°C)	**Fluence** (30°C)
STAR-PXL	$\gtrsim$ 3.5 μm	190 μs	150 kRad	$3\cdot10^{12} n_{eq}/cm^2$
ILD-VXD/In	$<$ 3 μm	50/10 μs	$<$ 100 kRad	$\lesssim 10^{11} n_{eq}/cm^2$
ILD-VXD/Out	$\lesssim$ 4 μm	100 μs	$<$ 10 kRad	$\lesssim 10^{10} n_{eq}/cm^2$

- **Final "500 GeV" CPS prototypes :** fab. in Winter 2011/12 **(0.35 μm process for economic reasons)**

  ⋇ **MIMOSA-30:** inner layer prototype with 2-sided read-out ▹ ▷ ▷

  ↪ one side : 256 pixels (16×16 μm^2)

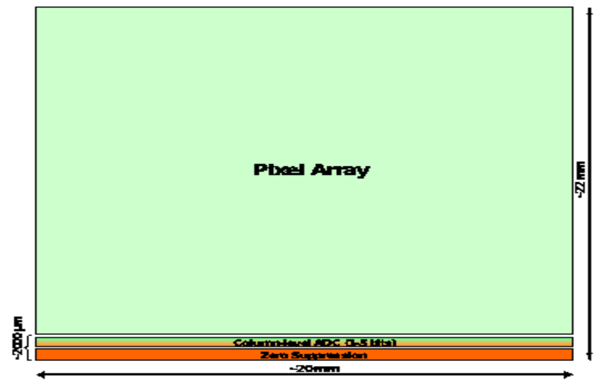
  other side : 64 pixels (16×64 μm^2)



  ⋇ **MIMOSA-31:** outer layer prototype ▹ ▷ ▷

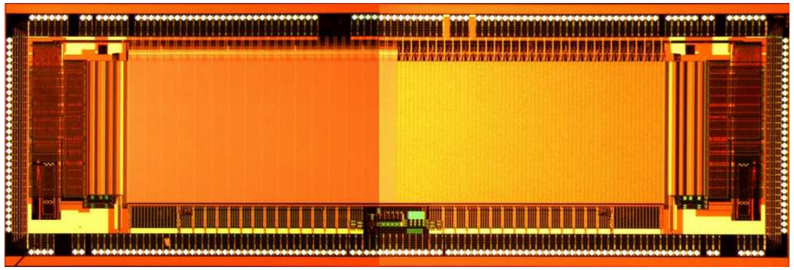
  ↪ 48 col. of 64 pixels (35×35 μm^2)

  ended with 4-bit ADC

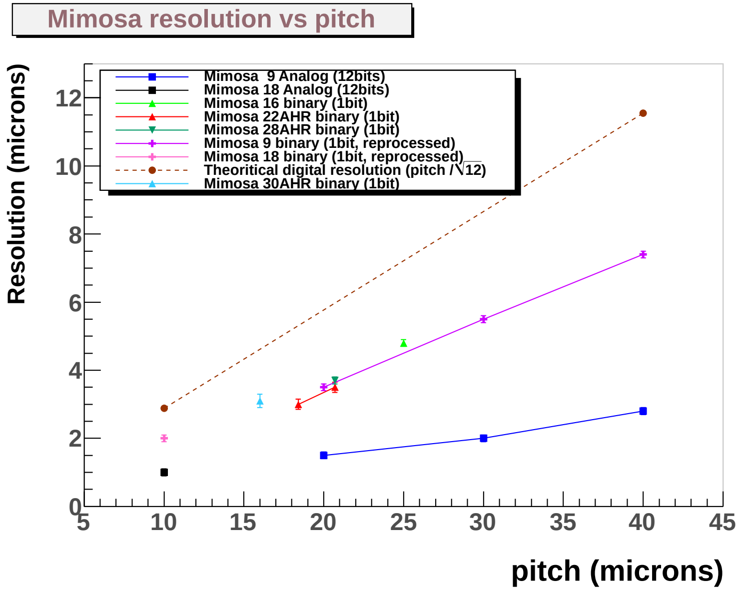


CMOS Pixel Sensors for the ILD-VXD (3/3)

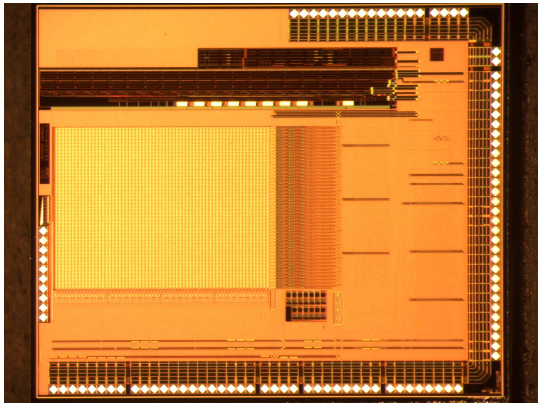
- **MIMOSA-30: prototype for ILD-VXD innermost layer** ▷ ▷ ▷



  - ⋇ 0.35 CMOS μm process with high-resistivity epitaxy
  - ⋇ in-pixel CDS, rolling shutter read-out, binary sparsified output
  - ⋇ columns length $\simeq$ final sensor (4-5 mm long)
  - ⋇ **high resolution side : pixels of 16×16** μm^2 $\Rrightarrow$ **expect** $\sigma_{sp} <$ **3** μm
    - 128 columns (discri) & 8 col. (analog) of 256 rows
    - read-out time $\lesssim$ 50 μs
  - ⋇ **time stamping side : pixels of 16×64** μm^2 $\Rrightarrow$ $t_{r.o.} \sim$ **10** μs
    - (expect $\sigma_{sp} \sim$ 6 μm)
    - 128 columns (discri) and 8 col. (analog) of 64 rows
    - lab tests positive : N $\sim$ 15 e$^-$ ENC & discri. all OK for $t_{r.o.} = 10\ \mu s$
  - ⋇ beam tests (CERN-SPS) in July '12 $\Rrightarrow$ σ_{sp} ▷ ▷ ▷



- **MIMOSA-31: prototype for ILD-VXD outer layers**
  - ⋇ pixels of 35×35 μm^2 (power saving) ▷ ▷ ▷
  - ⋇ 48 columns of 64 pixels ended with 4-bit ADC (1/10 of full scale chip)
    - $\hookrightarrow$ expect $\sigma_{sp} \lesssim$ 3.5 μm
  - ⋇ $t_{r.o.} \sim$ 10 μs (1/10 of full scale chip $\rightarrowtail$ $\sim$ 100 μs)



Acceleration of Frame Read-Out

- **Motivations for faster read-out:**
  - ⋇ robustness w.r.t. predicted 500 GeV BG rate (keep inner radius small, ...)
  - ⋇ standalone inner tracking capability (e.g. soft tracks)
  - ⋇ compatibility with high-energy running: expected beam BG at $\sqrt{s} \gtrsim$ 1 TeV $\simeq$ 3–5 $\times$ BG (500 GeV)

- **How to accelerate the elongated pixel read-out**
  - ⋇ elongated pixel dimensions allow for in-pixel discri. $\Rrightarrow$ $\geq$ 2 faster r.o.
  - ⋇ read out simultaneously 2 or 4 rows $\Rrightarrow$ 2-4 faster r.o./side
  - ⋇ subdivide pixel area in 4-8 sub-arrays read out in // $\Rrightarrow$ 2-4 faster r.o./side
  - ▷ 0.18 μm process needed: 6-7 ML, design compactness, in-pixel CMOS T, ...
  - ⋇ conservative step: 2 discri./col. **end** (22 μm wide) $\Rrightarrow$ simult. 2 row r.o.

- **Expected VXD performances at 1 TeV (and 0.5 TeV)**

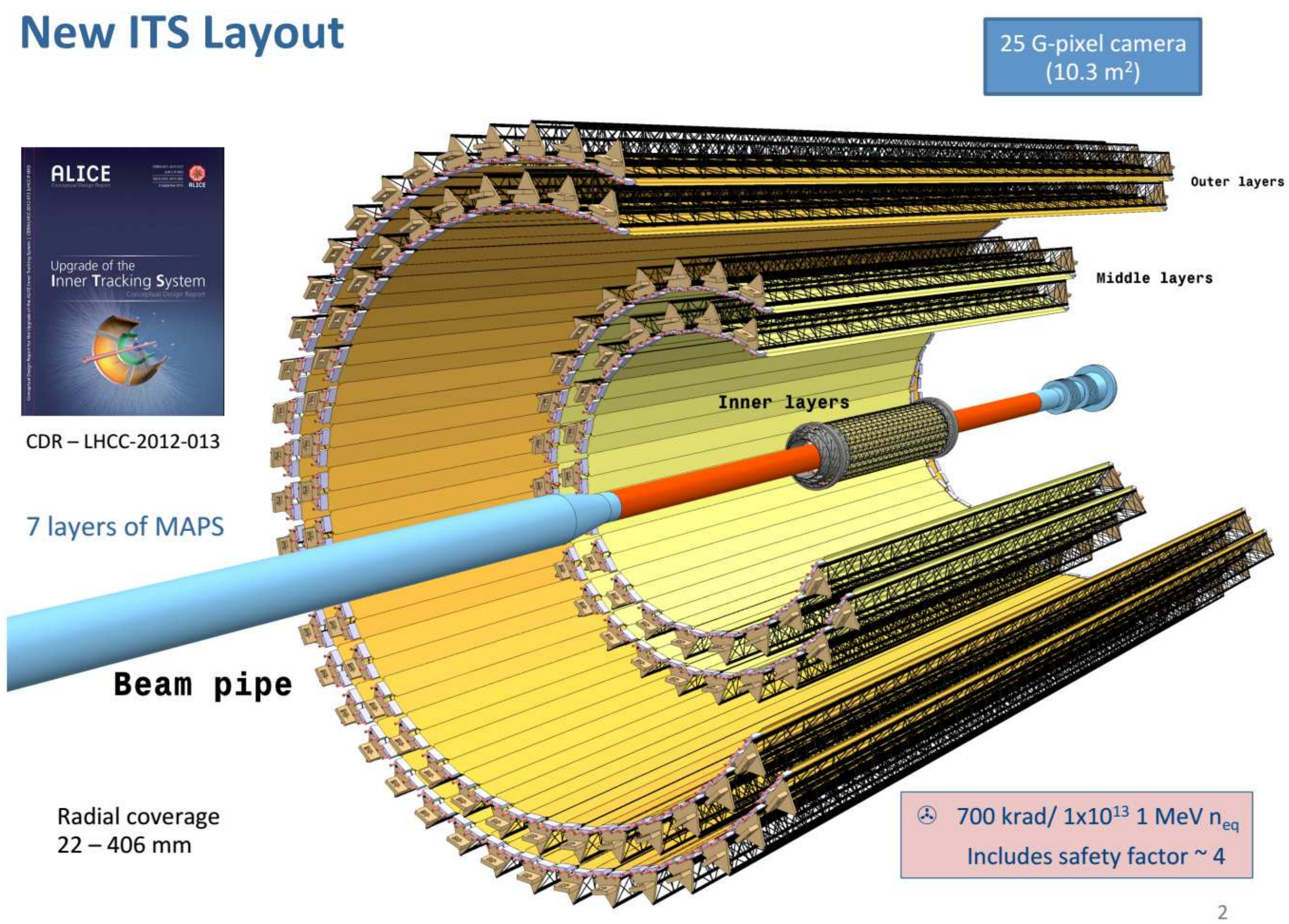
Layer	σ_{sp} MIMOSA/AROM	t_{int} MIMOSA/AROM	Occupancy [%] 1 TeV (0.5 TeV)	Power inst./average
VXD-1	3 / 5-6 μm	50 / 2 μs (10 μs)	4.5(0.9) / 0.5(0.1)	250/5 W
VXD-2	4 / 10 μm	100 / 7 μs (100 μs)	1.5(0.3) / 0.2(0.04)	120/2.4 W
VXD-3	4 / 10 μm	100 / 7 μs (100 μs)	0.3(0.06) / 0.05(0.01)	200/4 W

ALICE-ITS Upgrade

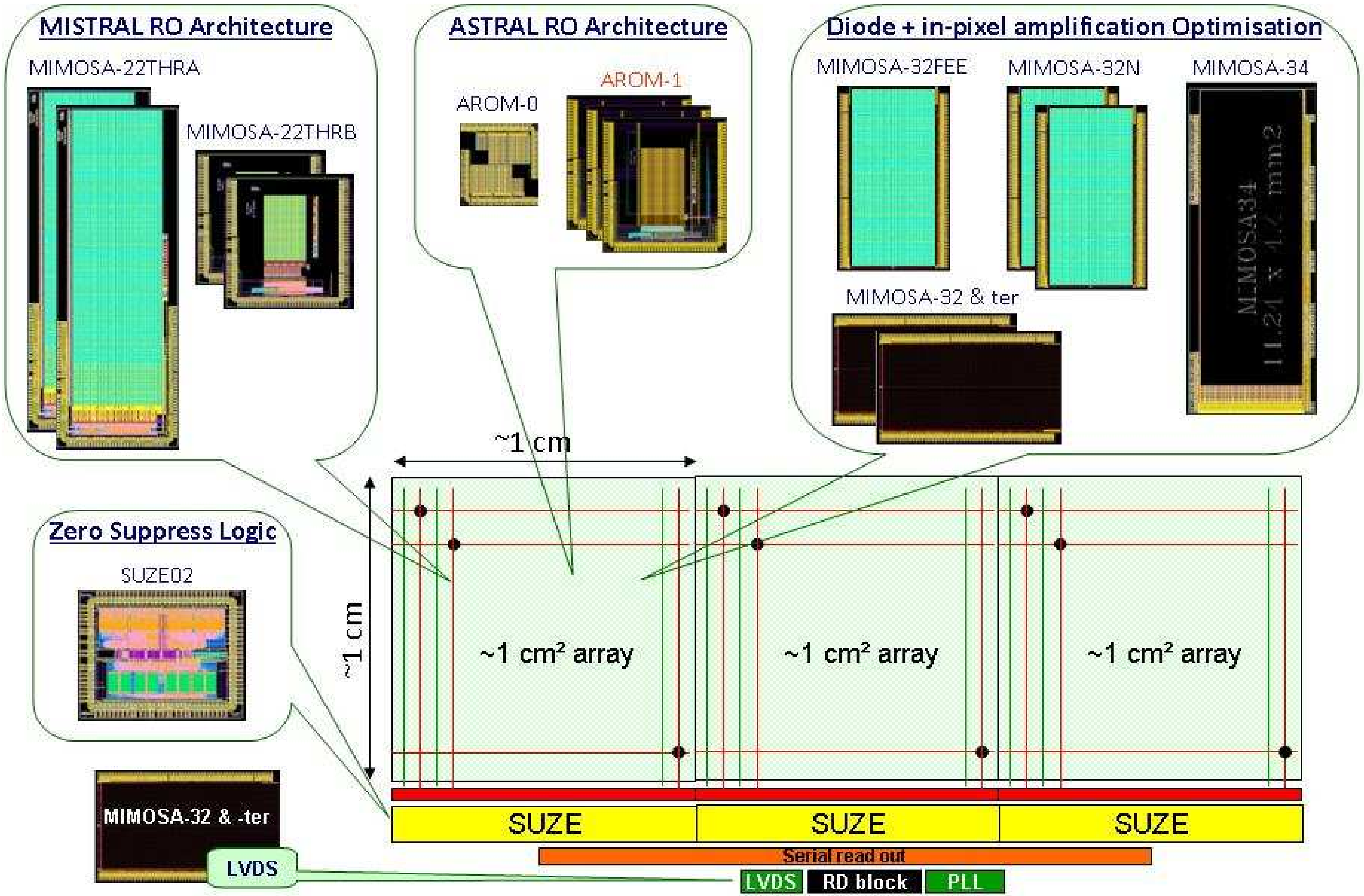
- 2 alternative sensors developped :
  - Baseline : **ASTRAL** (in-pixel discri.)
    $\hookrightarrow$ $\gtrsim$ 15 μs, 85 mW/cm^2
  - Back-up : **MISTRAL** (end-of-col. discri.)
    $\hookrightarrow$ $\gtrsim$ 30 μs, $<$ 200 mW/cm^2

- All main components validated in 2013 :
  - sensing node properties
  - in-pixel ampli+CDS
  - in-pixel discriminators
  - rolling-shutter with end-of-col. discri.
  - simultaneous 2-row read-out
  - sparse data scan
  - programmable chip steering (JTAG)

    $\hookrightarrow$ **outcome integrated in ITS-TDR**



CPS fabricated in 2012/13 in 0.18 μm Process

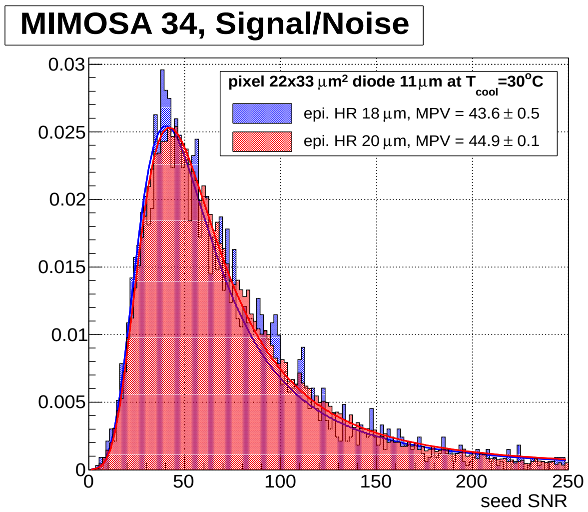


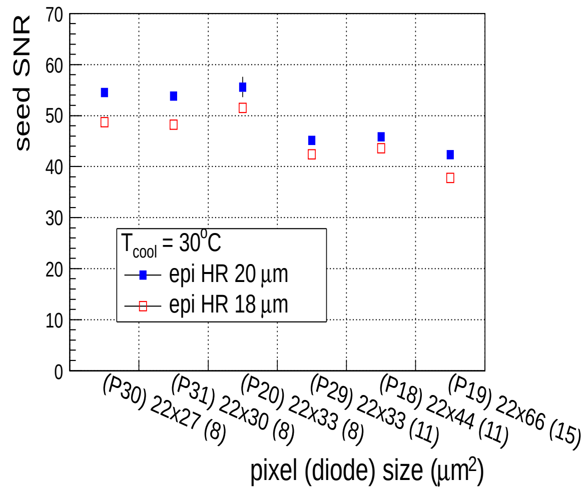
Pixel Optimisation : Epitaxial Layer and Sensing Node

- Pixel charge coll. perfo. for **HR-18** & **VHR-20** (no in-pixel CDS) :
  - ⋇ SNR distributions ⟼ MPV & low values tail
  - ⋇ $22 \times 33\ \mu m^2$ (2T) pixels at 30°C

⇛ **Results :**

- ◇ only ∼ 0.1 % of cluster seeds exhibit SNR $\lesssim$ 7–8
- ◇ SNR(VHR-20) ∼ 5-10% higher than SNR(HR-18)

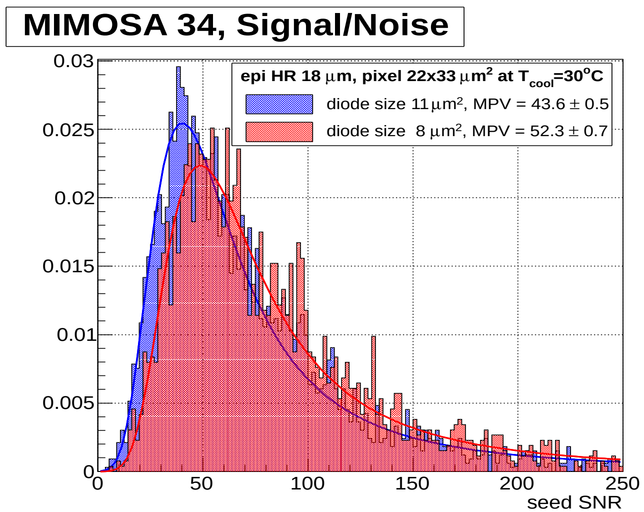


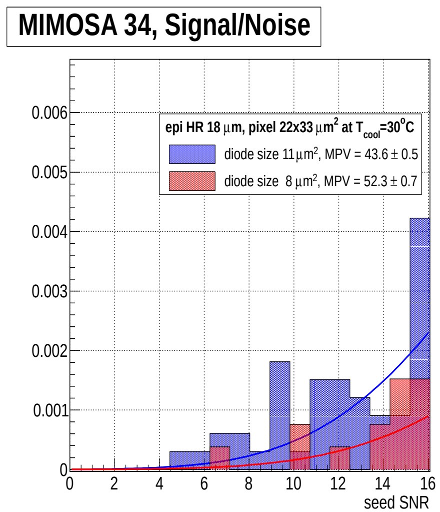


- Pixel charge coll. perfo. for 2 diff. sensing nodes:
  - ⋇ $10.9\ \mu m^2$ large sensing diode
  - ⋇ $8\ \mu m^2$ cross-section sensing diode underneath $10.9\ \mu m^2$ large footprint

⇛ **Results :**

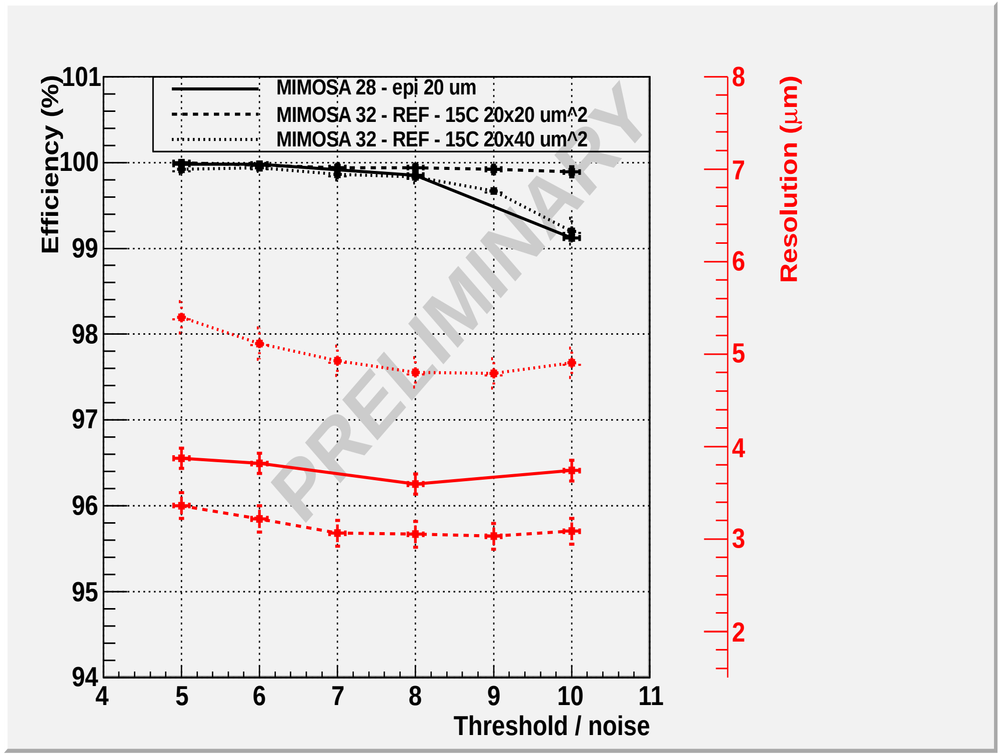
- ◇ $8\ \mu m^2$ diode features nearly 20% higher SNR(MPV) & much less pixels at small SNR (e.g. SNR <10)
  - ⟶ $Q_{clus} \simeq$ 1350/1500 e^- for 8/10.9 μm^2
- ⇛ marginal charge loss with $8\ \mu m^2$ diode
- ◇ radiation tolerance to 250 kRad & $2.5 \cdot 10^{12}$ n_{eq}/cm^2 at 30°C OK





Spatial Resolution

- **Beam test (analog) data used to simulate binary charge encoding :**
  - Apply common SNR cut on all pixels using $<$N$>$
    $\hookrightarrow$ simulate effect of final sensor discriminators
  - Evaluate single point resolution (charge sharing) and detection efficiency vs *discriminator threshold* for 20x20; 22x33; 20x40; 22x66 μm^2 pixels



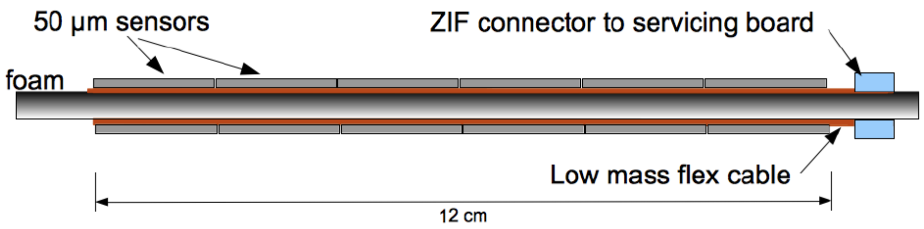
- **Comparison of 0.18 μm technology ($>$ 1 $k\Omega \cdot cm$) with 0.35 μm technology ($\lesssim$ 1 $k\Omega \cdot cm$)**

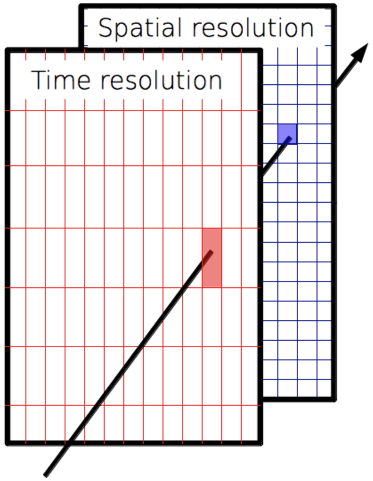
Process ▷	0.35 μm	0.18 μm			
Pixel Dim. $[\mu m^2]$	20.7×20.7	20×20	22×33	20×40	22×66
$\sigma_{sp}^{bin} [\mu m]$	3.7 ± 0.1	3.2 ± 0.1	∼ 5	5.4 ± 0.1	∼ 7

DEVELOPMENT OF ULTRA-LIGHT DOUBLE-SIDED LADDERS

Sensor Integration in Ultra Light Devices

- **2-sided ladders with time stamping for the ILD-VXD :**
  - manyfold bonus expected from 2-sided ladders:
    alignment, pointing accuracy (shallow angle),
    compactness, redundancy, etc.
  - studied by PLUME coll. (Bristol, DESY, IPHC) & AIDA (EU)
    ↪ **P**ixelated **L**adder using **U**ltra-light **M**aterial **E**mbedding
  - square pixels for single point resolution on beam side
  - elongated pixels for 5-50 times shorter r.o. time on other side
  - correlate hits generated by traversing particles
  - expected total material budget $\sim$ 0.3 % X_0

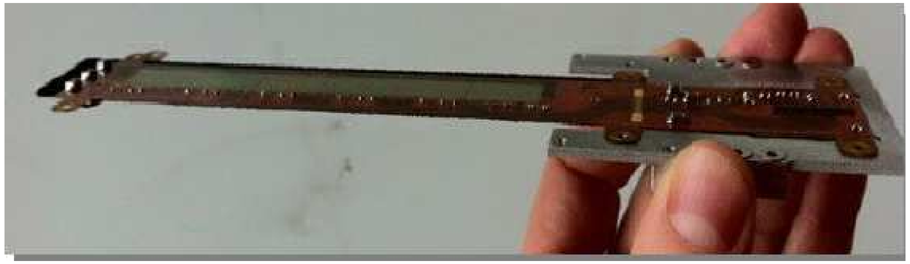


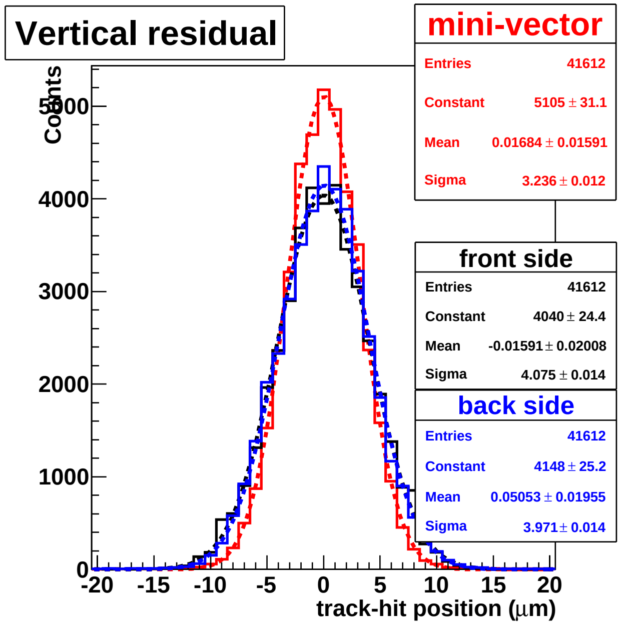


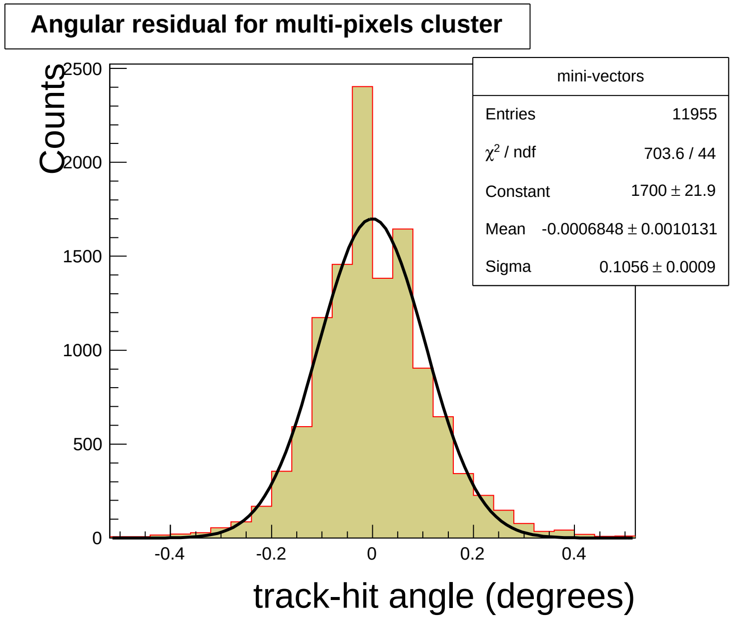
- **Prototypes fabricated :**
  - based on 2×6 MIMOSA-26 sensors mounted on each ladder face
  - mechanical support : 2 mm thick low density SiC foam
  - total material budget $\sim$ 0.6 % X_0
  - beam tests at CERN-SPS (traversing m.i.p.) in Nov. '11

2-Sided Ladder Beam Test Results

- **PLUME prototype-2010 tested at SPS in Nov. 2011:**
  - *Beam telescope : 2 arms, each composed of 2 MIMOSA-26 sensors*
  - *DUT : 1 PLUME ladder prototype (0.6 % X_0)*
    - ↪ *6 MIMOSA-26 sensors on each ladder face ($>$ 8 Mpixels)*
  - *CERN-SPS beam : $\gtrsim$ 100 GeV "π^-" beam*
  - *BT (track extrapolation) resolution on DUT $\sim$ 1.8 μm*
  - *Studies with PLUME perpendicular and inclined ($\sim$ 36°) w.r.t. beam line*
  - *Preliminary results (no pick-up observed): combined impact resolution & pointing resolution*







- **New PLUME proto. under construction with 0.35 % X_0** (X-sect.) ⟼ **beam tests in Q4/2014** (SPS ?)

CMOS Pixel Sensors (CPS): A Long Term R&D

- ***Initial objective: ILC, with staged performances***
  - ↳ *CPS applied to other experiments with intermediate requirements*

EUDET 2006/2010

Beam Telescope

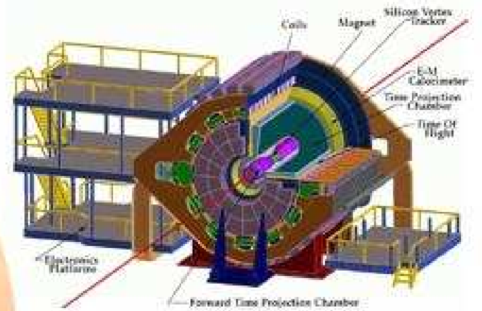
ILC >2020

International Linear Collider

EUDET (R&D for ILC, EU project)
STAR (Heavy Ion physics)
CBM (Heavy Ion physics)
ILC (Particle physics)
HadronPhysics2 (generic R&D, EU project)
AIDA (generic R&D, EU project)
FIRST (Hadron therapy)
ALICE/LHC (Heavy Ion physics)
EIC (Hadron physics)
CLIC (Particle physics)
BESIII (Particle physics)
...

STAR 2013

Solenoidal Tracker at RHIC

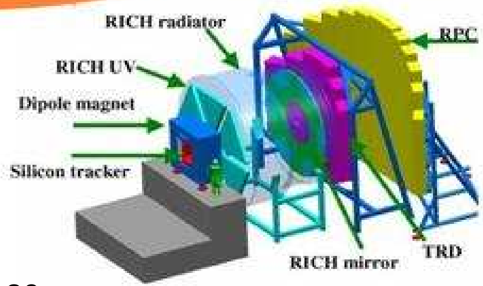


ALICE 2018

A Large Ion Collider Experiment

CBM >2018

Compressed Baryonic Matter



Plans for the Upcoming Years (1/2)

- R&D PLANS ON CPS :
  - realise full scale sensor in 0.18 μm technology : ASTRAL ($\lesssim$ 20 μs) & MISTRAL ($\gtrsim$ 30 μs)
  - achieve O(1) μs time stamping with elongated pixels $\Rrightarrow$ bunch tagging
  - validate concept with 3-bit charge encoding ADC in 0.18 μm technology
  - study alternative approach using Fine Pixel CPS (4-5 μm pitch)

- R&D OF 2-SIDED LADDERS :
  - validate ladder design resulting in 0.35 % X_0 material budget
  - validate ladder concept based on fast/precise sensors on 1st/2nd face (e.g. ASTRAL & MIMOSA-26)
  - validate power pulsing in high magnetic field
  - investigate 2-sided ladder design allowing for $<$ 0.3 % X_0

- FRAMEWORK : R&D CONTINUATION UNTIL EARLY 2020S
  - ALICE-ITS until 2016
  - CBM-MVD until 2018
  - MIMOSA-26/-28 users : EUDET-BT, FIRST, EIC, NA-61, NA-63, BES-III, biomedical & X-Ray -imaging, dosimetry, hadrontherapy, ...
  - H2020, LIA, ...

Plans for the Upcoming Years (2/2)

- 2014 :
  - ⋇ Sensors : realise & validate full scale architectures for ALICE-ITS (ASTRAL and MISTRAL)
  - ⋇ Ladders : realise and test 0.35 % X_0 2-sided ladder based on MIMOSA-26

- 2015 :
  - ⋇ Sensors : realise final prototype for the ALICE-ITS
  - ⋇ Ladders : test of vertex detector "sector" $\equiv$ 3 consecutive pairs of ladders on beam

- 2016 :
  - ⋇ Sensors : production tests of ALICE-ITS sensors $\rightarrowtail$ evolution towards CBM-MVD/FAIR (ASTRAL)
  - ⋇ Ladders : realise 2-sided ladder equipped with 2 different chips (e.g. ASTRAL / MIMOSA-26)

- 2017 :
  - ⋇ Sensors : follow ITS production, production of sensors for CBM-MVD (FAIR)
  - ⋇ Ladders : beam tests of 2-sided ladder equipped with 2 different chips

- 2018 : Start realisation of large sensors dedicated to ILC VXD

SUMMARY

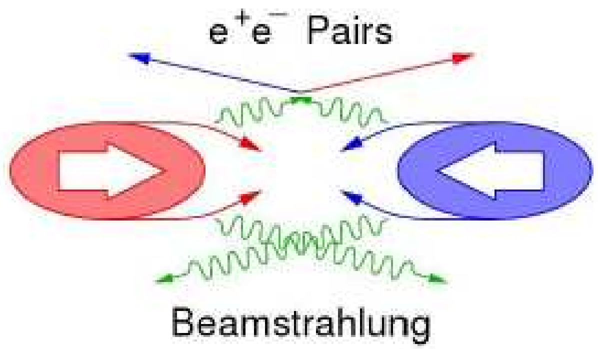
- R&D ON CPS :
  - ⋇ Well established architecture achieved and implemented in STAR-PXL (0.35 μm CMOS process)
    - ↪ extendable to sensors suited to ILD-VXD $\lesssim$ 500 GeV
  - ⋇ Not accessible with 0.35 μm process : standalone tracking, bunch tagging (SiD), 1 TeV running, etc.
    - ↪ 0.18 μm process accessed in 2011 should allow meeting these goals
  - ⋇ 2012-13 allowed assessing process & realising all major sensor architecture elements
    - ↪ Realisation of complete ASTRAL sensor in 2014 (ITS)
  - ⋇ Upcoming years : beyond 2014
    - ○ Final ALICE-ITS sensor & CBM-MVD variant (include all main elements for ILD-VXD)
      - ↪ ILC dedicated sensors in 0.18 μm process from 2017/18 on
    - ○ Investigate FPCPS delayed read-out approach

- 2-SIDED LADDERS : PLUME collaboration
  - ⋇ Prototype based on MIMOSA-26 sensors on the way to achieve 0.35 % X_0
  - ⋇ Upcoming years : beyond 2014
    - ○ Validate concept of complementary sensors with ASTRAL/MIMOSA-26 & power pulsing in strong mag. field
    - ○ Assess added value of double-sided ladders w.r.t. single-sided
    - ○ Investigate possibilities to still reduced the 2-sided ladder material budget $<$ 0.3% X_0

BACK-UP SLIDES

Machine Related Issues

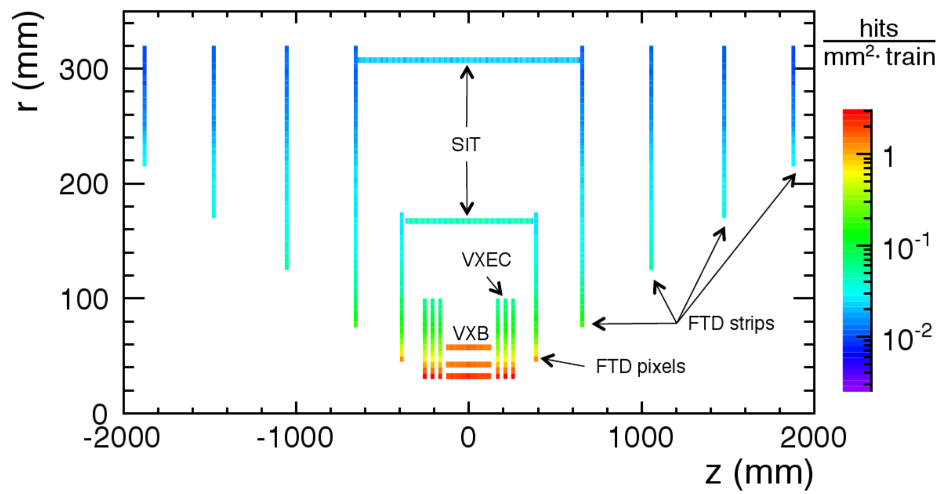
- 2 DIFFERENT MACHINE PROJECTS DRIVEN BY THE LC COMMUNITY :
  - ⋇ ILC ($\gtrsim$ 2026/27 Japanese roadmap) : $\sim$ 0.2–0.5 $\rightarrowtail$ 1 TeV
  - ⋇ CLIC : $\sim$ 0.5 – 3 TeV



- TWO MAIN ASPECTS GOVERN THE DETECTOR SPECIFICATIONS :
  - ⋇ beam related backgrounds :
    - ∘ e^+e^- pairs and $\gamma\gamma$ collisions (CLIC)
    - ∘ drive occupancy & radiation load
      - $\hookrightarrow$ annual load: O(100) kRad & O(10^{11}) n_{eq}/cm^2 **($<$ 10^{-3} LHC load !!!)**
  - ⋇ beam time structure $\Rrightarrow$ $<$ 1% duty cycle

    |||||| |||||| |||||| |||||| ||||||

    - ∘ short bunch trains separated by "long" beamless periods
    - ∘ influences occupancy & allows substantial power saving



- IMPACT OF DIFFERENT ILC AND CLIC RUNNING CONDITIONS :
  - ⋇ different vertex detector specification hierarchy
    - $\Rrightarrow$ different vertex detector geometry and sensor optimisations

Time Resolution Considerations

- TIMING REQUESTS ARE CENTRAL TRACKING AND COLLIDER DEPENDENT :

- OCCUPANCY MANAGEMENT:
  - ⋇ aim for pixel occupancy $\lesssim$ few 10^{-2} - 10^{-3} (tracking strategy dependent)

    $\Rrightarrow$ optimise read-out time $\times$ pixel size (density) $\times$ inner radius

Linear Collider	Bunch train Duration [μs]	N(BX)/train	Inter-bunch Duration [ns]	Inter-train Duration [ms]	Duty Cycle
ILC (500 GEV)	727	1312	554	200	0.36 %
ILC (1 TEV)	897	2450	366	200	0.45 %
CLIC (3 TEV)	0.156	312	0.5	20	0.00031 %

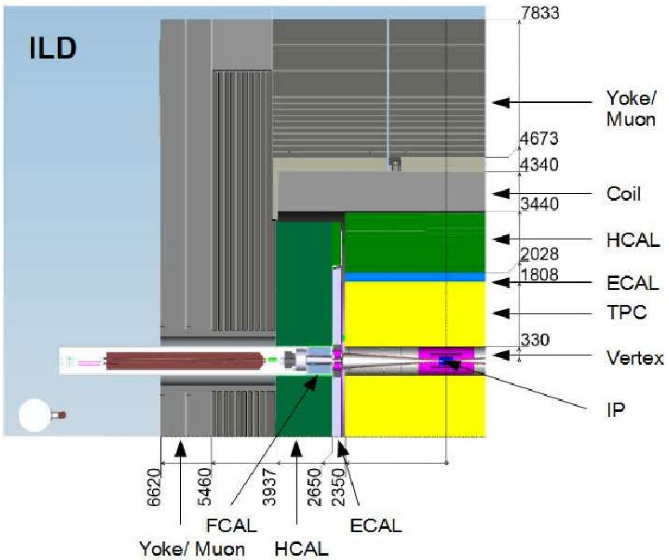
- POWER MANAGEMENT :
  - ⋇ 2 options for ILC :
    - ○ signal read out continuously during train and detector $\sim$ switched of inbetween trains

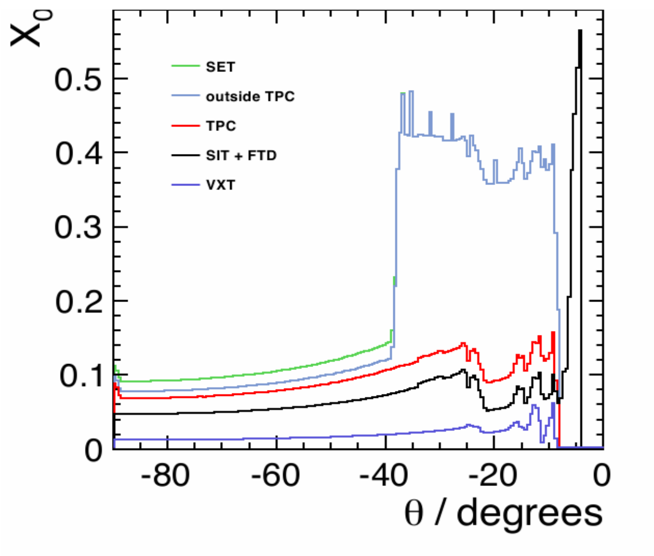
      $\Rrightarrow$ target read-out time depends on tracking strategy: track seed in main tracker or vertex detector
    - ○ charge stored in pixel during train & processed+transfered slowly inbetween trains (immune to potential EMI)

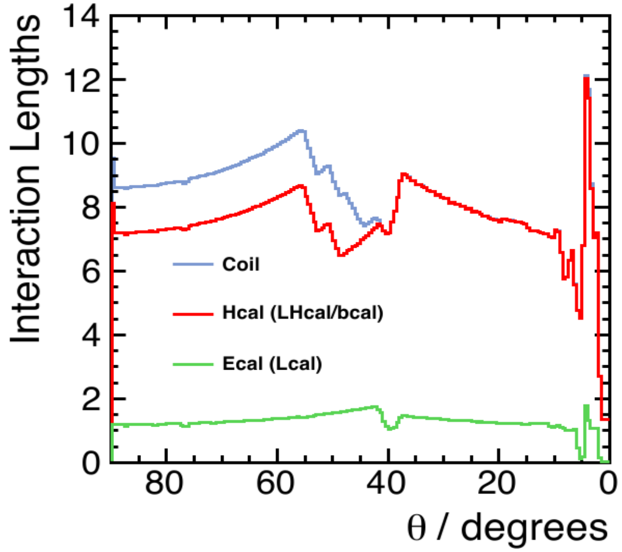
      $\Rrightarrow$ constrains pixel size or/and in-pixel circuitry (timestamp)
  - ⋇ CLIC (3 TeV) : $\lesssim$ 10 ns time (20 BX) resolution required $\Rrightarrow$ continuous read-out

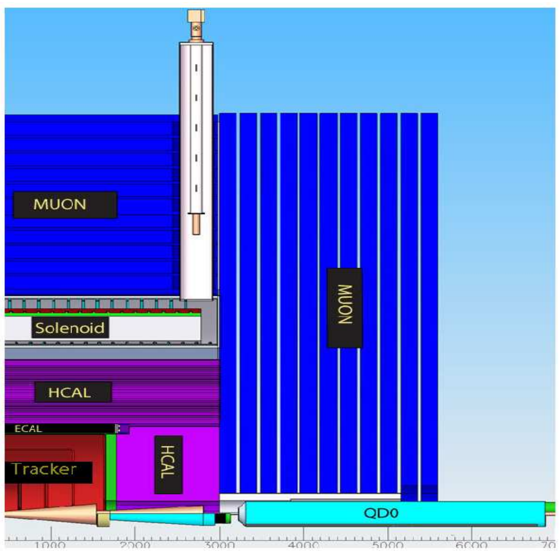
    $\Rrightarrow$ strong impact on (fast) sensor technology
  - ⋇ **General goal :** O(10) mW/cm^2 average power to allow air flow cooling (mat. budget !)

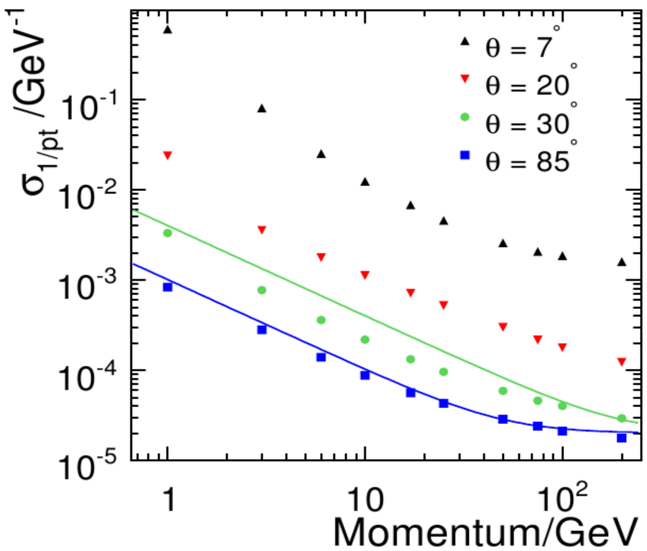
Optimising the Experimental Set-Up for the ILC

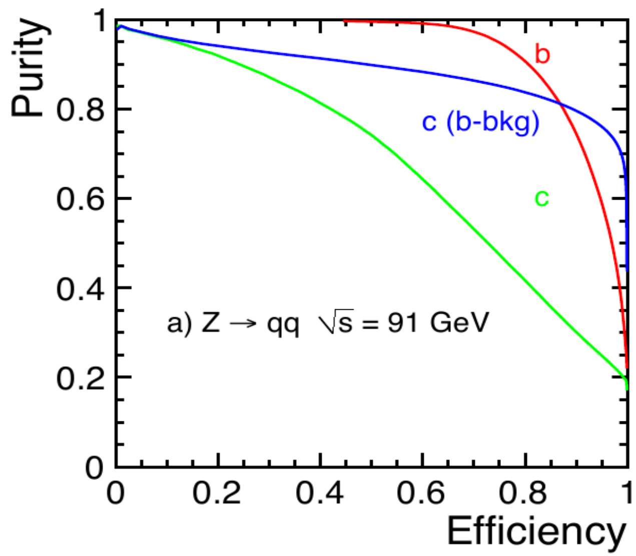












LC Vertexing Devices

- MAIN CHARACTERISTICS OF ILC VERTEX DETECTORS:
  - ⋇ **Geometry :**

    S $\sim$ 0.5 m^2; coverage: $\cos\theta \lesssim$ 0.98

    SiD : short barrel complemented by 3 end-cap disks

    ILD : long barrel geometry

    R_{in} - R_{out} $\simeq$ 15–60 mm

    3 double-sided or 5 single-sided layers $\rightarrowtail$ 0.1–0.15 % X_0/sgle-layer !
  - ⋇ **Sensors :**

    $\sigma_{R\phi,z} \lesssim 3\ \mu m$ (20μm pitch), 50 μm thin, O(10)mW/cm^2 (mean)

    $\Delta t \sim 10\ \mu s$ (ILD) or $\ll 10\ \mu s$ (SiD) depending on tracking strat.

    2 r.o. alternatives : during or inbetween trains (option: 5$\times$5 μm^2 pixels)

    R&D on various sensor techno. & r.o. architectures: exploit t $<$ construct.
- MAIN CHANGES NEEDED FOR CLIC VERTEX DETECTORS:

  Sensors : $\Delta t \lesssim 10\ ns$!!!

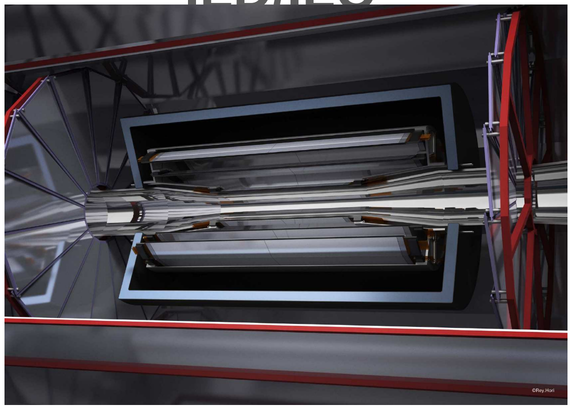
  Geometry : R_{in} - R_{out} $\simeq$ 30–60/80 mm; S $\sim$ 0.7–1.1 m^2
- MAIN R&D TOPICS ADDRESSED :

  high precision low power pixel sensors $\rightarrowtail$ various optimisations

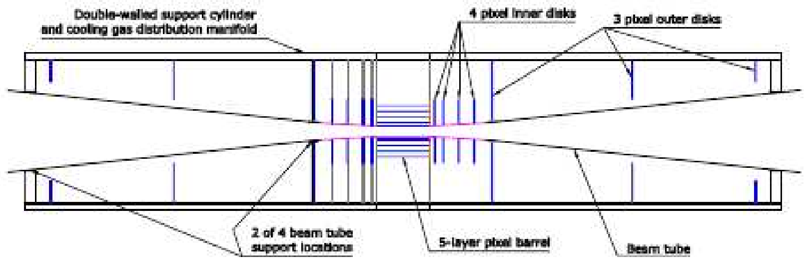
  mechanics and cooling

  power delivery and pulsing

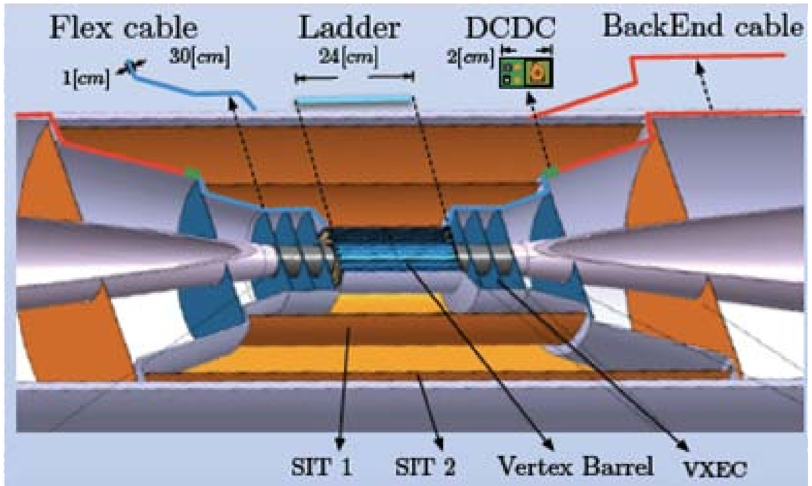
ILD/ILC



SiD/ILC



CLIC



Power Delivery & Cycling

- PIXEL SENSORS : $\sim$ 0.1–1 W/cm^2 $\Rrightarrow$ 1-10 kW/m^2

  $\hookrightarrow$ would require active cooling, generating material budget overheads

- EXPLOIT THE VERY LOW DUTY CYCLE OF THE ACCELERATOR : ILC : few 10^{-3} CLIC : few 10^{-6}

  ⋇ EITHER very slow ($\equiv$ low power) signal processing $\Rrightarrow$ postponed read-out inbetween trains

  ⋇ OR fast signal processing during train (occupancy !) & detectors switched off between trains $\equiv$ power pulsing/cycling

- SUBSTANTIAL DIFFICULTIES :

  ⋇ Low power slow read-out imposes :

  either $\sim$ 5 μm pitch against occupancy $\Rrightarrow$ large Nb(pixels) read out in 200 ms

  $\Rrightarrow$ long serial read-out fitting inbetween trains (// read-out tends to break power limit)

  or in-pixel circuitry to timestamp consecutive hits in same (larger) pixel

  $\Rrightarrow$ conflict between pixel dimensions fitting spatial resolution (small) and those fitting timing resolution (larger)

  ⋇ Continuous read-out with power cycling leads to :

  switching on & off a few grams light ladders in a high B field (3.5 - 5 T) $\Rrightarrow$ F(Lorentz) up to several tens of grams ...

  distributing several hundreds of Amperes shortly before each train arrival

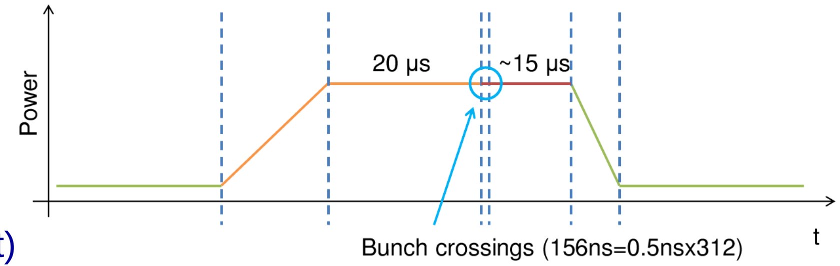
  heat cycle the ladders ...

- TESTS ALREADY STARTED :

  ⋇ DEPFETS: power cycling test outside of magnet sucessful

  ⋇ CMOS pixel sensor power cycling test foreseen in 2T magnet (AIDA project)

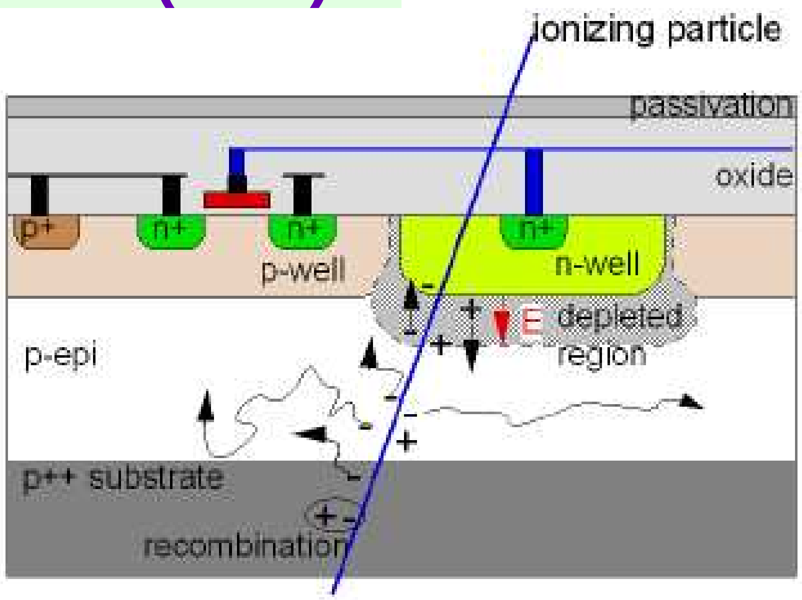
  ⋇ CLIC inner tracking system test bench



CLIC power pulsing scheme

Main Features of CMOS Sensors (CPS)

- P-type Si hosting n-type "charge collectors"
  - signal created in epitaxial layer (low doping):
    Q $\sim$ 70–80 e-h / $\mu m \mapsto$ signal $\lesssim$ 1000 e^-
  - charge sensing through n-well/p-epi junction
  - excess carriers diffuse and/or drift to diode
    with help of reflection on boundaries
    with p-wells and substrate (high doping)
    $\Rrightarrow$ continuous signal sensing (no dead time)



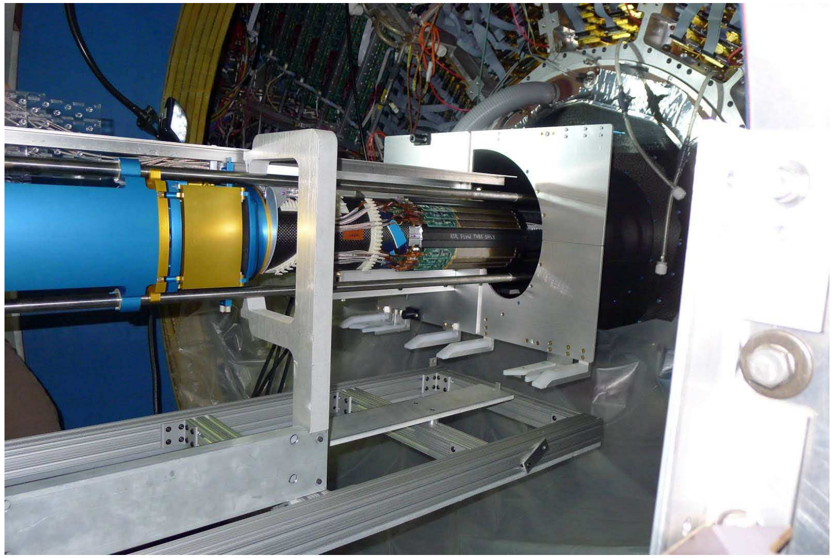
▷ ▷ ▷ since a few years : high resistivity ($> 1\ k\Omega \cdot cm$) epitaxial layer

- Prominent advantages of CMOS sensors :
  - ◇ **granularity :** pixels of $\lesssim 10\times10\ \mu m^2 \Rrightarrow$ high spatial resolution (e.g. $\lesssim 1\ \mu m$ if needed)
  - ◇ **low material budget :** sensitive volume $\gtrsim$ 10 - 20 $\mu m \Rrightarrow$ total thickness $\lesssim$ 50 $\mu m \Rrightarrow$ thinning $\lesssim$ 50 μm
  - ◇ **signal processing μcircuits integrated in the sensors** $\Rrightarrow$ compacity, high data throughput, flexibility, etc.
  - ◇ **industrial mass production** $\Rrightarrow$ cost, industrial reliability, fabrication duration, multi-project run frequency, technology evolution, ...
  - ◇ **operating conditions :** from $\ll 0^\circ$C to $\gtrsim$ 30-40°C

- Main limitation of the approach : CMOS industry addresses a market far from HEP needs
  - ◇ fab. process parametres not optimised to fully exploit the potential of CPS
  - ◇ **BUT recently accessible processes (epitaxial layer, feature size) have opened up new perspectives**

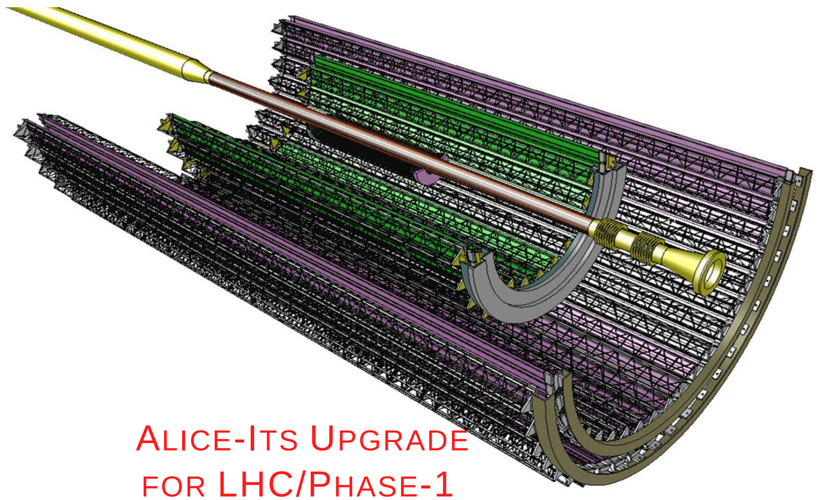
CMOS Pixel Sensors: Present Status

- **ESTABLISHED ARCHITECTURE :**
  - CMOS process : 0.35 μm, 2-well, 4 ML, 15/20 μm & $\sim$ 1 k$\Omega \cdot cm$ EPI
  - in-pixel CDS
  - end-of column discri. (binary encoding)
  - single-row rolling shutter read-out
  - sparse data scan on chip periphery
  - 18.4/20.7 μm pitch $\Rrightarrow$ $\gtrsim$ 3.3.5 μm resolution
  - used in EUDET BT (115 μs) & STAR-PXL (190 μs)
    - ▷ **recent step:** Commissioning of 3/10 STAR-PXL completed at RHIC with pp & ArAr collisions in May-June 2013



STAR-PXL-3SECT INSERTION
PP & ARAR RUN IN MAY-JUNE'13

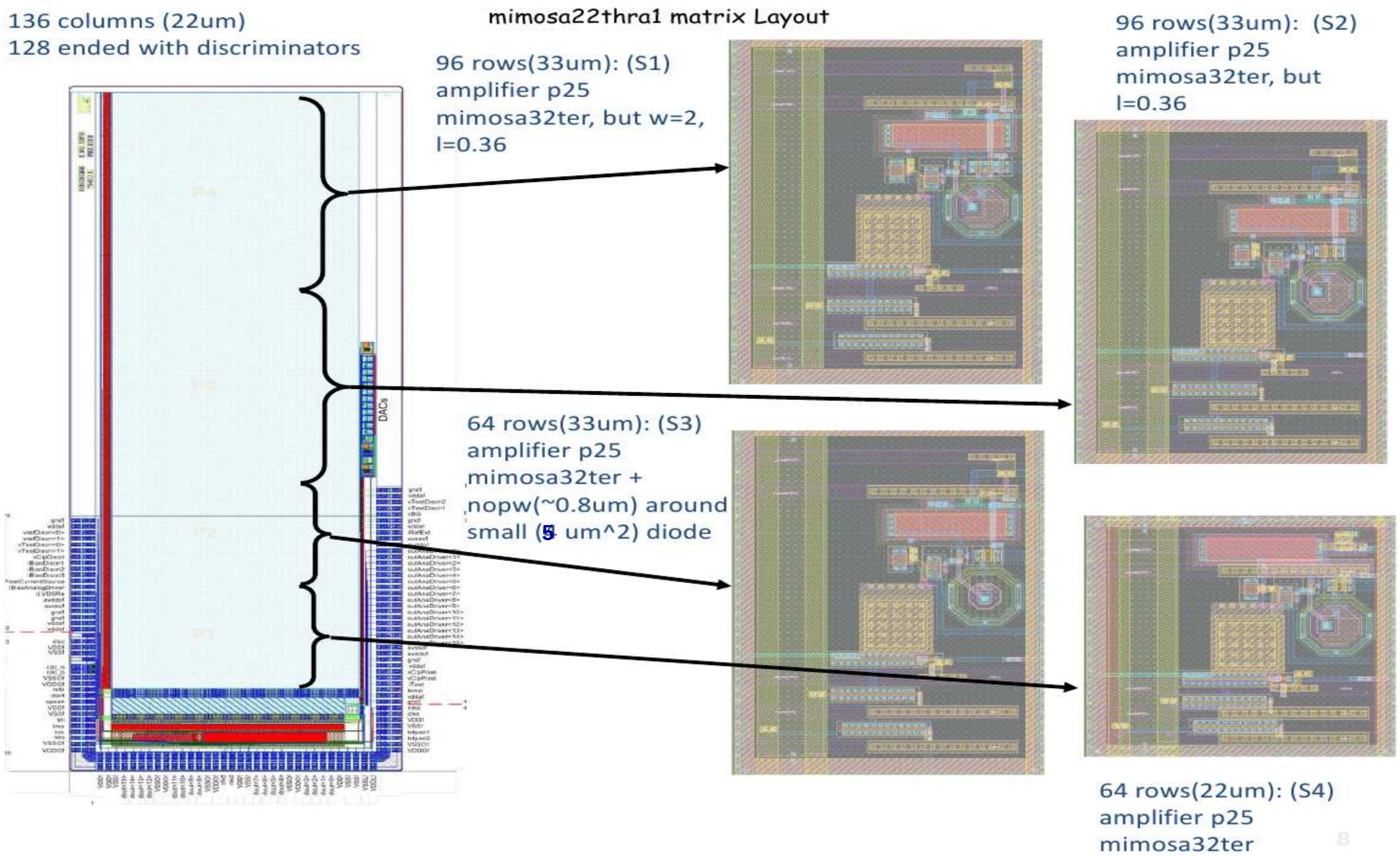
- **NEW PROCESS UNDER STUDY SINCE 2011/12 :**
  - CMOS process : 0.18 μm, 4-well, 6 ML, 15/40 μm & $\sim$ 1-6 k$\Omega \cdot cm$ EPI
  - allows in-pixel discrimination $\Rrightarrow$ faster read-out & reduced power, etc.
  - development driven by ALICE-ITS upgrade & CBM-MVD/FAIR ($\sim$ 20 μs)
    - ▷ **recent step:** Assessment of CMOS proces detection performances & validation of rolling-shutter read-out completed in 2013



ALICE-ITS UPGRADE
FOR LHC/PHASE-1

MISTRAL : In-Pixel + Read-Out Circuitry Studies

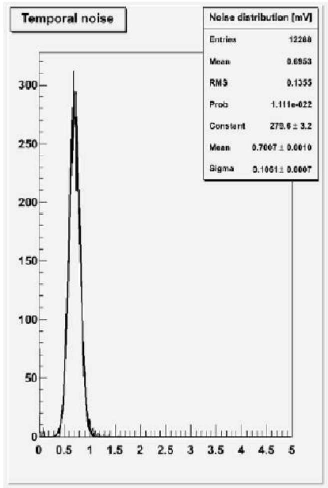
- **MIMOSA-22THRa1 : single row read-out ($\equiv$ MIMOSA-28/STAR-PXL)**
  - ⋇ 128 col. of 320 pixels (22$\times$22/33 μm^2) ended with a discri. + 8 col. without discri. for tests
  - ⋇ In-pixel CDS in 4 variants (2 with enlarged pre-amp T gate against RTS noise)
  - ⋇ Rolling-shutter (single row) read-out $\rightarrowtail$ t$_{int}$ $\simeq$ 50 μs



MISTRAL : In-Pixel + Read-Out Circuitry Studies

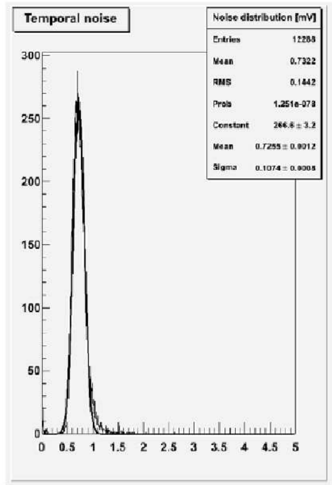
- MIMOSA-22THR threshold scans of single- & double-row read-out to derive TN and FPN
- TN of single-row array:
  - ⋇ S4 pre-amp T gate : L/W = 0.18/1 μm
    - $\hookrightarrow$ TN $\sim$ 17 e$^-$ ENC **+ tail**
  - ⋇ S2 & S1 pre-amp T gate : L/W = 0.36/1 & 2 μm
    - $\hookrightarrow$ TN $\sim$ 16–18 e$^-$ ENC **with minor/no tail**

  $\Rrightarrow$ **Effective mitigation of noise tail by doubling input T gate dimensions**



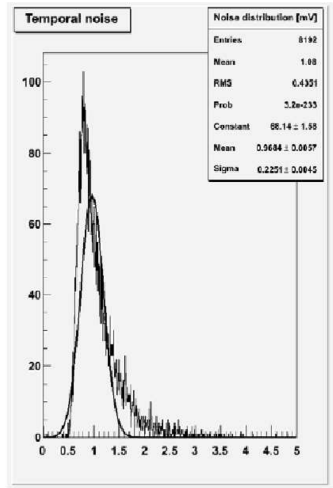
S1 (L & W increase)

Low Res	HR18 >1kO	HR20 >2kO
TN: 695 µV	TN: 670 µV	TN: 682 µV
FPN: 168 µV	FPN:176µV	FPN: 175 µV



S2 (L increase)

Low Res	HR18 >1kO	HR20 >2kO
TN: 732 µV	TN: 692µV	TN: 702 µV
FPN: 178 µV	FPN: 183µV	FPN: 175 µV

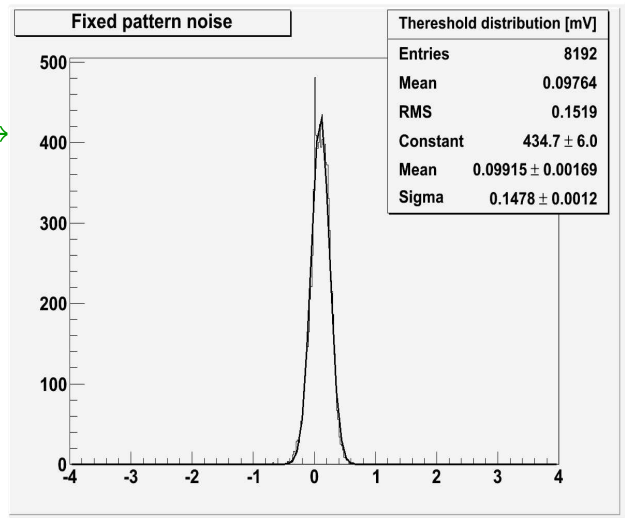


S4 (P25 mi32Ter)

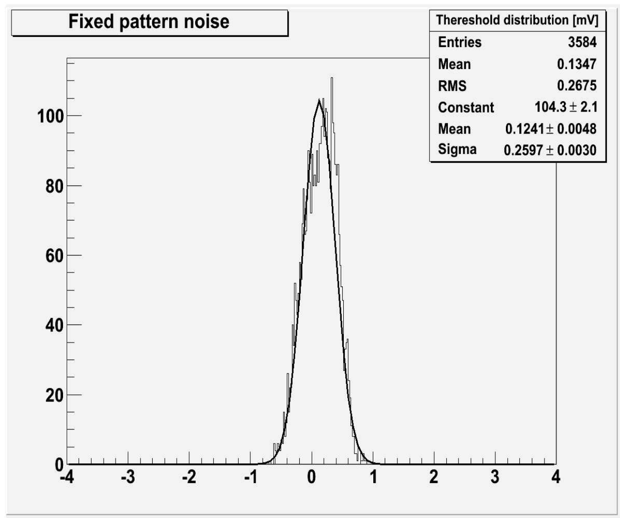
Low Res	HR18 >1kO	HR20 >2kO
TN: 1080 µV	TN: 945µV	TN: 980 µV
FPN: 207 µV	FPN: 208µv	FPN: 212 µV

- FPN of 2-row r.o. (2 discri./col.):
  - ⋇ Concern: analog/digital signals coupling $\Rrightarrow$ FPN $\rightarrowtail$
  - ⋇ Measured FPN (dble-row) $\lesssim$ 5 e$^-$ ENC
    - $\rightarrowtail$ FPN (sgle-row) $\lesssim$ 3 e$^-$ ENC

  $\Rrightarrow$ **Marginal noise increase**



1 discri./col.

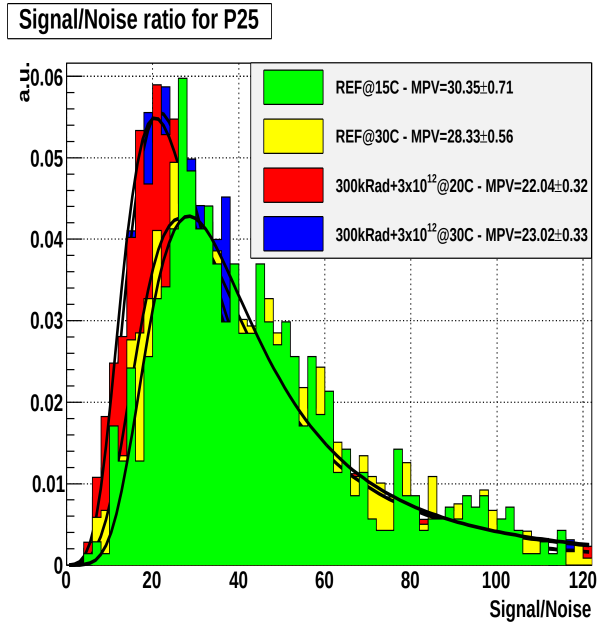


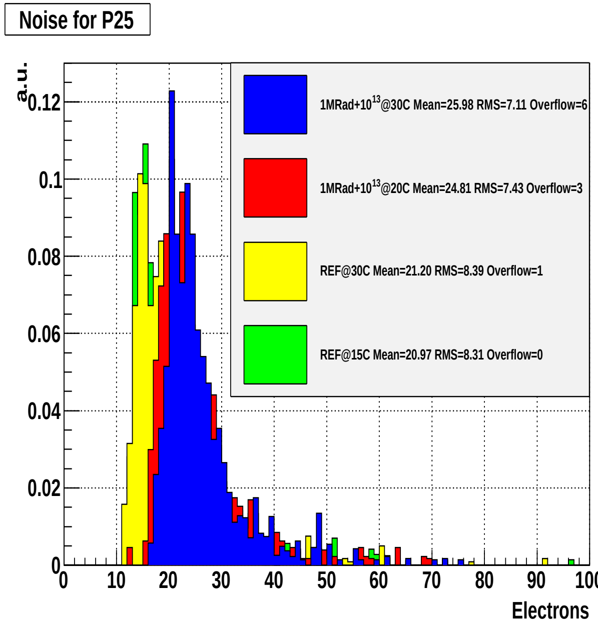
2 discri./col.

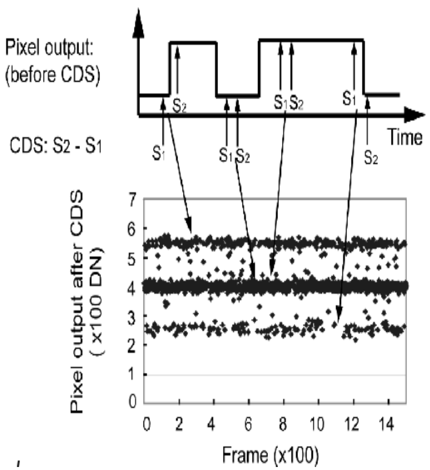
Outcome of 2012 Exploration of the 0.18 μm Process

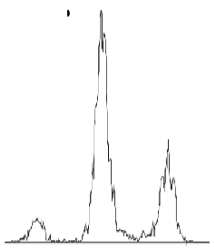
- **Steps validated in 2012 :**
  - ⁎ Several in-pixel amplifier variants lead to satisfactory SNR & det. eff. ($20\times20\ \mu m^2$) incl. after 1 MRad & $10^{13}n_{eq}/cm^2$ at 30°C
  - ⁎ Results pres. at VCI-2013 (J. Baudot)

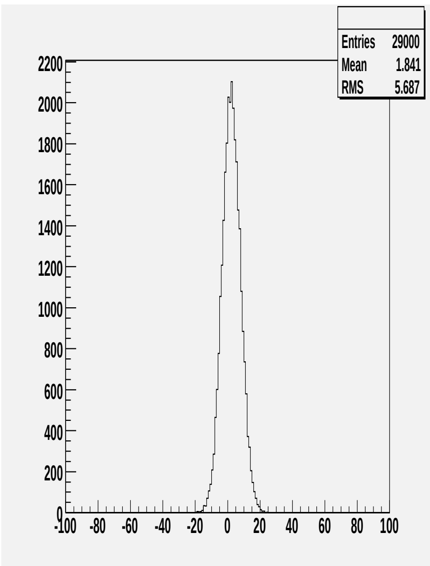
- **Call for improvement :**
  - ⁎ **Pixel circuitry noise : tail due few noisy pixels**
  - ↪ **attributed to RTS noise**
  - ⇒ required optimising T geometries

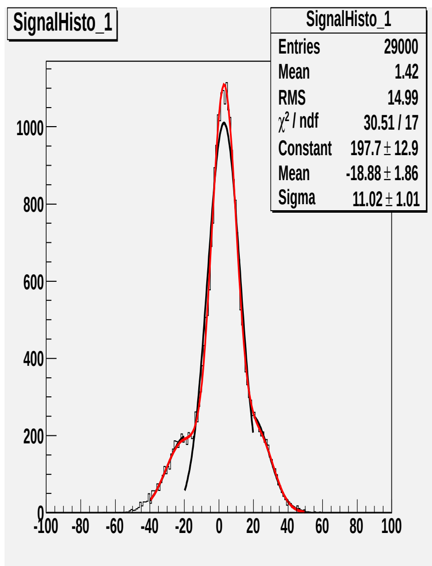


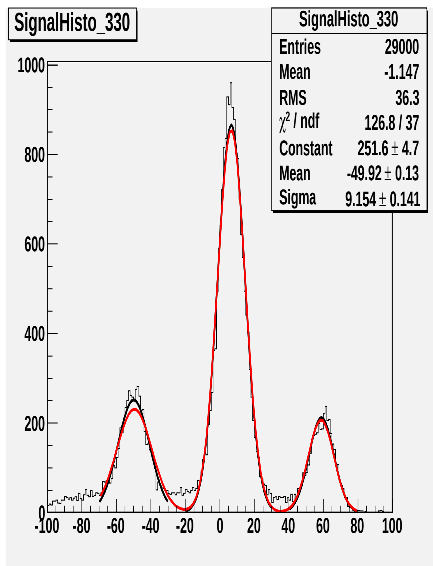






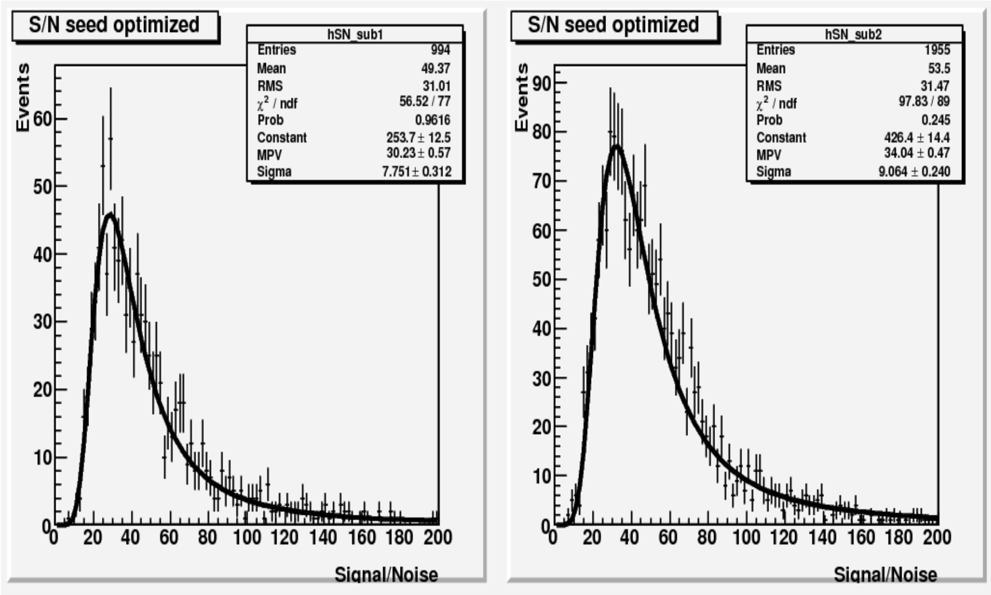






SNR of Pixel Array

- MIMOSA-22THRa1 exposed to $\sim$ 4.4 GeV electrons (DESY) in August 2013



- Analog outputs of 8 test columns (no discri.)

  $\hookrightarrow$ SNR with HR-18 epitaxy, at T=30°C

  ⋇ Noise determination with beamless data taking

  ⋇ Ex: S2 (T gate L/W=0.36/1 μm against RTS noise)
  S1 (T gate L/W=0.36/2 μm against RTS noise)

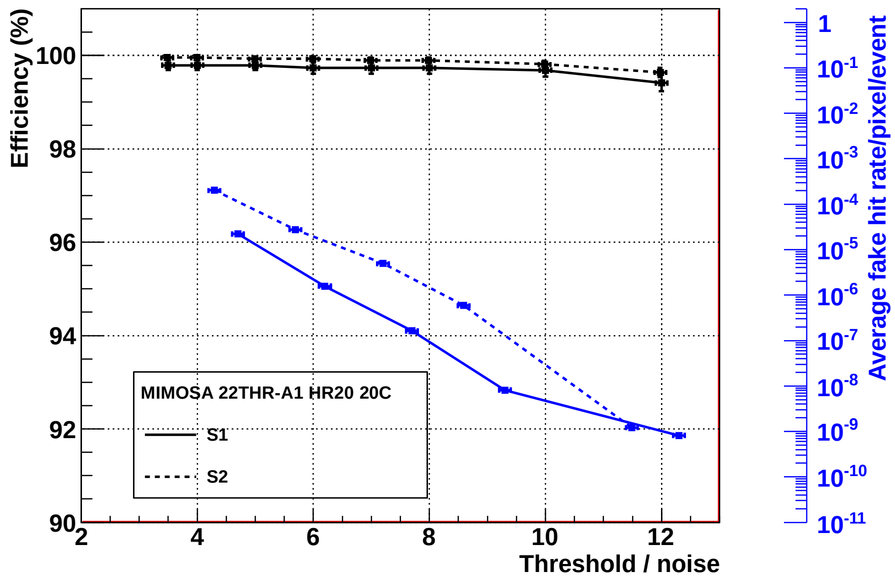
- Results :

  ⋇ Charge collected in seed pixel $\simeq$ 550 e$^-$

  ⋇ Detection efficiency of S1 & S2 $\gtrsim$ 99.5%
  while Fake rate $\lesssim$ O(10^{-5}) for
  Discrimination Thresholds in range $\sim$ 5N $\rightarrowtail$ $>$ 10N

  ⋇ Mitigation of Fake Hits due to RTS
  noise fluctuations confirmed

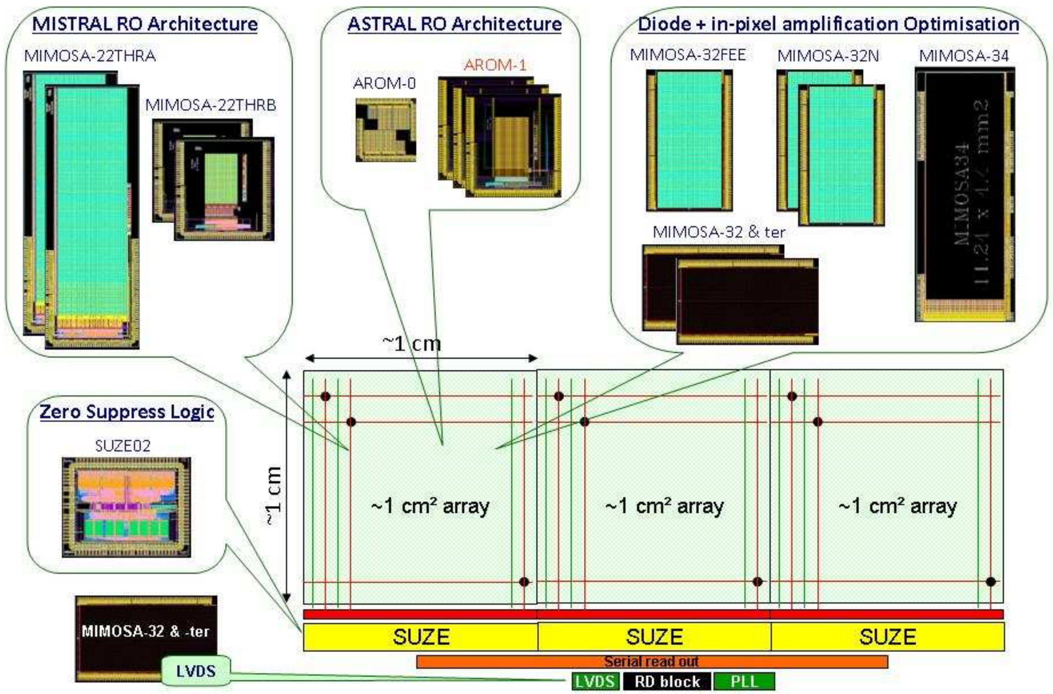
  ⋇ A few 10^{-3} residual inefficiency may come
  from BT-chip association missmatches
  and non-optimised cluster algorithme



CPS : Present R&D

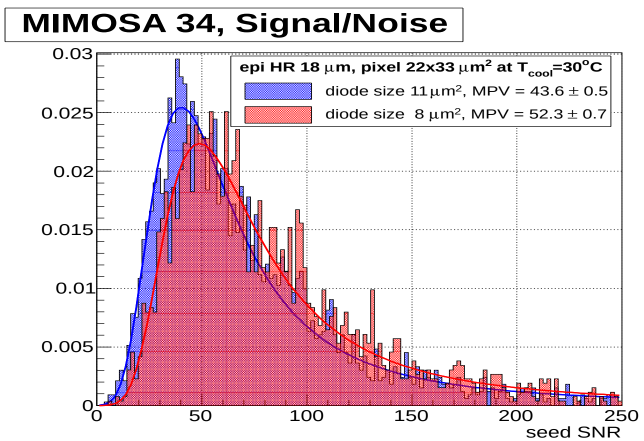
- **Faster read-out for :**
  - ⋇ robustness w.r.t. predicted 500 GeV BG rate
    (keep small inner radius, ...)
  - ⋇ standalone inner tracking capability (e.g. soft tracks)
  - ⋇ compatibility with high-energy running:
    expected beam BG at $\sqrt{s} \gtrsim$ 1 TeV $\simeq$ 3–5$\times$BG (500 GeV)

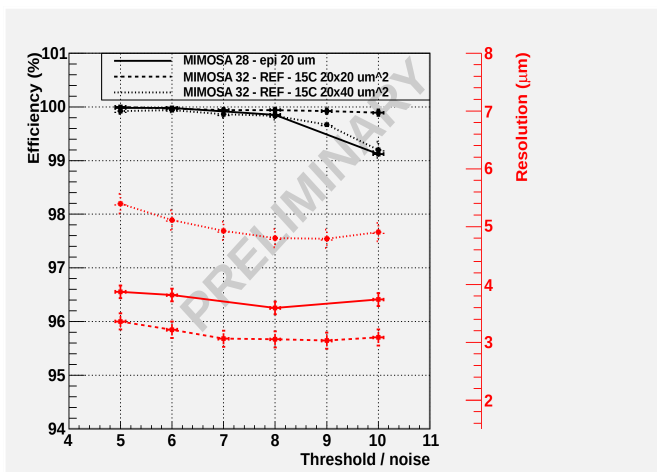
- **Moving to a 0.18 μm imaging CMOS process :**
  - ⋇ Deep P-well & 6 metal $\Rrightarrow$ in-pixel discri. (AROM sensor)
  - ⋇ Epi. layer: 18–40 μm thick, $\rho \sim$ 1–6 k$\Omega \cdot cm$
  - ⋇ Stiching $\Rrightarrow$ multi-chip slabs (yield ?)

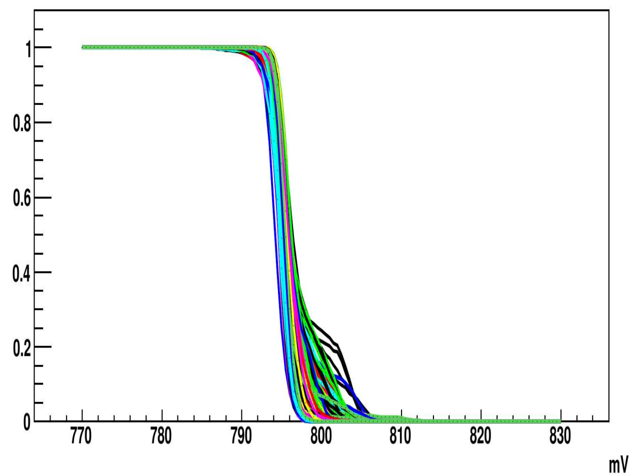


12 diff. chips exploring sensing + r.o. fab. in 2013

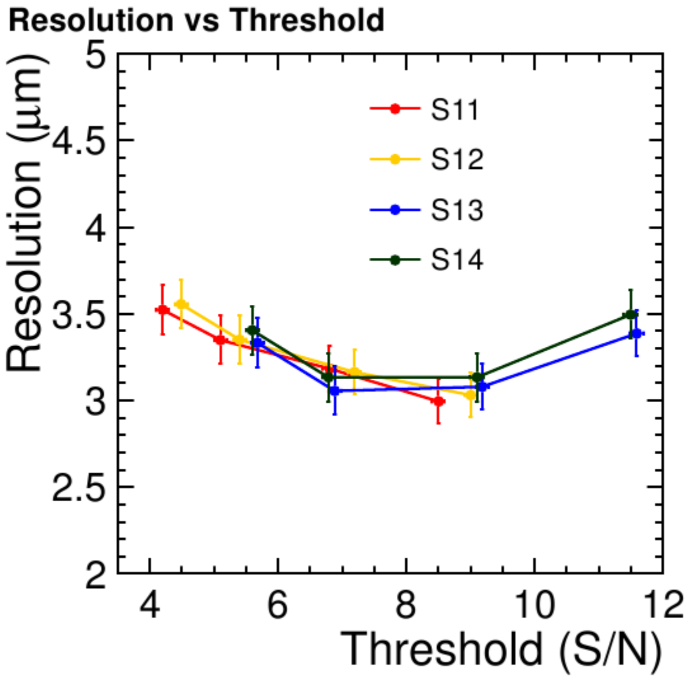
- **2013 (beam) test results :**

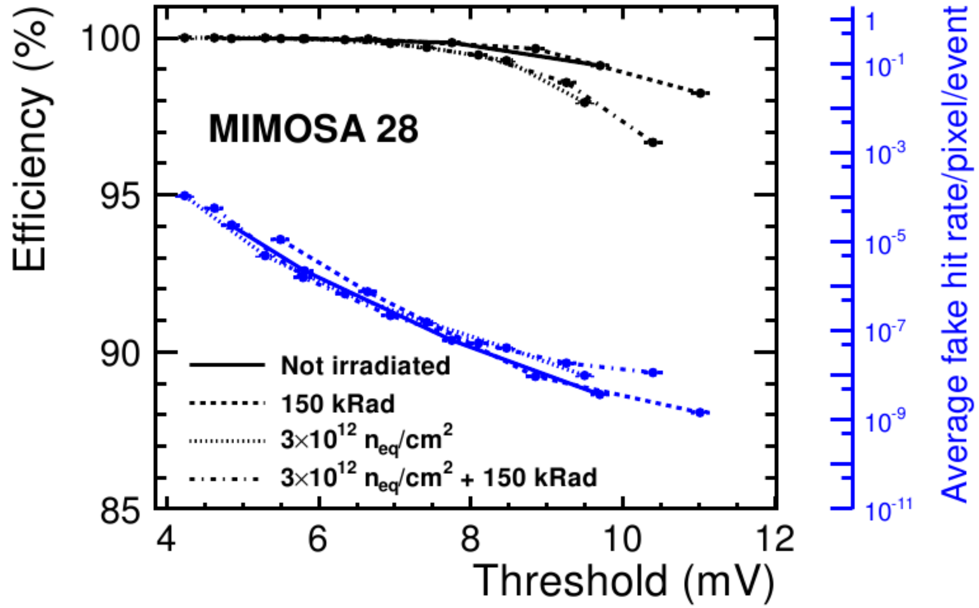


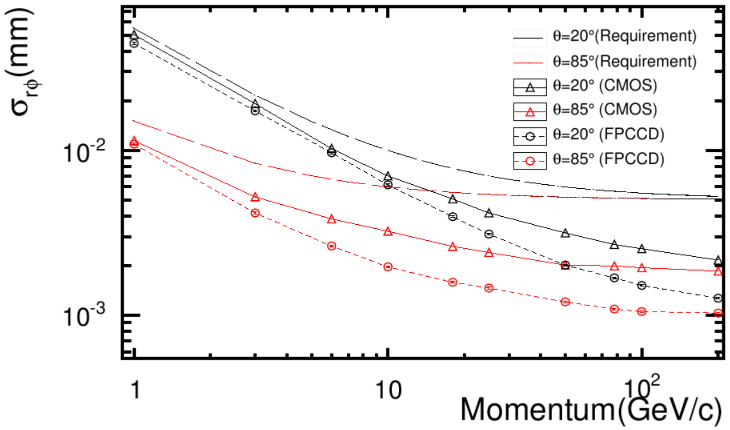


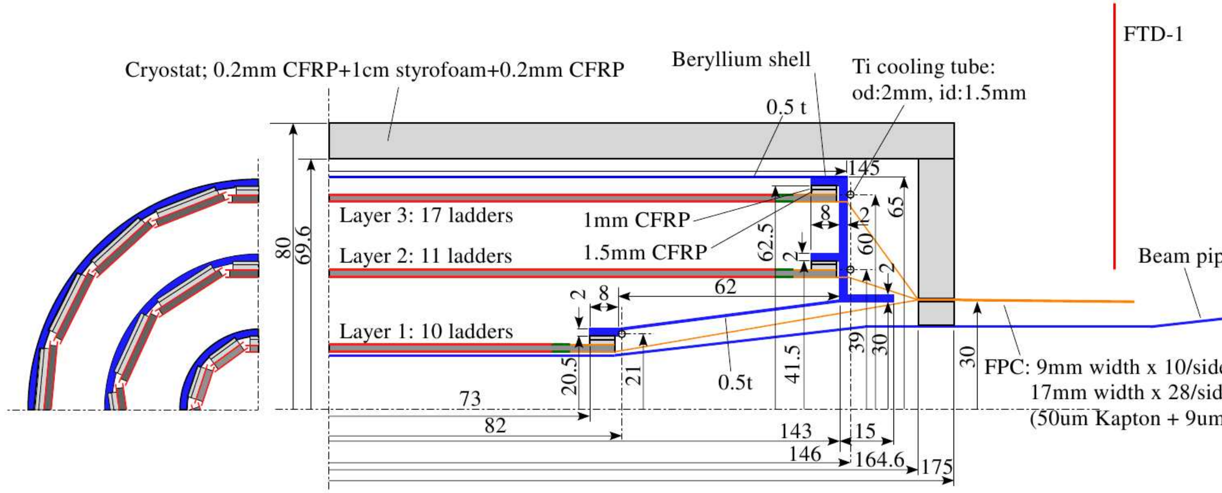


ILD-VXD : DBD


Resolution vs Threshold
Resolution (µm)
Threshold (S/N)
S11
S12
S13
S14


MIMOSA 28
Efficiency (%)
Threshold (mV)
Average fake hit rate/pixel/event
Not irradiated
150 kRad
3×10^{12} n_{eq}/cm^2
3×10^{12} n_{eq}/cm^2 + 150 kRad

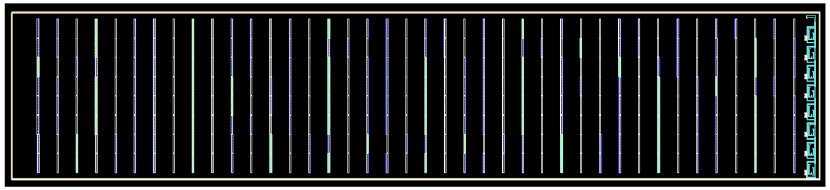

$\sigma_{r\phi}$(mm)
Momentum(GeV/c)
θ=20°(Requirement)
θ=85°(Requirement)
θ=20° (CMOS)
θ=85° (CMOS)
θ=20° (FPCCD)
θ=85° (FPCCD)

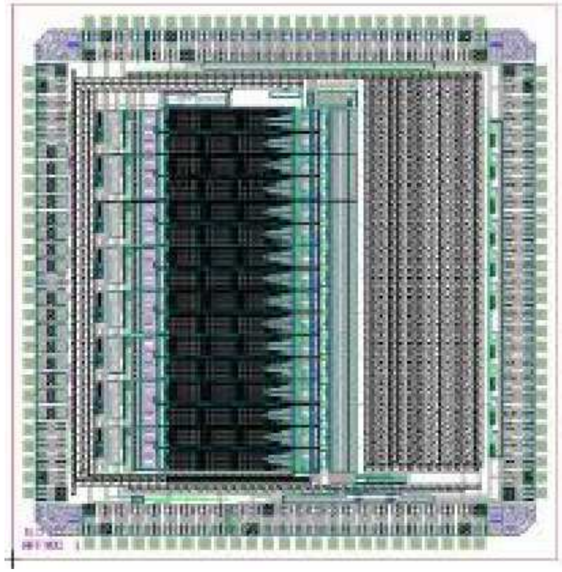

Cryostat; 0.2mm CFRP+1cm styrofoam+0.2mm CFRP
Beryllium shell
Ti cooling tube:
od:2mm, id:1.5mm
FTD-1
Layer 3: 17 ladders
Layer 2: 11 ladders
Layer 1: 10 ladders
1mm CFRP
1.5mm CFRP
Beam pip
FPC: 9mm width x 10/side
17mm width x 28/side
(50um Kapton + 9um

Fine Pixel CCDs: Main Features

- PROMINENT FEATURES OF FPCCDS:
  - Signal charge created in a fully depleted $\sim$ 15 μm thin epitaxial layer
    - $\Rrightarrow$ limited charge spread
  - Very small pixels (5$\times$5 μm^2):
    - ⋇ $\sigma_{sp} \lesssim 1\ \mu m$
    - ⋇ beam related BG rejected by pattern recognition
  - High-res epi and small pixels (occupancy/BX $\sim$ few ppm) used to integrate over full train duration
    - $\Rrightarrow$ devt addresses very low power ADCs
  - Can be thinned down to 50 μm
  - Need -40°C cooling for radiation tolerance purposes
    - $\Rrightarrow$ impact on material budget (modest ?)

62.4 mm long prototype



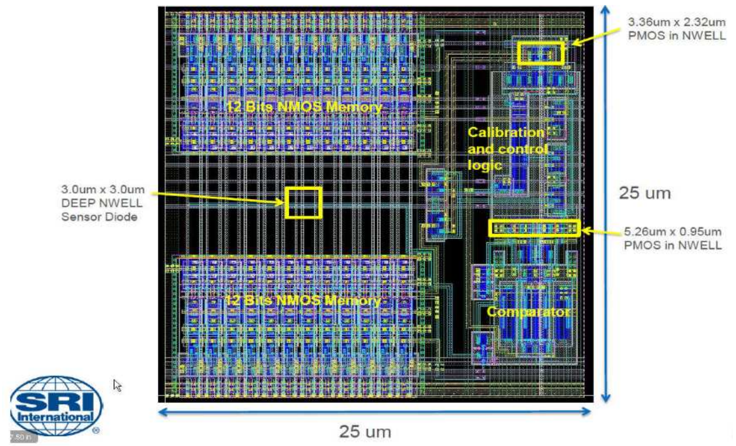


- SEVERAL ESSENTIAL R&D TOPICS ADDRESSED :
  - 5$\times$5 μm^2 pixel matrix detection performances
  - Low power, large bandwidth, r.o. electronics (e.g. 8-bit? ADC)
  - Low mass CO_2 cooling
- Approach not limited to CCDs: should work with CMOS sensors (cost effective, smaller pixels, cooling)

Chronopixel Sensors: Main Features

- PROMINENT FEATURES OF CMOS PIXEL SENSORS:
  - CMOS Pixel Sensor with in-pixel (sgle BX) 12-bit time stamping

    $\Rrightarrow$ tracking based on Vx detector seed (SiD option)
  - Read-out delayed inbetween consecutive bunch trains (power saving)
  - Double-hit timestamping possibility (25×25 μm^2 pixels)



- REQUIRES A VERY ADVANCED (MIXED ?) CMOS TECHNOLOGY :
  - VDSM ($\lesssim$ 90 nm, with deep P-well), for high μcircuitry density

    $\hookrightarrow$ trade-off: pixel size (occupancy) vs in-pixel circuitry complexity
  - Epitaxial layer: thick and resistive enough for cluster spread and SNR

- CUSTOMISED DESIGN IN INDUSTRY (SARNOFF)

  $\Rrightarrow$ cost, design optimisation possibility, devt timeline, ...

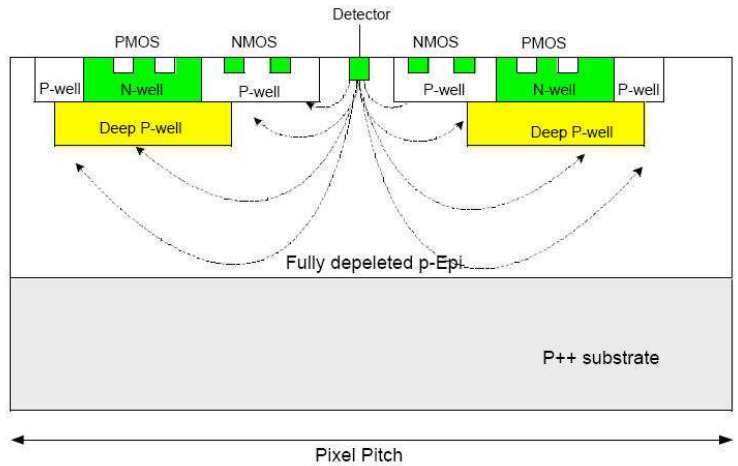
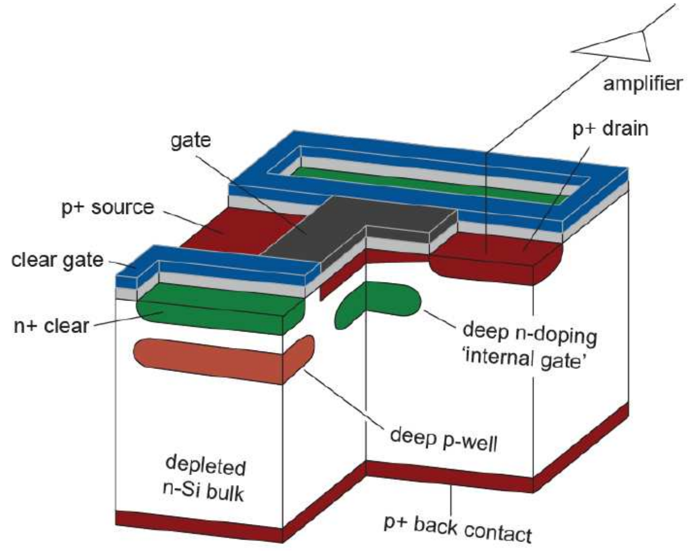
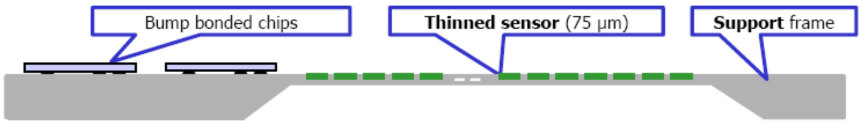


Figure 11.1 Proposed pixel architecture employing the deep p-well layer

DEPFET Sensors: Main Features

- PROMINENT FEATURES OF DEPFET PIXEL SENSORS:
  - Signal charge created in a fully depleted Si substrate and collected by a n-type node ("internal gate") burried under a p-channel FET, delivering a current modulated ($\propto$) by the charge collected on the node
  - External gate to enable read-out $\Rrightarrow$ r.o. chips
  - Clear contact removes charge from internal gate $\Rrightarrow$ switcher chip
  - Steering and signal processing ASICs bonded on ladder edge & end
  - Read-out based on rolling shutter mode $\Rrightarrow$ low power
  - High granularity $\Rrightarrow$ micronic spatial resolution
  - Can be thinned down to 50 μm
  - Sensors are embedded in Si mechanical support
    $\Rrightarrow$ low material budget

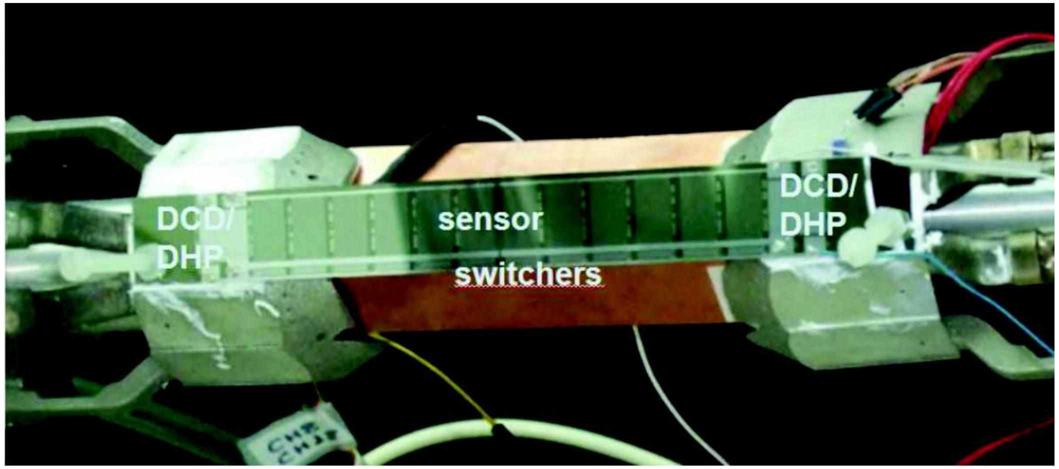




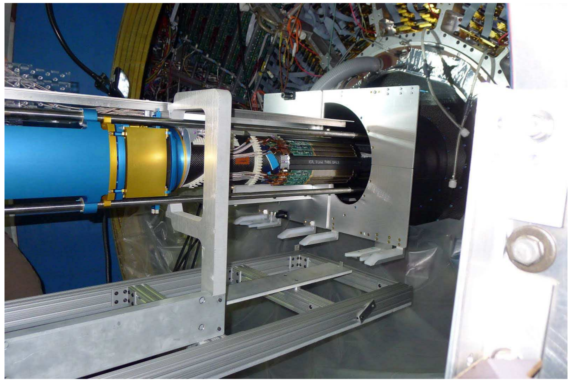
- TECHNOLOGY UNDER PROD/DEVT FOR THE BELLE-II VERTEX DETECTOR:

  $\hookrightarrow$ Several specs close to those of the ILD-VXD inner layer (e.g. $<$ 0.2% X_0)

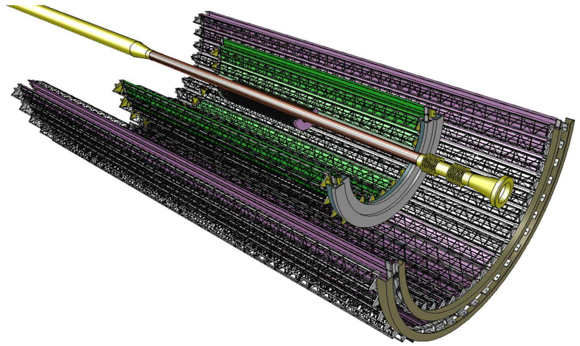
  $\hookrightarrow$ granularity $\times$ speed still to improve



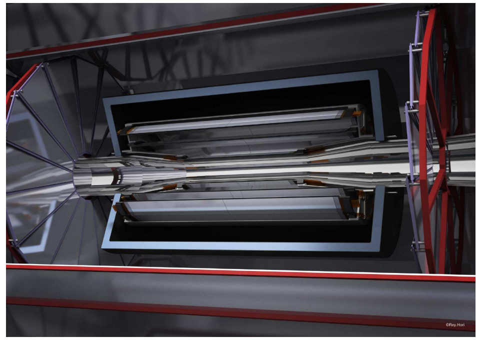
Activités du Groupe PICSEL



- CAPTEURS À PIXELS CMOS (CPS) POUR LE STAR-PXL:
  - 400 capteurs MIMOSA-28 ($9{\cdot}10^5$ pix,, 200 μs, $\sigma_{sp} \sim 3.5\mu m$)
  - installation d'un détecteur de 3 sect./10 le 8 mai 2013 à RHIC ▷▷▷
    $\hookrightarrow$ mise en service avec coll. pp depuis le 9 mai
  - implication IPHC actuelle: 1 IR Elec. (+ suivi des concepteurs)



- CPS POUR L'ITS-2020 D'ALICE: MISTRAL ($30\mu s$) & ASTRAL ($\lesssim 15\mu s$)
  - 7 (baseline) ou 3 couches ($\lesssim 9$ m^2) pixellisées ($\lesssim 10^{10}$ pixels)
  - dévt de CPS en techno. CMOS-$0.18\mu m$ en coll. avec CERN et al.
    $\hookrightarrow$ 2012: techno validée au niveau du pixel (1 MRad$\oplus 10^{13}$ n$_{eq}/cm^2$ à 30°C)
  - 2013-14: prototypage pour valider l'architecture globale avec sparsification
  - implication IPHC actuelle: 6-7 Ing. μElec., 3-4 Ing. Elec., 3 phys. (1 prof.)
  - coll. avec Univ. Frankfurt pour le MVD(CBM): même CPS (vide, T $< 0^\circ$C)

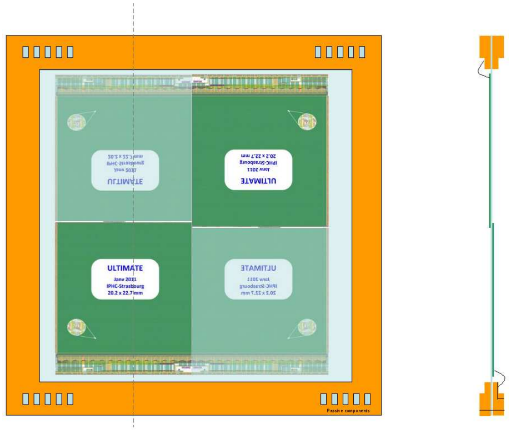


- DÉVTS POUR UN DÉT. DE VERTEX À L'ILC: DBD EN Q1/2013
  - adaptation des CPS(ALICE) pour ILC-500 puis ILC-1000 ($\sim 2\ \mu s$)
  - dévt d'échelles ultra-légères simple- & double-face
  - études d'optimisation de la géométrie du détecteur

Activités du Groupe PICSEL

- ACCOMPAGNEMENT DES APPLICATIONS DE MIMOSA-26 (Télescope EUDET ⟼ 6-7 exemplaires) :
  - Dét. Vx (FIRST/GSI)
  - Proto. MVD (CBM/FAIR)
  - Dét. Vx (NA-61/SPS $\geq$ 2013)
  - Dosimétrie en ligne à protons (ANR QAPIVI, etc.)

- CONTRIBUTIONS AUX APPLICATIONS DE MIMOSA-28 (STAR-PXL) :
  - Imageur protons (TraCal) au GSI/Bio
  - Proto. télescope AIDA (WP-9.3) ▷▷
  - Proto. tracker BESS-3 (FCPPL)



- AIDA (FP-7)
  - dévt d'un capteur abouté de 4×6 cm^2 pour télescope final
    ↪ démonstrateur Dét. Vx eRHIC (LDRD BNL)
  - réalisation d'un secteur simplifié de Dét. Vx pour l'ILC équipé d'échelles PLUME
    ↪ études d'alignement micronique
  - dévt d'une connectique de haute densité pour capteurs à 2 couches (3DIT)
    ↪ coll. avec institut Fraunhofer

- PROBIM (COLL. IMNC): EN ÉMERGENCE
  - imagerie β avec sources internes : dépôt éventuel d'un projet ANR en 2014

- IMAGEUR X: ACTIVITÉ EN EMERGENCE
  - dévt d'un *spectromètre à rayons X* dérivé de MISTRAL/ASTRAL (couche épitaxiée de 30–40μm hautement résistive

Overview of the IPHC Team

- 4 PHYSICISTS :
  - 2 University staff : J.Baudot, A. Besson
  - 1 CNRS staff : M. Winter
  - 1 Postdoc : A. Perez Perez

- 10 ELECTRONICS AND MICRO-TECHNICS ENGINEERS :
  - PICSEL group: G. Claus, M. Goffe, Ch. Illinger, K. Jaaskelainen, M. Specht, M.Szelezniak
  - Micro-technics group : M. Imhoff, O. Clausse, J.S. Pelle, F. Agnese

- 13 CHIP DESIGNERS :
  - CNRS: Ch.Hu-Guo, C.Colledani, F.Morel, I.Valin, H.Pham, W.Dulinski, A.Dorokhov, G.Bertolone, A.Himmi
  - University: G. Dozière
  - 3 PhD students: T.Y. Wang, W. Zhao, Y. Zhou