ATLAS Liquid Argon Calorimeter Upgrade project

High speed and high density readout electronics for the Liquid Argon Calorimeter of the ATLAS experiment at CERN

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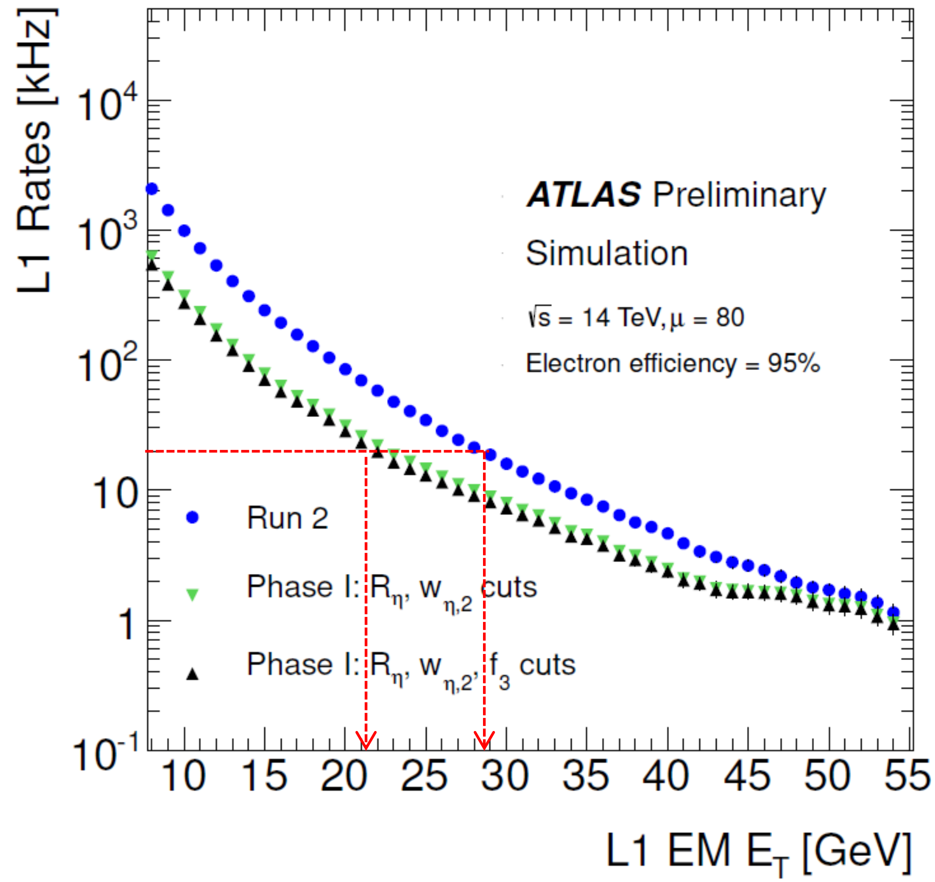
Introduction

- Coming LHC runs
  - High energy upto 14 TeV
  - High Luminosity up to 2 x 10^{34} with 25 ns bunch spacing (Phase-I).

  → Trigger system needs to be upgraded to preserve the acceptance to events with low pt objects (electron, photons and taus).
  - HL-LHC (2025-) will be followed (Phase-II).

- ATLAS Liquid Argon Calorimeter provides the inputs to the trigger for EM objects.

  → Upgrade Electronics in long shutdown (LS2, 2018-2019).

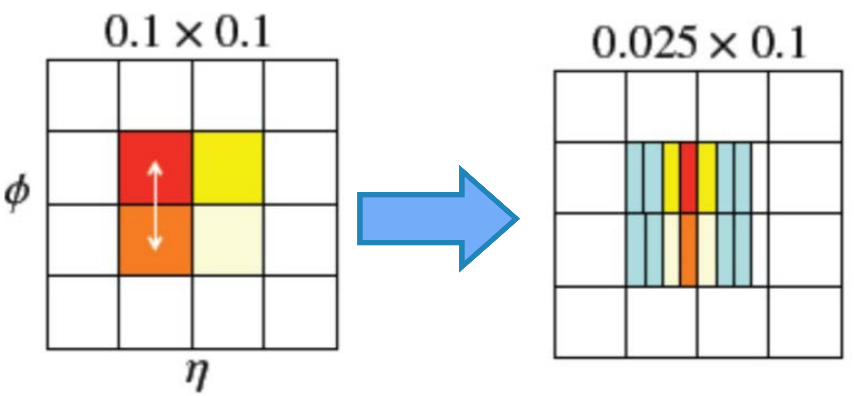


Single EM object can use up to 20kHz bandwidth in L1.

For example, VH(125GeV) signal events will be discarded by using such high E_T cuts.

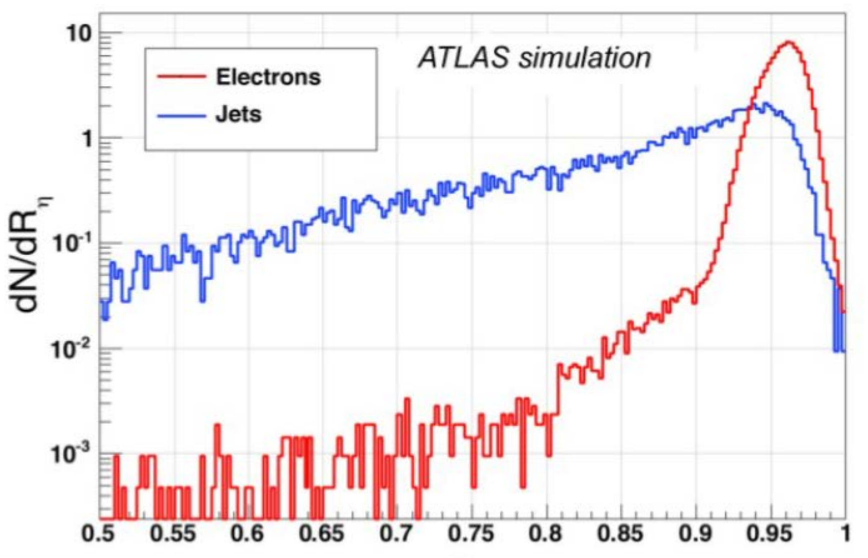
How to reduce the trigger rate?

- Current system
  - Trigger tower size: $\Delta\eta \times \Delta\phi$ = 0.1 × 0.1 (Shower width ~0.08)
  - 1 Tower in EM calorimeter
    → Shower shape is not fully used.



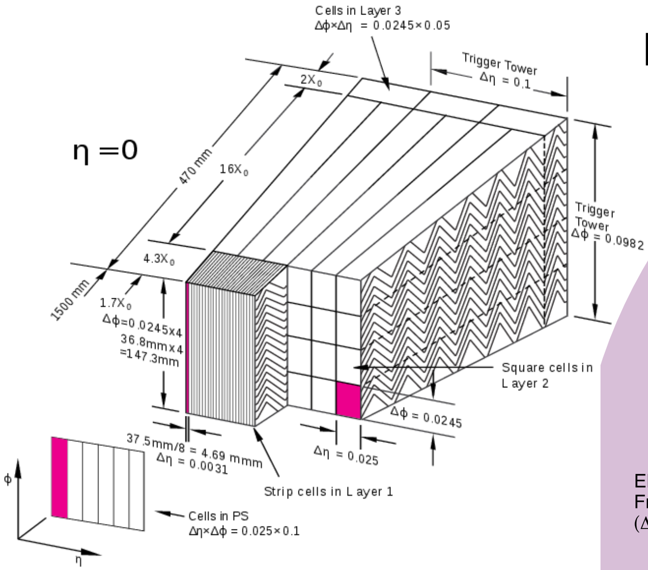
- New system
  Introduce "Super Cell"
  - Longitudinal segmentation
  - Lateral segmentation down to 0.025
    → Utilize narrow EM shower against Jet objects

  Digitize trigger signal on detector
  → Robust energy reconstruction by Digital signal processing (Filtering) against large pileup under high luminosity environment.

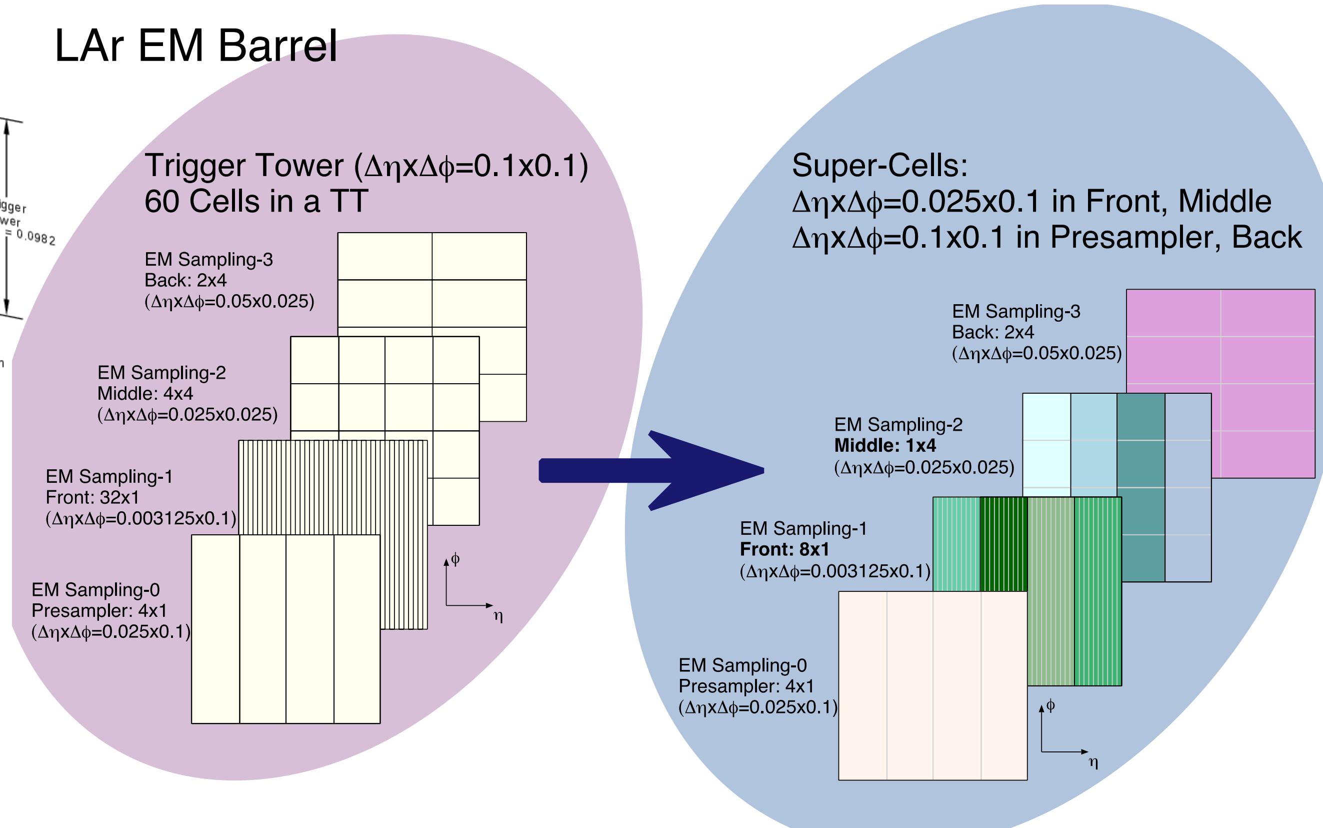


$$R_\eta = \frac{E_{T3x2}}{E_{T7x2}}$$

Trigger tower to Super Cell



LAr EM Barrel



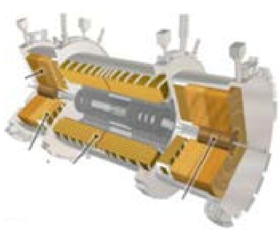
Presampler	Front	Middle	Back
SC_layer=0	SC_layer=1	SC_layer=2	SC_layer=3
SC_region=0	**SC_region=0**	**SC_region=0**	**SC_region=0**
SC_eta=0...13 [Δη=0.1]	SC_eta=0...55 [Δη=0.025]	SC_eta=0...55 [Δη=0.025]	SC_eta=0...12 [Δη=0.1]
SC_region=1	**SC_region=1**	**SC_region=1**	SC_eta=13 [Δη~0.05]
SC_eta=14(15) [Δη~0.1(0.12)]	SC_eta=56..58 [Δη=0.025]	SC_eta=56 [Δη=0.075]	SC_phi=0...63 [Δϕ=0.1]
SC_phi=0...63 [Δϕ=0.1]	SC_phi=0...63 [Δϕ=0.1]	SC_phi=0...63 [Δϕ=0.1]	

Increase number segmentation by a factor of 10.

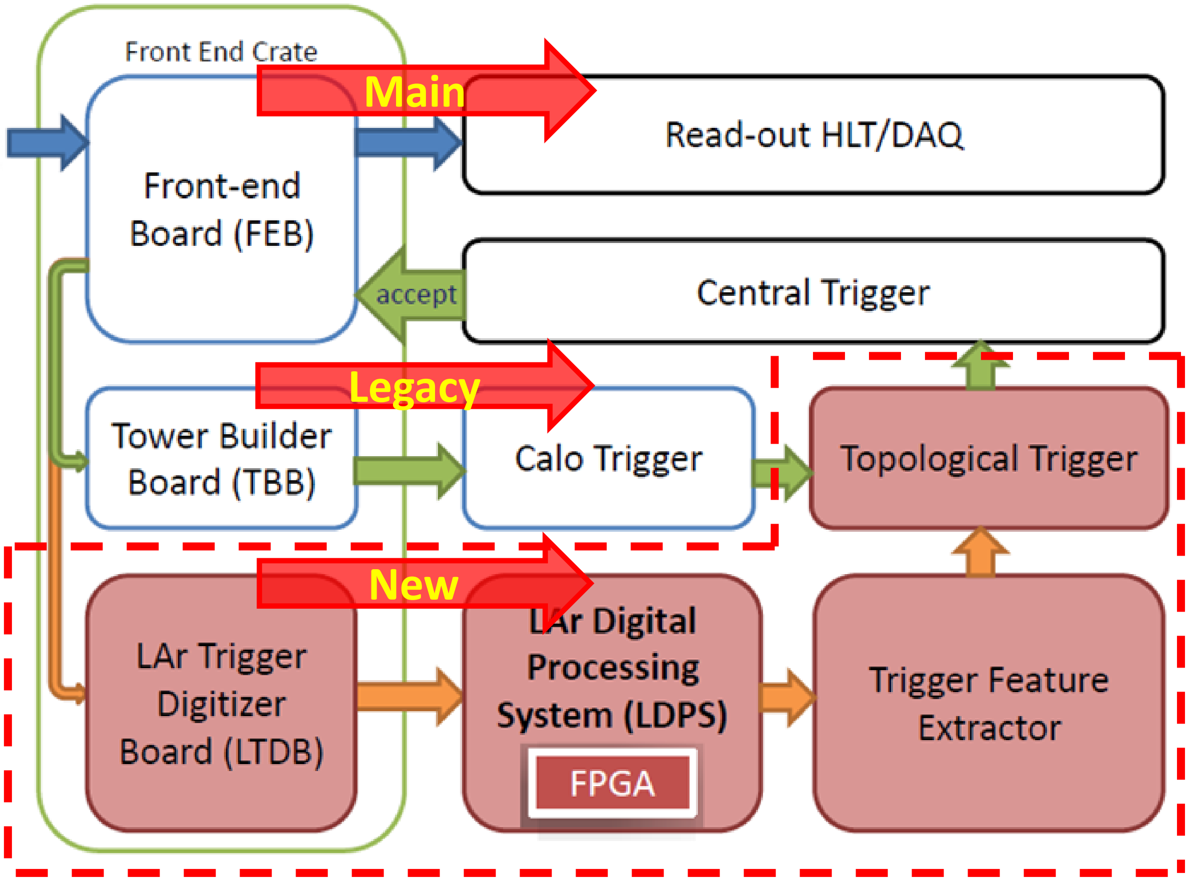
Trigger Tower (ΔηxΔϕ = **0.1x0.1**) →10 Super Cells (ΔηxΔϕ = **0.025x0.1**)

Super Cell (SC): 1 SC each from 1st and last layer, 4 SCs from Front and Middle

Phase1 LAr readout scheme



- Electronics upgrade for Trigger at Phase-I (2018)
  - Introduce new components while keeping legacy electronics
- Introduce Super-Cells (10 times finer granularity)
  - $\Delta\eta \times \Delta\phi$ = **0.1x0.1** → 4 layers with **0.025x0.1** in middle layers.



Phase-1 components shown by the red dashed lines.

New components:

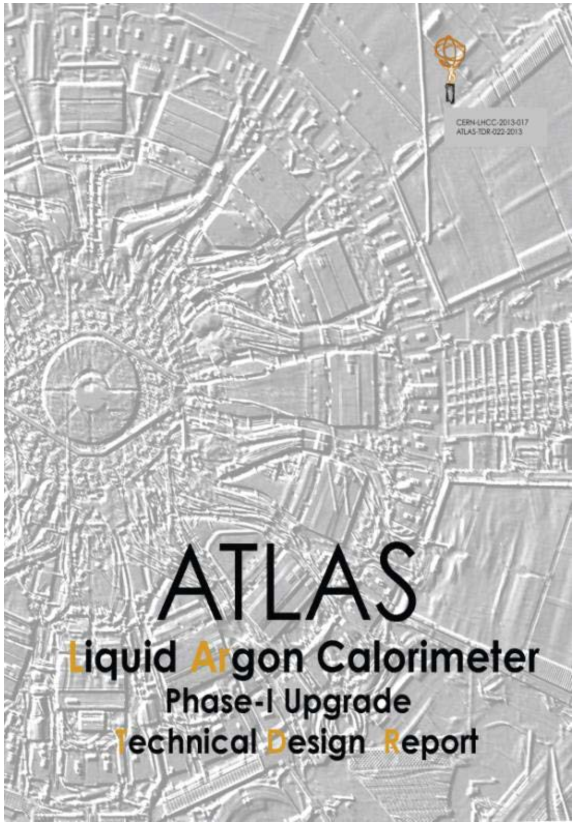
- Summed signals are digitized at Front-End (FE).
- Converted to E_T by Digital signal processing at Back-End with FPGA (BE).
  - Send to Feature extractor (FEX) to make L1-Trigger.

Fast data transfer is key

- **25 Tbps (FE→BE)**
- **41 Tbps (BE→FEX)**

TDR and MOU

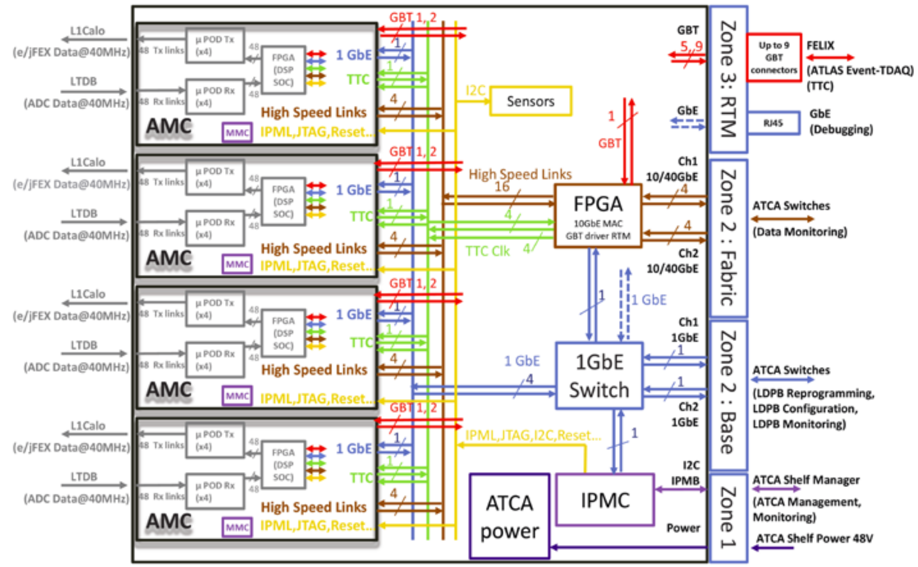
- Technical Design Report for
  ATLAS Liquid Argon Calorimeter Phase-I Upgrade
  https://cds.cern.ch/record/1602230/files/ATLAS-TDR-022.pdf
  – ATLAS released, and LHCC endorsed last December.



Memorandum of Understanding for Phase-1 Upgrade project between CERN and funding agencies.
- Sent to Funding Agencies for signature.

Backend electronics

- Functionalities
  - Receive digital data from **the front-end**
  - Reconstruct energy within ~ 125ns
  - Transmit data to **L1 trigger system**
  - Monitoring these functionalities



- Requirements
  - 4 AMC (advanced mezzanine card) on one ATCA Carrier board
  - AMC for max 320 channels
    - 16cm x 7.4cm (small board)
    - **RX** 12bits x 40MHz x 320 = **153.6Gbps**
    - **TX** 24bits x 40MHz x 320 = **307.2Gbps**

MicroPOD (>100Gbps)

Total, 31 Carrier boards in 3 ATCA crate

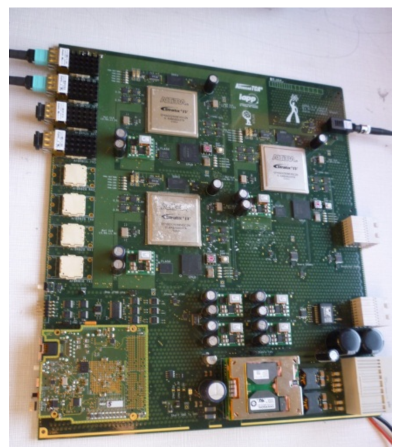
We are collaborating on this development

Activities

We have 3 main activities. CPPM, LAPP and Tokyo work together for each item.

<u>Integration / Operation</u>

- Preparing a test bench at EMF (LAr Electronics Maintenance Facility, close to ATLAS P1) to test LAr trigger components including **Demonstrator**.
- Build infrastructure, firmware and software for new hardware
- Operation for ATLAS data taking.



LPDB demonstrator
Designed by LAPP,
To be installed to ATLAS in June 2014.

<u>AMC R&D</u>

- To understand **Demonstrator**, we made this board in Japan with LAPP design/blueprint.
- Test board with MircoPOD and FPGA.
- Design for prototype AMC .

<u>FPGA Firmware</u>

- Filtering algorithm
- BCID
- Monitoring etc

Test with real data by using **Demonstrator** (during RUN2)
Schematic design for AMC has been started.

Members from CPPM, LAPP and Tokyo

French Group			Japanese Group		
Name	Title	Lab./Organis.	Name	Title	Lab/Organis.
I. Wingerter-Seez	DR	LAPP/CNRS	Y. Enari	Assi. Prof	Tokyo
F. Bellachia	IR-info	LAPP /CNRS	N. Kanaya	Assi. Prof	Tokyo
T. Berger-Hrynova	CR	LAPP /CNRS	J. Tanaka	Asso Prof	Tokyo
S. Cap	AI-elec	LAPP /CNRS	K. Terashi	Assi. Prof	Tokyo
M. Delmastro	CR	LAPP /CNRS	S. Yamamoto	Assi. Prof	Tokyo
N. Dumont-Dayot	IE-elec	LAPP /CNRS	T. Yamanaka	Postdoc	Tokyo
J. Fragnaud	CDD-info	LAPP /CNRS			
N. Letendre	IR-elec	LAPP /CNRS	Y. Minami	D2	Tokyo
G. Perrot	IR-elec	LAPP /CNRS	S. Hisajima	M2	Tokyo
O. Simard	Postdoc	LAPP /CNRS	Y. Minegishi	M2	Tokyo
G. Aad	CR	CPPM/CNRS			
B. Dinkespiler	IR-elec	CPPM /CNRS			
J.P. Cachemiche	IR-elec	CPPM /CNRS			
C. Diaconu	DR	CPPM /CNRS			
C. Meesen	IR-info	CPPM /CNRS			
E. Monnier	DR	CPPM /CNRS			

The three groups work together on these items closely. Hardware development needs frequent exchange information or idea.

Summary and Outlook

- Enhance Trigger performance is crucial item for high luminosity run at LHC.
- On the ATLAS LAr Calorimeter,
  - Upgrade electronics step by step
    Phase-I (2018~2019) : Trigger data path
    Phase-II (2023~2025) : Main readout data path
- For Phase-I upgrade, we are collaborating on the Backend electronics, especially on :
  - Development on the AMC (MicroPOD + highend FPGA),
  - R&D on new filtering algorithm,
  - Install / operate / test the demonstrator.
    - The demonstrator will be installed next month!
- Close and frequent discussion is essential for the project, therefore your support Travel support would re-enforce our young but already very successful collaboration.

BACKUPs

LHC schedule

New LHC schedule beyond LS1

Only EYETS (19 weeks) (no Linac4 connection during Run2)

LS2 starting in 2018 (July) 18 months + 3months BC (Beam Commissioning)

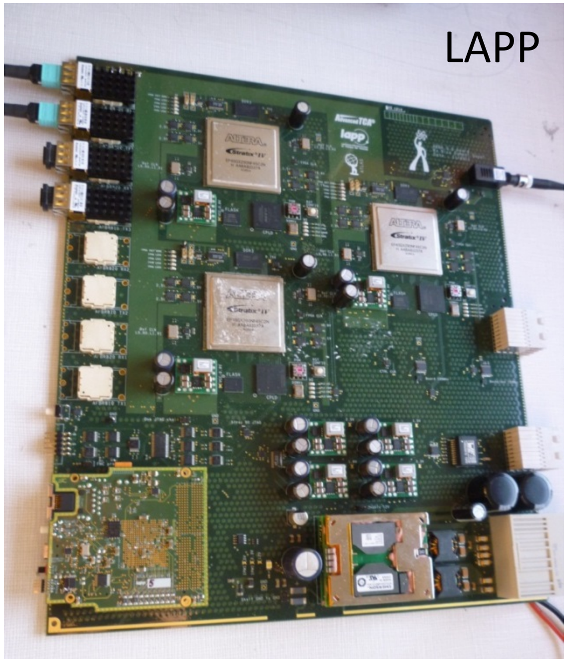
LS3 LHC: starting in 2023 => 30 months + 3 BC

injectors: in 2024 => 13 months + 3 BC

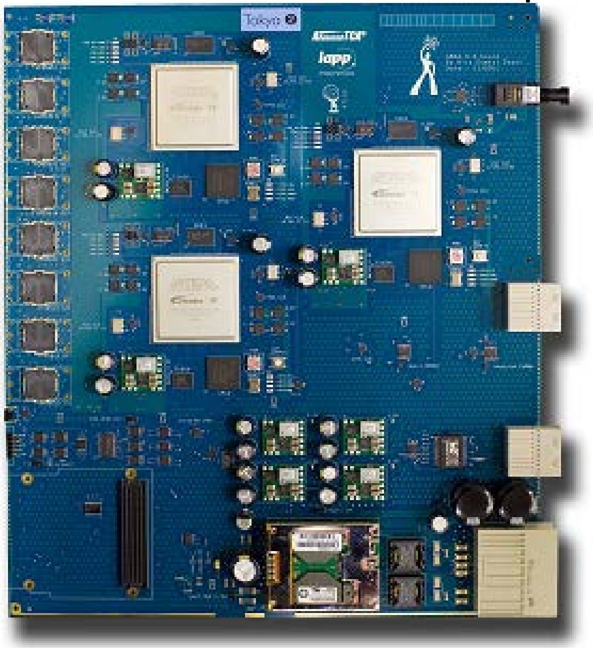
LHC schedule approved by CERN management and LHC experiments spokespersons and technical coordinators
Monday 2nd December 2013

Demonstrator board

- This is a board to test/demonstrate functionalities of the backend electronics of Phase 1 Upgrade.
  - Receive digital signal from the frontend with high-speed links, perform energy reconstruction and so on.
  - Installed during this shutdown, that is, in the next year (2014).
  - Does not affect the existing trigger path. (we MUST confirm it before installing it.)
  - Developed by LAPP.

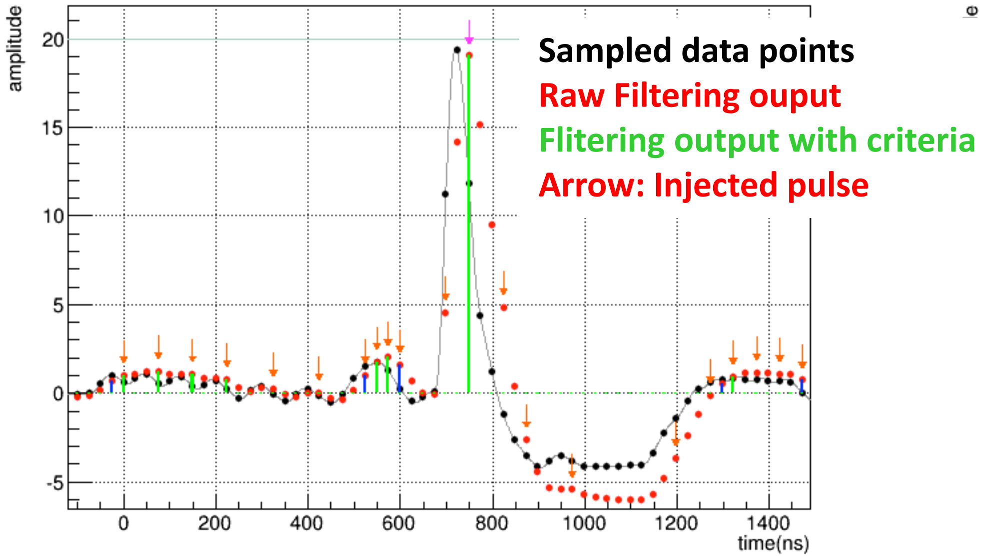


Same one but made in Japan.

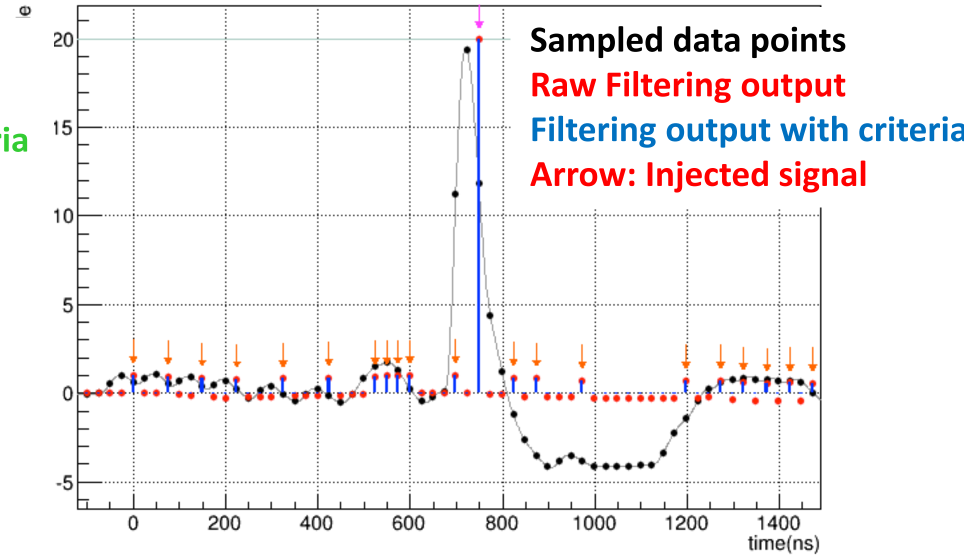


R&D on new Filtering Algorithm

Current algorithm (Optimal filtering)
Use 5 sampled data



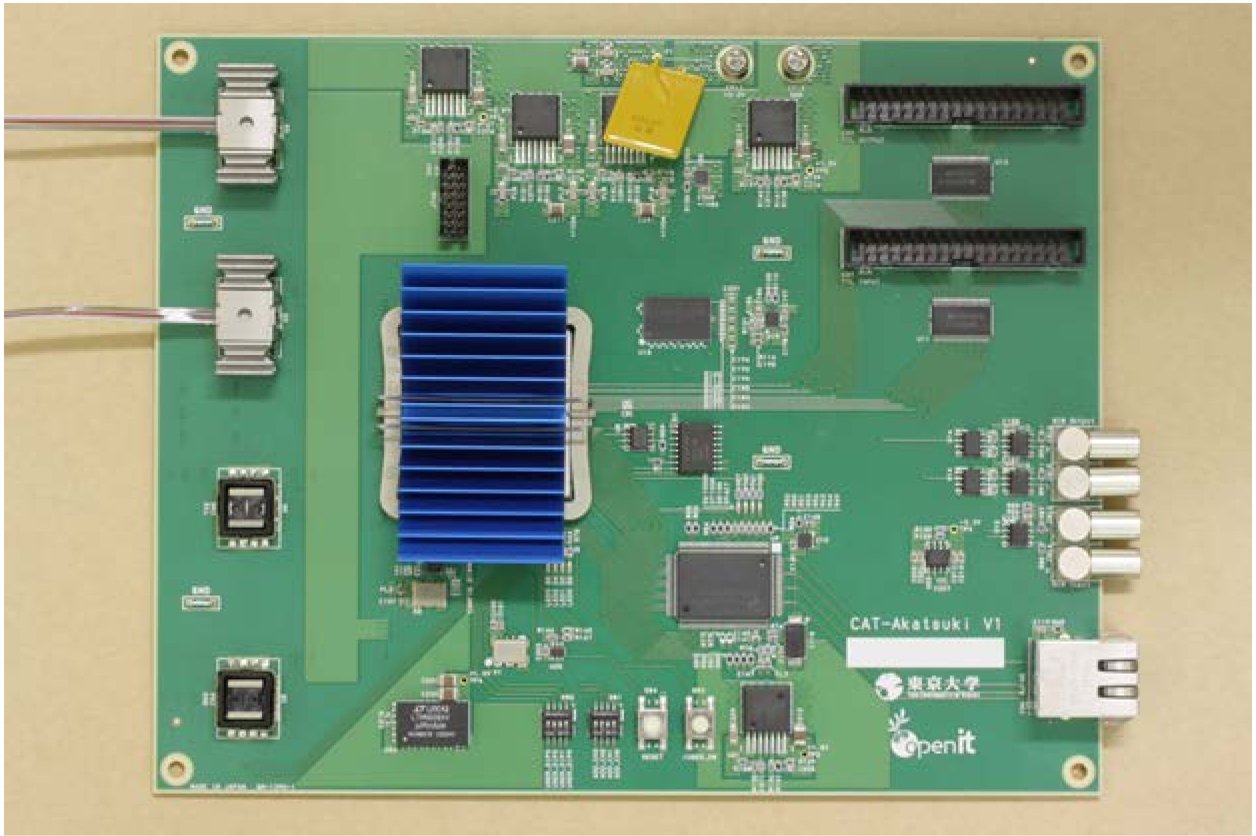
New Filtering Algorithm
Use 32 sampled data with same Latency
→ By using past data, we can recover all real energy even in the over-shoot.



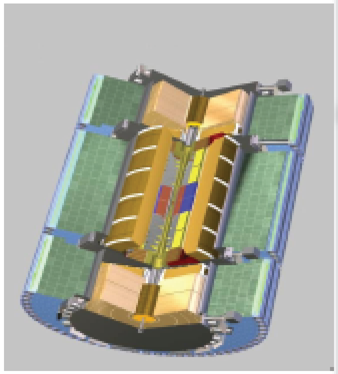
- Injected signal: Amplitude =20（Electron） and Amplitude=1(pileup)
- New Filter can detect all injected signal which are missed with current filter
  - 33% improvement of detection efficiencies for Pileup signals, nearly 100%
- Energy resolution is also significantly improve (by a factor of five)

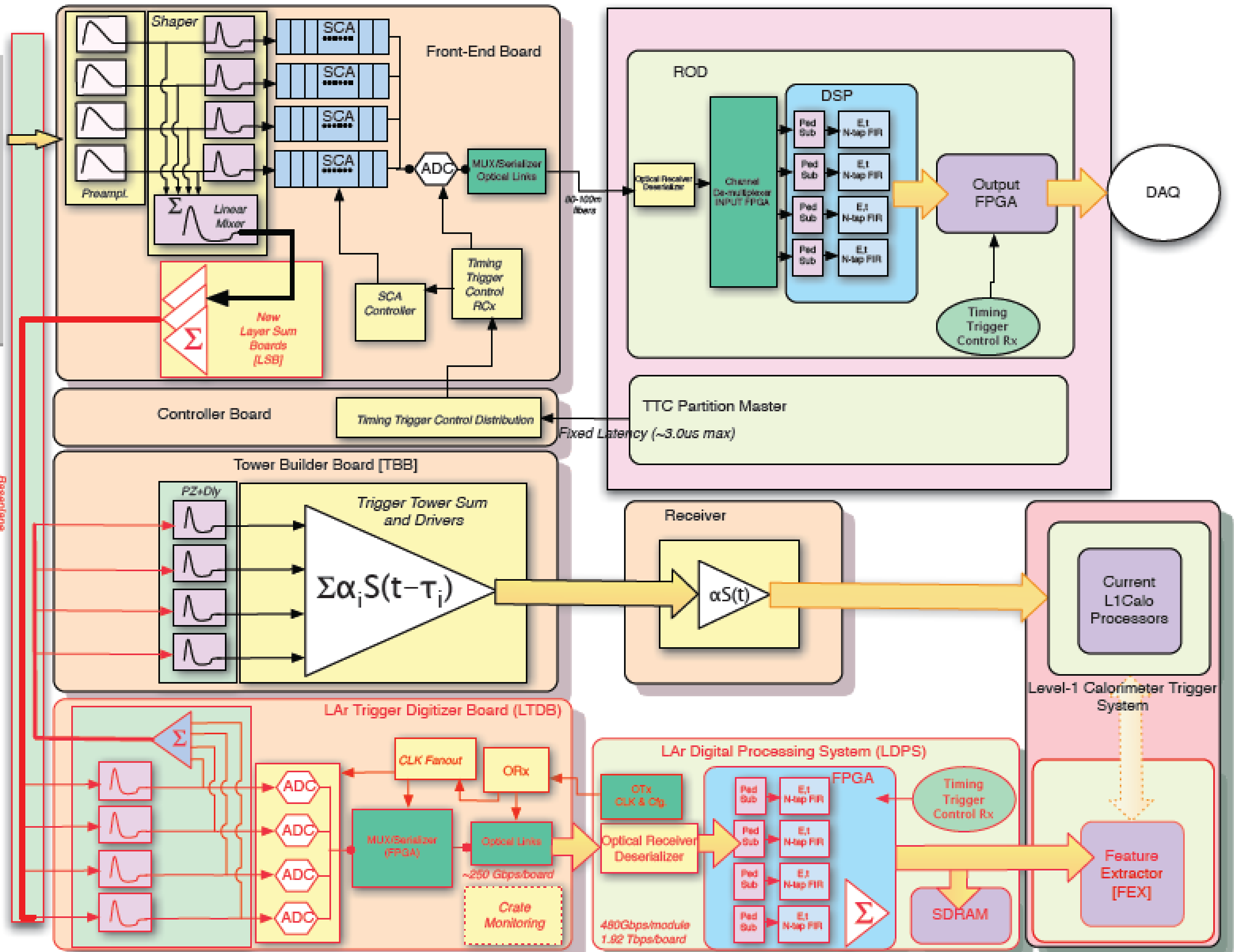
R&D for AMC

- Developing our original R&D board under KEK Open-It project.
  - Our final goal is to demonstrate high-speed and high-density data transfer by using MicroPOD and Xilinx-7 series FPGA.
    - This is key requirement in Phase-I upgrade and also a starting point of Phase-II upgrade.
  - http://openit.kek.jp/project/atlas-emcalo-readout-rd/index.html



Phase1 LAr readout scheme





Given Latency for LAr system

Table 1: Latency estimates (in units of BC) for a LTDB - LDPS system up to entry into FEX. Elements in the table which have been calculated (not measured) are shown in *italics*

	BCs	Sub Total	Total
Time-of-flight to endcap at eta = 2	0.6		
Cable to pulse preamplifier	1.2		
Pulse preamplifier and shaper	0.4		
		2.2	2.2
Digitization on LTDB	*8*		
Multiplexing on LTDB	*1*		
Serializer on LTDB	*2*		
Optical cable (70 m) from LTDB to LDPS	14		
		25	27.2
Deserializer on LDPS	2		
Channel demultiplexing on LDPS	1		
Pedestal subtraction	1		
E, t, Q, N-tap FIR, BCID Calculations	5		
Digital summation	*2*		
Multiplexing on LDPS	*1*		
Serializer on LDPS	2		
Optical cable (15 m) from LDPS to e-jFEX	3		
		17	**44.2**

Front-End
11x25ns = 275 ns

Back-End
14x25ns = 350 ns

Without cabling, FE part:275ns, BE part: 350ns