SAMPIC - P2IO – R&D

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1 Project goals

Ps-range precision time picking is an emerging technique opening a lot of new possibilities for particle physics (particle identification, background reduction,…) or societal applications (TOF PET,..). Since 1990s, most of the fine-timing solutions are built around Time to Digital Converters based on Delay Line Loop. These TDCs can be integrated on ASICs or even since few years in high performance FPGAs. But existing time picking electronics chains based on TDCs are suffering from two main limitations: their timing resolutions is limited by the discriminator and by the quantization step of the TDC. Reaching 10 ps resolution then requires the use of a power-hungry discriminator specially tailored for one type of detector and a very fine-step TDC – requiring a large silicon area- which are both difficult to integrated in an ASIC. The new WTDC (Waveform and Time to Digital Converter) principle, depicted on Fig.1, permits to overcome most of this limitation. In this new type of circuit, the standard DLL-based TDC is associated with a short analog memory – based on Switched capacitor arrays - in which the detector signal is recorded. Then the fine timing of the event is obtained by merging the TDC timing with the one extracted from the digitized analog signal recorded in the SCA. The two main advantage of this method is that the timing of the discriminator is no more critical for the one of the timing measurement and that the method used to extract the fine timing is now a digital algorithm which can be adapted to the detector without changing the hardware.

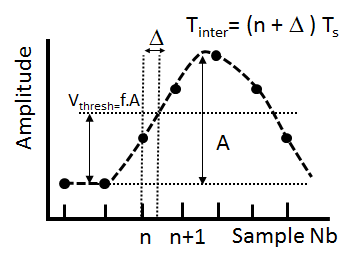
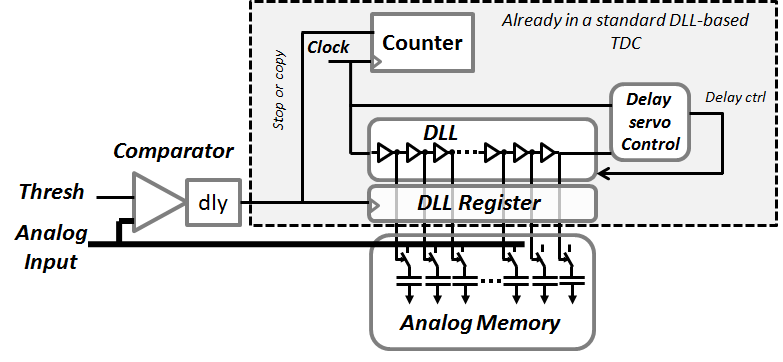


Figure 1: left: Principle of the WTDC, right: example of fine timing extraction using the dCFD algorithm on the digitized samples.

The main goals of the project are:

* Design and manufacture a prototype of a multichannel WTDC chip demonstrating the timing capabilities of this new concept.
* Design, manufacture and evaluate a complete electronics system (hardware, firmware, software) allowing the use of the WTDC in small/medium size experiments.

2 Description of work achieved

A first prototype of WTDC, the SAMPIC0 chip has been designed, manufactured and tested. It integrates 16 independent channels, each consisting of a chain similar to the one shown on Fig.1, with a SCA depth of 64 samples designed to operate up to 10 GSamples per second and the trigger system allowing the chip to self-trigger on events or to operate in more complex trigger modes. The SAMPIC0 chip also includes a digitizing system, based on massively parallel ramp ADCs, allowing converting simultaneously into 11-bit digital data all the cells of the triggered channels (1024 ADC integrated in the chip) as well as all the serialization and control digital electronics required to operate and readout the chip at a high throughput rate . This prototype is much more ambitious than the one initially foreseen as it can already operate at high rate. This chip, shown on Fig. 2, was the first submitted through CMP - the French MPW provider- using the new CMOS 0.18 µm technology from AMS and was also a test vehicle for this technology. For these two reasons, the planning was shifted by almost one year with respect to the initial plans, but stays compatible with the initial plans as this first prototype already matches the goal of the second prototype initially planned. A large part of this work was achieved in the frame of the PhD thesis of Hervé Grabas (defended in December 2013).

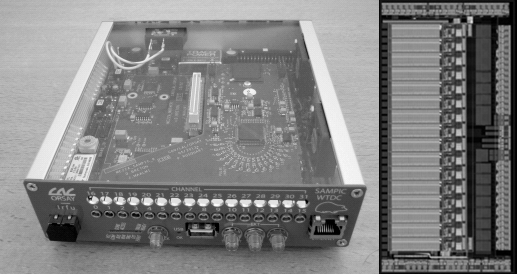


Figure 2: left: picture of the SAMPIC WTDC module. The SAMPIC chip is clearly visible at the center of the mezzanine board, right: microphotography of the SAMPIC0 chip (7 mm2).

In parallel, an acquisition system, shown on Fig.2, was designed. It associates a mother boards equipped with up to two mezzanines each housing a 16-channel SAMPIC chip. This module can be already read by USB and it integrates also all the hardware for a future optical fiber and Ethernet readout. Dedicated software, running with windows and integrating GUI and special display and parameter extraction capabilities for the WTDC operation was also developed. This module and its associated software are used as a test setup for the evaluation of the SAMPIC chip, but can be also used for small setups or test beams.

The SAMPIC0 chip is fully functional and its main characteristics, given in Table 1, are matching our expectations. Figure 3 shows quality of waveforms digitized by SAMPIC

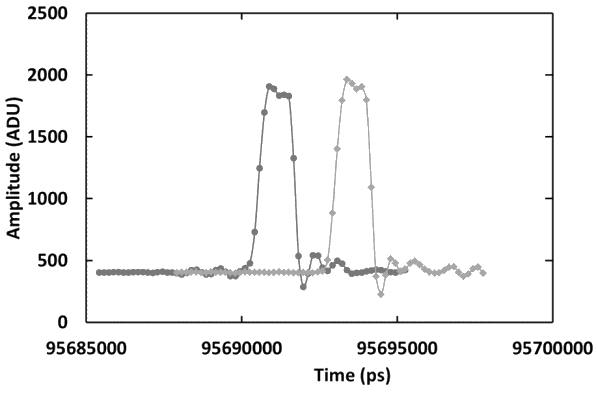
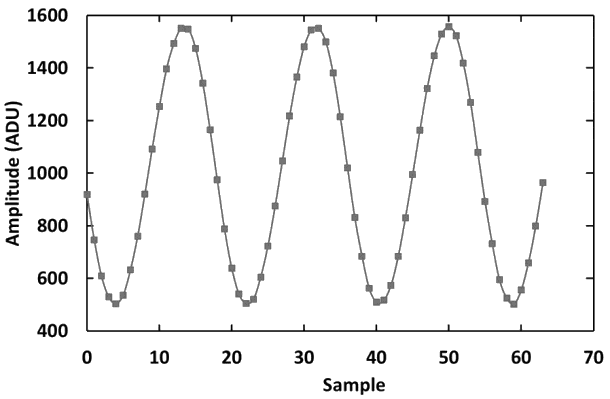


Figure 3: waveforms acquired and digitized by SAMPIC0 in self-trigger mode. Left: 800mV, 1GHz sinewave sampled at 10 GSPS (without any timing correction). Right: two 800mV-amplitude, 1 ns-wide pulses digitized by SAMPIC0 at 6.4 GSPS. The starting samples of the two waveforms are shifted because each channel is self-triggered by the pulse it detects (WTDC display mode).

The timing precision of the SAMPIC modules have been evaluated by measuring the time difference of pulses similar to those of Fig.3 (right) digitized by two channels. Results of such characterization as a function of the delay between the two pulses are shown on Fig. 4.

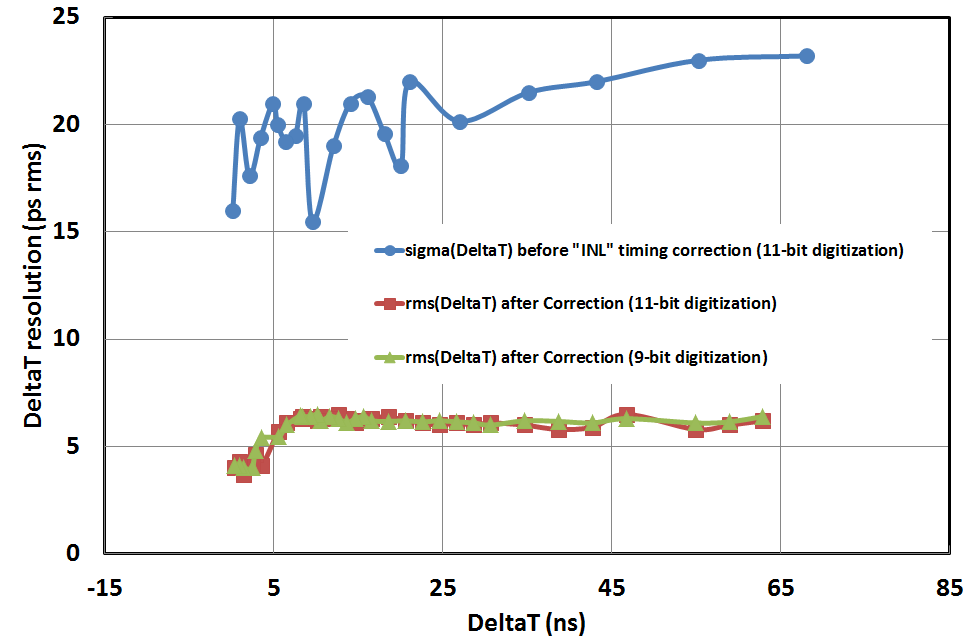
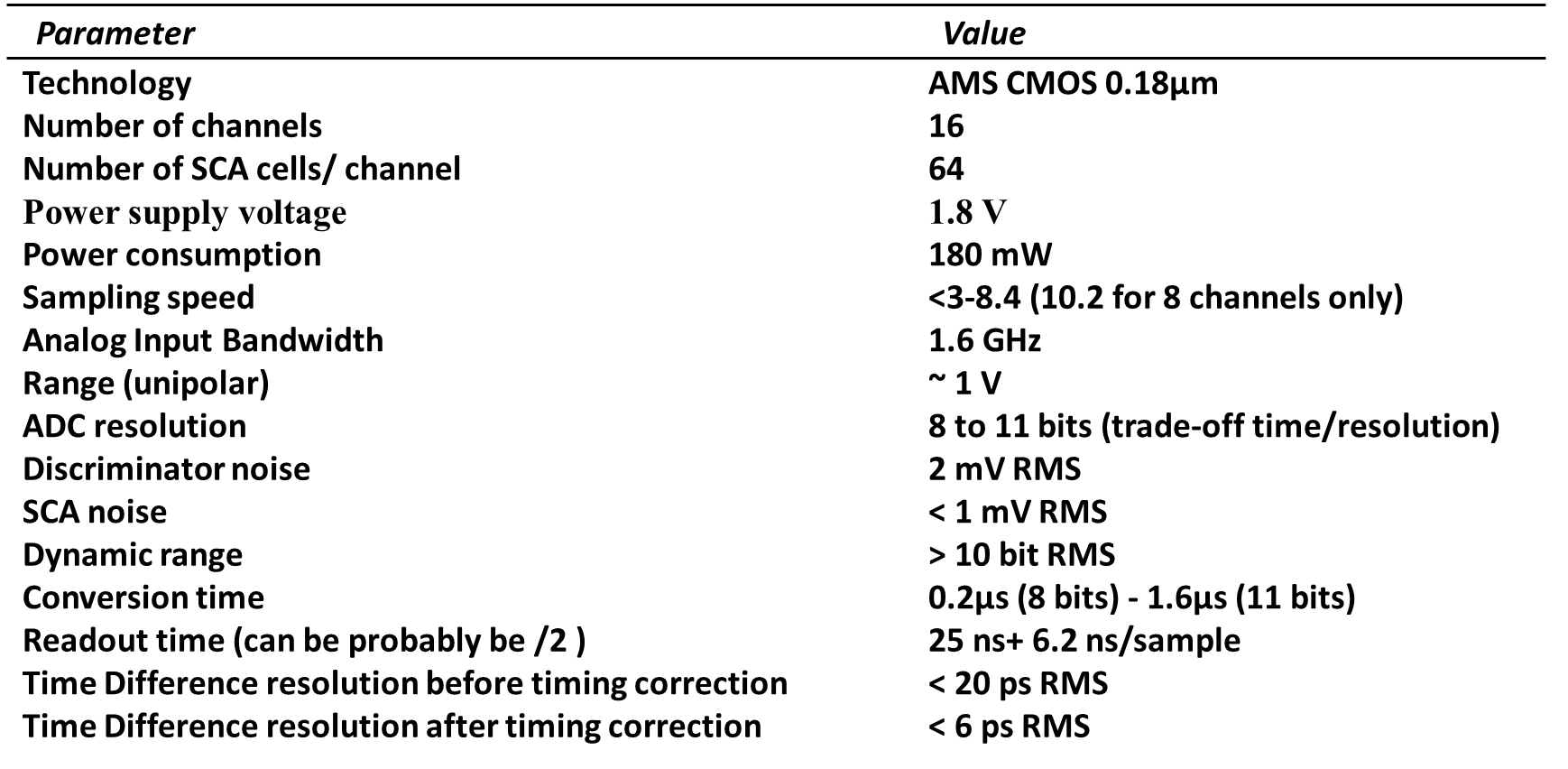


Figure 4: Variation of Timing difference resolution with the delay of two pulses similar to those of Figure 3 for timing-uncorrected and corrected data.

The measured timing resolution on the time difference is less than 25 ps RMS for uncorrected data and is reduced to less than 7 ps RMS for all the delays after a simple timing calibration. This resolution is kept unchanged from 10 ps to several µs delays so that we can claim that the timing resolution for an individual pulse is better than 5 ps RMS which was the goal of the design.

Table 1: Main parameters of the SAMPIC0 chip



Despite some minor bugs in its design, the SAMPIC0 chip fulfills our entire initial requirements and is as of today the only design offering a sub 5ps resolution with low deadtime. Its acquisition system is still constantly progressing and 5 SAMPIC modules have been produced, among which two are used at CERN respectively by the TOTEM and AFP collaborations for detector and beam tests.

3 Ongoing work (within the next year)

* Test with detectors,
* Improvement of the acquisition software, including the building of Windows/Linux generic C libraries,
* Development of the firmware and hardware to use the Ethernet and optical interfaces of the module,
* Design of the second version of the chip. The bugs will be fixed and the chip rate capability will be improved. It will also permit a more complex trigger configuration (like coincidence between channels),
* Design of a 64 or 128-channel board adapted for scalable acquisition setups.

4 Publications & presentations

Publications:

* « Le développement d’un système de mesure du temps de vol picoseconde dans l’expérience ATLAS », PhD Thesis defended by Hervé Grabas, Université de Paris XI, 3 dec 2013
* “SAMPIC: a 16-channel self-triggered waveform-based TDC chip with ps timing capabilities”, E. Delagnes et al., in press, Acta Physica Polonica (proceedings of the 2014 Clermont Timing Workshop).
* ”SamPic0: a 16-Channel, 10-GSPS WTDC Digitizer Chip for Picosecond Time Tagging”, D. Breton et al. , proceeding s of the IEEE-RT 2014 conference
* “Reaching a few picosecond timing precision with the 16-channel digitizer and timestamper SAMPIC ASIC”, E. Delagnes et al., submitted to NIM A.

Talk and Posters 2013-2014 :

* Several presentations in AFP and TOTEM meetings (Grabas, Saimpert, Delagnes, Royon)
* Talk at Topical Workshop on electronics for particle physics, Perugia (Italy) 23-27 sept 2013, H. Grabas
* Talk at Fast Timing Workshop, Erice (Italy), 20-22 Nov 2013., E. Delagnes
* Talk at Workshop on Picosecond Photon Sensors for Physics and Medical Applications, Clermont-Ferrand, March 12-14 2014, E. Delagnes
* Talk at IEEE-Real Time Conference, May 25-30, 2014, Nara (Japan), D. Breton.
* Talk at New Development in PhotoDetection (NDIP 2014), June 30th-July 4th 2014, Tours (France), E. Delagnes
* Talk at IEEE Nuclear Science Symposium , Nov 2014, Seattle (USA), E. Delagnes

5 Relevance of the project within P2IO and special added value for P2IO

This R&D project lies in the frame of a 20-year old collaboration between IRFU and LAL - 2 laboratories of P2IO - on the topic of analog memories for High Energy Physics. This development has permitted:

\* to keep the close link between the technical teams of the two laboratories,

\* to turn a patented idea into reality,

\* to keep the “Orsay/Saclay” team within the 3 world-leading teams in the topic of development of analog memories,

\* to develop an innovative timing system with unprecedented timing and rate performance, opening new horizons for physics experiments,

\* to make it available for the experiments of the P2IO community,

\* to develop a technology which may be used in other fields like medical imaging.

Moreover, one PhD thesis has been defended on this project supported by P2IO, 4 papers with explicit references to the role of P2IO have been published and 6 talks on SAMPIC have been presented in international conferences or workshops in which we have always underlined the key role of P2IO.

6 Possible valorization of the project

5.1 For physics experiments:

Even if SAMPIC is still at the prototype phase, there is a large interest of the community for this development. Tests are ongoing at CERN for the ATLAS AFP and TOTEM experiments. This chip is also considered for the “SHIP” experiment at CERN.

5.2 Industrialization:

Preliminary contacts have been taken with companies to industrialize the SAMPIC module. An European patent has been delivered and a US patent is still in its reviewing phase.

5.3 For other applications:

The timing performance of SAMPIC also catches the interest of designers of the future instruments for medical applications. We thus already have contacts in the field of proton-therapy and of time of flight based PET scanners (2 different contacts).

6 Expenses

The repartition that was decided initially was:

|  |  |  |
| --- | --- | --- |
|  | IRFU | LAL |
| Received in 2012 | 29050 € | 29050 € |
| Balance received in 2014 | 5850 € | 5850 € |

The preliminary breakdown of the actual expenses is :

|  |  |  |
| --- | --- | --- |
|  | IRFU | LAL |
| 2012-2013 : chip (1st proto) manufacturing | 9575 € |  |
| 2012-2013 : small equipments or subcontract< 4kE | 2952 € | 13000 € |
| 2012-2013 : travels | 1326 € | 1235 € |
| 2014, already spent: small equipment or subcontract <4kE | 2941 € | 4390 € |
| 2014, already spent: travels |  | 1460 € |
| 2014 (Q4): chip (2nd proto) manufacturing | 15000 € |  |
| 2014-2015: prevision of expenses for small equipments or subcontract <4kE | 3106 € | 14815 € |

The part of the budget not yet spent will be used for the 2nd prototype of the chip and its packaging, for the manufacturing of new test boards and for the manufacturing of the 64/128-channel board.

7 Future of the project (after P2IO)

* The SAMPIC chip has already acquired a worldwide notoriety, which might be premature as SAMPIC is still in the prototyping phase. It will for sure be proposed for many physics experiments. But the design team is today submitted to a rising pressure from the community aiming at using this system as soon as possible.
* A PHC H2020 project, based on a modified version of SAMPIC, has been submitted at the Oct 2014 EU call with the goal of developing a new generation of PET scan.