Appel d'offres R&D du LABEX P2IO

Upgrade du calorimètre électromagnétique de l'expérience ATLAS

Thème scientifique : Capteurs de nouvelle génération et leurs retombées.

Rapport intermédiaire

CEA/DSM/Irfu/SPP et CEA/DSM/Irfu/SEDI, Saclay

F. Deliot, H. Deschamps, F. Louis, B. Mansoulié, Ph. Schwemling

LAL, Orsay

D. Breton, D. Fournier, T. Guillemin, A.C. Schaffer, S. Simion

1 Project goals

The LTDB (LAr Trigger Digitizer Board) is an upgrade of the ATLAS calorimeter Level-1 trigger system, planned for Phase-1 running of the LHC (2018). It is designed to cope with the increased luminosity of the LHC. In order not to increase the trigger rate abow the present allocated bandwidth of 20 kHz for the calorimeter level 1 electromagnetic trigger while maintaining high efficiency for electromagnetic objects (electrons and photons), the upgraded trigger has to be more selective agains jets. This can be achieved by adding more discriminating variables in the trigger decision. The present system (see figure 1, top) is based on the summation of the energy deposited in $\Delta\eta \times \Delta\varphi = 0.1 \times 0.1$ trigger towers, with no information on longitudinal shower development retained. In addition, the 0.1×0.1 trigger tower are significantly coarser than the characteristic structures of the lateral shower development, and as a consequence they dont give information about the nature of the shower, electromagnetic or hadronic.

To overcome these limitations and give more information to build the trigger decision, the LTDB (figure 1, bottom) keeps the longitudinal information on the shower development, and the granularity of the sommation is significantly improved : in the first and second samplings of the calorimeter, that carry most information about shower development, it is 0.025 in the η direction instead of 0.1.

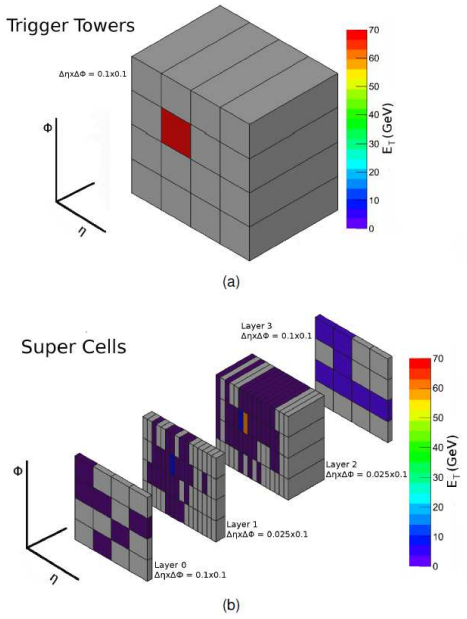

Figure 1: Granularity of the present calorimeter L1 trigger system (top) and of the upgraded calorimeter L1 trigger system , based on the LTDB (bottom)

In the new system, a trigger tower of 0.1×0.1 will be divided into 10 independant sums of elementary detector cells. These sums are called supercells in the following. In addition, in contrast with the present trigger system which is based on a purely analog board, the LTDB digitizes the signal coming from the supercells and sends the digitized results over high-speed (5Gb/s) digital optical links to the central trigger system, where the decision to keep or reject the data of each event is taken.

The ATLAS/Liquid Argon collaboration has decided to build a demonstrator of the LTDB, to be integrated on ATLAS by summer 2014. Two competing teams have started to design demonstrators based on different architectural choices. A US consortium started a design based on a digital motherboard and analog mezzanines. The driving argument for this architecture is the choice of a big FPGA, to implement digital functionalities. A french team around Saclay and Orsay started to design a board based on an analog motherboard and digital mezzanines. This architecture is more logical, because it gives the digital part the latitude to evolve from FPGAs to ASICS, and eases production and maintenance. The goal of our project is to build, test and integrate our demonstrator on ATLAS, to evaluate and validate our technical choices.

2 Description of work achieved

The general sharing of the work within our project is that the design of the analog functionalities has been done by the IRFU team, the design of the digital parts has been done by LAL team. The successful mating of the analog motherboard and of the digital mezzanines, followed by the integration of the board on the ATLAS detector, required obviously a lot of information exchange and common work for both teams.

The first step in our project has been to develop the building blocks for the analog section of the LTDB, i.e. the analog chain going from the Front-End crate baseplane to the LTDB ADCs, and creating also the summed signals needed for normal operation of the TBB, that are sent back to the backplane. The design we have developed for our demonstrator is based only on the radiation hard components used in the present front-end electronics. It features a minimal number of active components. This feature is desirable because it allows to use minimal space on the PCB, it keeps the dissipated power in the analog section to a minimum, minimizes the noise injected in the system and also minimizes the signal transit time.

After amplification and conversion from single ended to differential, and before being digitized, the signals are subjected to a mild shaping, in the form of a single pole of 15 ns, to slow down somewhat the signal, filter out

high frequency noise and avoid aliasing problems at the digitization stage. We have studied several possible realizations of the pole : passive RC, passive LR and active RC. We came to the conclusion that the best option in terms of noise and cross-talk is the active RC, which is what we have finally implemented.

The digital mezzanines, connected each to the mother board by two connectors, one for signal transmission, and the other for powering, are based on a COTS 12 bits low power ADC, a Cyclone V ALTERA FPGA to configure the ADCs, read them out and format the data. Standard ATLAS clock cleaners and PLLs for clock distribution and reception have been used. Optical communication with the LTDB readout system is done with standard CERN designed VTTX transceivers running at 5 Gbs/s. Two versions of the mezzanines have been designed and produced, and both have been successfully mated to the analog motherboard. The first version did not yet implement the optical readout and allowed data readout mainly through JTAG, the second had optical readout and all the needed data formatting features implemented. In total, the complete demonstrator of the LTDB needs nine digital mezzanines, plus one dedicated slow control mezzanine.

After having defined the schematics of the analog section of all channels, we have designed and produced a 64 channels test-board. This step allowed us to prove that we were able to fit all the components on the space available on the board. Preliminary evaluations had indicated that space would be very cramped, so it was of utmost importance to actually design, route and produce a section containing a significant number of channels to check the board could actually be built. This board has been mated to the first version of the digital mezzanine, which allowed to check the overall functionality on a few channels.

After that step, we have proceeded to the design of a complete LTDB demonstrator board. The added complexity with respect to the 64 channel prototype is that the complete board has to implement several ancillary subsystems that have to be carefully designed :

- A power distribution compatible with the ATLAS Front-End power bus, with only few voltage available and limited current that can be drawn from each individual line. We have made the choice to use only LHC standard regulator, widely used in ATLAS, and not to take the risk having not completely radiation qualified DCDC converters on our board. Here the difficulty is to ensure optimal use of the voltages and currents available on the power bus. This is particularly touchy given the high power consumption of the LTDB (about 200 W), due to the high quantity of digital components implemented on it. This power is much higher than the power used by the other front-end boards, that have only minimal digital functionalities implemented.

- A slow control system, to control and monitor the power distribution, program and configure the FPGAs, and also distribute the clocks on the board. The first option we considered was to implement the GBT system, developed by CERN to replace the present TTC (Trigger, Timing and Clock) system, used on the present boards. However, it was rapidly obvious that this system was not mature enough to be implemented on our board. We developed a slow control system based on the components used in the present Front-End system, namely the SPAC (Serial Protocol for Atlas Calorimeters) and the ASIC that implements this communication protocol.

- A LHC clock and Bunch Counter Reset system has been designed and implemented on a dedicated mezzanine. The fan out of these signals, that have to be distributed to all the digital mezzanines, is done through the mother board.

In parallel with the design of the demonstrator board, we have also built a mechanical demonstrator to test the insertion in an ATLAS Front-End crate. We did that to show that it was possible to actually build a board with a large cutout close to the front panel to accomodate the digital mezzanines, assemble it, insert it into and extract it from a Front-End crate, and still have good reliability of the electrical connexions. We also used this mechanical board to check successfully that the mechanical dimensions were all correct.

The cabled demonstrator mother board has been delivered at Saclay at the beginning of May. Its fine tuning, debugging and the integration of the digital mezzanines took until mid July. The board was then brought to CERN, where final debugging took place.

The board has been characterized at CERN using the same setup as the one used for the US demonstrator. The tests that were done include connectivity tests, linearity measurements, noise and cross-talk measurements. The measurements showed its performances were more than adequate for integration into ATLAS and for maintaining the triggering capability of the present system.

After one a half year spent on preparing the demonstrators, the situation is the following :

- The LTDB demonstrator based on the options we promote, i.e. an analog motherboard plus digital mezzanines, has been successfully built, tested at CERN and integrated on the ATLAS detector.

- All signals needed for normal operation of the present trigger system are correctly generated by the LTDB demonstrator. This was the main condition for the collaboration to accept the integration of the demonstrator on the detector.

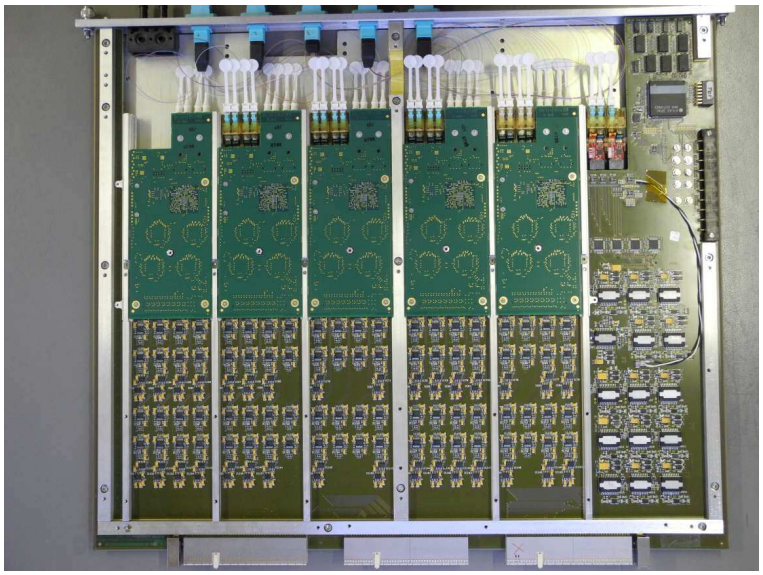

Figure 2: View of the board assembled

- Only six channels out of 280 are not functional, and the up to now measured performance of this demonstrator proves the soundness of our design.
- Discussion is ongoing with our US colleagues to converge on a common architecture for the final LTDB.

It should also be mentioned that the realization of the demonstrator needed more resources, manpower, money and time than anticipated. As a consequence, the design of the test benches we planned in our project is somewhat late and being actively worked on now.

3 Publications

The work we have done has been regularly presented at the ATLAS collaboration meetings. Once cosmics and collision data digitized by our LTDB demonstrator will be available, the resulting assessment of the performance of our board will also be presented in conferences. On a longer time scale, a publication on the LTDB demonstrators in the Journal of Instrumentation should be prepared.

4 Relevance of the project within P2IO

The development of the LTDB demonstrator has allowed us to progress towards the realization of the final LTDB board. The LTDB board is a key ingredient to make the best use for physics of the increased instantaneous luminosity of the LHC by 2018. The success of the LTDB realization will have drastic impact on the study of the Higgs properties in final states with electrons and photons. The accumulated luminosity (about 300 fb^{-1} for the whole Phase-I data taking period) will also allow for the first time a study of vector boson scattering, increase the reach in the search for exotic top quarks and new physics in general. LAL-Orsay teams and Irfu teams are present on these physics topics which are at the heart of P2IO's physics priorities. A strong involvement in the realization of the hardware upgrades needed to make the data analysis possible will give these P2IO teams on the long term a strong legitimity on these physics topics.

5 P2IO added value

It is clear that without P2IO, the realization of the demonstrator would have been much more difficult. On a very down to earth level, the P2IO funding has allowed us to be very reactive : we knew from the start that the planning for the realization of the demonstrator would be very tight, and it proved indeed to be the case. In this situation, the P2IO funding has allowed us to obtain very quick deliveries from our subcontracting companies. The existence of the P2IO funding at the level of the LTDB demonstrator project itself also allowed us to have only minimal administrative burden, which was invaluable at a time it was crucial for the project to concentrate on technical issues.

In addition, the existence P2IO funding has given during the realization of the demonstrator a good framework for collaboration between LAL-Orsay and Irfu/CEA. It has clearly motivated people to push the demonstrator as far as possible.

6 Possible valorization of the project

The realization of the LTDB demonstrator has given both teams the opportunity to design and build a complicated board, with a delicate interplay of many technical issues : thermal management, mechanics and integration, high speed optical data transmission, minimization of interactions between analog and digital signals.

This will give the teams the possibility to embark later on similar projects.