### PICSEL group @ IPHC Physics with Integrated Cmos Sensors and ELectron machines



## **PICSEL: Group history & composition**

#### Physicists

PICSEL

uelectronics

- Permanents
  - ➤ Marc WINTER (Project coordinator), since 1999 ⇒ (..., DELPHI, PICSEL)
  - > Jerome BAUDOT (Professor), since 2006 ⇒ (DELPHI, STAR, ALICE, PICSEL)
  - ➤ Isabelle RIPP-BAUDOT (researcher), since 2010 ⇒ (DELPHI, CMS, D0, SuperB, PICSEL)
  - ➤ Auguste BESSON (Assistant Professor), since 2003 ⇒ (D0, CMS, PICSEL)

#### Post-doc

- ➤ Serhiy SENYUKOV (leaving dec.2013) ⇒ (ALICE, PICSEL)
- ➤ Luis Alejandro PEREZ PEREZ (Sep.2013 Sep.2016) ⇒ (Babar, CKMfitter, SuperB, PICSEL)
- PHD students
  - Loic COUSIN (Sep 2011-Sep 2014) ⇒ (AIDA and alignment studies + double layers @ILD studies)
  - ➢ Robert MARIA (Sep 2012- Sep 2015) ⇒ (Time dependent asymmetry in D0 decays and plume + tracking in Belle 2)
- Microcircuit designers and support
  - 12 permanents (See Claude Colledani's presentation)
  - Test Experts
    - 6 permanents

## CPS and vertex detector optimisation: squaring the circle



#### Early 2000s

- Different approach compared to hybrid pixels & LHC
- Focus on resolution and material budget
- Vertex detector design and specifications
  - Physics performances
    - Spatial resolution
    - ➤ Material budget ⇔⇒multiple scattering
  - **Experimental environment constraints** 
    - Radiation hardness (ionising and non ion. rad.)
    - ➢ Occupancy ⇐⇒Read-out speed
    - ▶ Power dissipation  $\Leftrightarrow \Rightarrow$  cooling ?
  - Other parameters
    - Costs, fabrication reliability and flexibility
    - Mechanical integration
    - > Geometry
    - > Alignment issues
- Interdependance of these parameters
  - e.g. lower radius of inner layer
    - > Better  $\sigma_{i.p.}$  but larger occupancy, higher rad.
    - $\blacktriangleright$  Needs higher read-out speed and/or granularity  $\Rightarrow$  power dissipation

#### ⇒ CPS presents an attractive trade off with respect to all these parameters



## CMOS pixel sensor (CPS) for charged particle detection





- Main features
  - Monolithic, p-type Si
    - $\blacktriangleright$  Signal created in low doped thin epitaxial layer ~10-20  $\mu$ m
    - > ~ 80 e- /µm ⇒ total signal ~ O(1000 e-)
  - Thermal diffusion of e-
    - Limited depleted region
    - Interface highly P-doped region: reflection on boundaries
  - Charge collection: N-Well diodes
    - ➤ Charge sharing ⇒ resolution
  - Continuous charge collection
    - No dead time
- Main Avantages
  - Granularity
    - > Pixel pitch down to 10 x 10  $\mu$ m<sup>2</sup>  $\Rightarrow$  spatial resolution down to ~ 1  $\mu$ m)
  - Material budget
    - > Sensing part ~ 10-20  $\mu$ m  $\Rightarrow$  whole sensor routinely thinned down to 50  $\mu$ m
  - Signal processing integrated in the sensor
    - Compacity, flexibility, data flux
  - Flexible running conditions
    - > From  $\leq 0^{\circ}$ C up to 30-40°C if necessary
    - ➤ Low power dissipation (~ 150-250 mW/cm<sup>2</sup>) ⇒ material budget
    - ▶ Radiation tolerance: >~100s kRad and O(10<sup>12</sup>  $n_{eq}$ ) ⇒f(T,pitch)
  - Industrial mass production
    - > Advantages on costs, yields, fast evolution of the technology, Possible frequent submissions
- Main limitation
  - Industry adresses applications far from HEP experiments concerns
    - > Different optimisations on the parameters on the technologies
  - Recently: new accessible processes:
    - Smaller feature size, adapted epitaxial layer
    - > Open the door for new applications

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### CMOS: Past, present and future: 15 years of R & D



## State of the art



- IPHC-Strasbourg and collab.
  - CPS developped since ~ 1999
    - ➢ 4-5 fabricated prototypes /year
    - 2-3 test beam campaigns /year
    - ~ 50 conferences
    - ~ 60 publications
    - ≻ ~ 15 PhD
  - Typical performances in AMS 0.35 μm technology
    - > Detection efficiency  $\ge$  99.9% with fake rate  $\sim \le 10^{-5}$
    - > Typical spatial resolution (20  $\mu$ m pitch) :
      - ~1.5 µm (analog output)
      - ~3.5 µm (digital output)
- Read-out architecture with digital output
  - In pixel preamplification and CDS
  - Column parallel rolling shutter read-out
    - Continuous read-out
    - Integration time = #rows x row r.o. time (100ns)
    - End-of-columns discriminators
    - > Data sparsification (0-suppression)

⇒enhances r.o. speed with preserving material budget, granularity and power comsumption





## State of the art (2): current applications

Institute Particles Classe Honore Classe Transcom

- EUDET pixel telescope
  - Beam telescope (FP6 project)
    - ➢ 6 x Mimosa-26 planes (// r.o. and dig output)
    - Successfully operating since 2008
- STAR PXL detector
  - First vertex detector equipped with CPS
    - 2 layers = 40 ladders x 10 sensors
    - ➢ First sectors (3/10) installed May 2013
    - Commissioning completed
    - End of construction under way
- Prototype: Mimosa-28 (Ultimate)
  - AMS 0.35 µm techno with high resisitivity epitaxial layer
  - > 960 x 928 pixels, 20.7 µm pitch ⇒ 3.8 cm<sup>2</sup>
  - In pixel CDS & ampli, collumn parallel read-out
  - End of column discri. and binary charge encoding
  - On chip zero suppression

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## Upgrade for more demanding applications



- CPS are also considered by forthcoming projects
  - ALICE @ LHC: baseline for ITS upgrade
  - CBM @ FAIR (>2018): baseline
  - ILD @ ILC@ 500 GeV: TDR option

	$\sigma_{single \ point}$	read-out time	TID	Fluence $n_{eq}/cm^2$	T <sub>coolant</sub> °C
STAR-PXL	5 µm	~200 µs	150 kRad	3×1012	30
future projects	3-5 µm	I-30 µs	up to 10 MRad	up to 1014	< 0 - 30

### ⇒ higher particles rates

- Goal: ALICE ITS upgrade (cf. TDR draft) ⇒scheduled for 2017-18 LHC shutdown
  - Addionnal L0(22mm) + replacement of inner layers
  - scheduled for 2017-18 LHC long shutdown
    - > 0.25-1 MRad + 0.3-1x10<sup>13</sup>n<sub>eq</sub>/cm<sup>2</sup>
    - Chip sensitive area 1x3 cm<sup>2</sup>

- ➤ Inner layers ⇒0.3% X0
- > Spatial resolution ~ 4  $\mu$ m
- $\blacktriangleright$  Read-out speed ~ 10-30  $\mu$ s



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MISTRAL > Col. // read-out with in pixel ampli.

Read-out speed ~ 30 μs

> In pixel discri & 2/4-row encoding

(cf. C. Colledani's talk)

Auguste Besson

ASTRAL

## Spin off

- Visible photon detection
  - design of a specific electron bombarded CMOS (LUCY)
    - ➢ collab. with IPN-Lyon and PHOTONIS
    - goal = hybrid photo-detector with
      - \* sensitivity to single photons
      - \* spatial resolution in the 10 microns range
    - paper: NIM A 648 (2011)266–274, doi:10.1016/j.nima.2011.04.018
- X-rays
  - concept studies, no practical applications
    - > Explore high res. Process, single photon counting, 1 PhD.
- Radiation monitor
  - Dosimeter for space application
    - Ongoing thesis and prototype
- Beta detection
  - > Nucl.Phys. B (Poc.Suppl.) 125 (2003) 133
- Hadrontherapy
  - proton telescope based on thinned MIMOSA 26 or M28
    - > FIRST experiment at GSI: Carbon cross-sections measurement
    - > Online dose monitoring for carbon-therapy with Proton Interaction Vertex Imaging
    - http://hal.archives-ouvertes.fr/hal-00838442



#### •Tools

## -Software for test beam analysis (TAF/MAF)

Track matching, efficiency, resolution, clustering, etc.

-Digitisation tool

>(DIGMAPS) standalone tool to build a digitizer
-GFANT 4 full simulation

➢AIDA & self alignement (L.Cousin)

### •e<sup>+</sup>e<sup>-</sup> Physics and tracking

-ttbar-H Yukawa coupling @ ILC

-Tracking ILD-VTX @ ILC

➤Tracking studies @ ILD

Standalone tracking with VTX

-See I.Ripp Baudot's talk





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  - ≻(Y.Voutsinas + B.Boitrelle )
  - ➤Tracking studies @ ILD
  - ≻Standalone tracking with VTX

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Energy deposition, charge transport, charge collection discriminator simulation

Efficiency Resolution Multiplicity



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## Integration activities

### • PLUME

- Double sided ladders -
  - Collab. Bristol & DESY
  - Double sided ladders with ~ 0.35% X0
  - ➢ First prototype built in 2011
  - See J.Baudot's talk.

• SALAT in AIDA project

- Large surface detectors (stitching)
  - First demonstrator built
  - ➢ Goal: 6 x 4 cm<sup>2</sup>
  - > Applications: Large area telescope, forward discs
- SERNWIET
  - Sensor embedding in kapton
    - Collab. CERN



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Auguste Besson

Image obtained with 55Fe source, X-rays detected by MIMOSA-26

## Summary

- Group founded with the starting CPS R&D in early 2000s
- Motivations
  - Lepton collider physics
  - Exploit fully the potential of CPS
    - Pursuing the R&D and prototypes fabrications
    - Integration developpements (PLUME, etc.)
    - > Algorithms & tracking optimizations
- Know how
  - Physics & tracking
    - ➢ Resolution, clustering, digitisation, alignment, etc.
    - > Interests: e.g. low momentum tracks, VTX standalone tracking, c-tagging, etc.
  - Hardware Expertise
    - > Microelectronics, Mechanical integration, Microtechnics (probe tests, bounding), PCB designs
  - Test experts
    - DAQ systems, Lab tests, Beam test = 2 telescopes + 2-3 campaigns/year (@ DESY & CERN)
- ⇒ Mastering the complete fabrication chain (from design to validation) on site.
- ⇒ Faster fabrication/validation cycles (typically < 1 year)

## Back up

## **Read-out speed**

- ILC motivations
  - − Robustness with respect to predicted beam background ⇒occupancy
  - Capabilities to stand the increased occupancy @ 1 TeV (x3-5)
  - Stand alone tracking capabilities (low momentum tracks)
- How to improve read-out speed ?
  - Elongated pixels (+staggered pixels)
    - Less row per column
    - ➤ Allow in pixel discriminator  $\Rightarrow$  r.o ≥ 2 x faster
  - More parallelisation
  - > 2 or 4 rows read out simutaneously  $\Rightarrow$  r.o ≥ 2-4 x faster
  - Sub arrays read out in //  $\Rightarrow$  r.o  $\ge$  2-4 x faster
  - > Only possible in smaller feature size process (0.18  $\mu$ m) see next slide



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## Validation of the 0.18µm technology roadmap

- Goal: ALICE ITS upgrade (cf. TDR draft) ⇒scheduled for 2017-18 LHC shutdown
  - Addionnal L0(22mm) + replacement of inner layers
  - scheduled for 2017-18 LHC long shutdown
    - (See talks by Beolè and Bufalino)
       0.25-1 MRad + 0.3-1x10<sup>13</sup>n<sub>eq</sub>/cm<sup>2</sup>
- ➤ Inner layers ⇒0.3% X0
- > Spatial resolution ~ 4  $\mu$ m
- Chip sensitive area 1x3 cm<sup>2</sup>
- $\blacktriangleright$  Read-out speed ~ 10-30 µs



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• STEP 1 (2012): First prototypes ⇒Validation of MIP detection performances



## Mimosa-28 (=Ultimate) performances



- Operating conditions
  - JTAG + 160 MHz
  - Temperature
    - ≻ 35°C
  - Read-out time =  $200 \ \mu s$ 
    - > Suited to  $\geq 10^6$  part/cm<sup>2</sup>/s
  - Power comsumption
    - ➤ 150 mW/cm<sup>2</sup>
- Performances
  - Noise ~ 15 e- ENC @ 35°C
  - Eff vs fake rate
  - Spatial resolution
    - charge sharing
    - ➤ σ<sub>sp</sub> ≥~ 3.5 μm
  - Radiation tolerance
    - 3.10<sup>12</sup>n<sub>eq</sub>/cm<sup>2</sup> + 150 kRad @ 35 °C

#### Mimosa 28 - epi 20 um - NC S400 Efficiency 10<sup>-1</sup> 98 10-2 10<sup>-3</sup> 96 10-4 94 10-5 10<sup>-6</sup> 92 10-7 90 **10<sup>-8</sup>** 88 10<sup>-9</sup> Not irradiated 150 kRad 10<sup>-10</sup> 86 10-11 10 11 12 9 8 Threshold (mV)

### ⇒ reached performances meets specifications

### An example of vertex detector optimisation: ILD @ ILC





- Spatial resolution/material budget  $\Rightarrow \sigma_b < 5 \oplus 10/p\beta \sin^{3/2} \theta \ \mu m$ .
- Occupancy 1<sup>st</sup> layer: ~ 5 part/cm<sup>2</sup>/BX ⇒ few % occupancy max
- Radiations: O(100 krad) et O(1x10<sup>11</sup>  $n_{eq (1MeV)}$ ) / year
- Power dissipation: 600W/12W (Power cycling, ~3% duty cycle)
- Proposed geometry:
  - 3 x double sidded ladders
    - Optimize material budget / alignment.
- 2 designs:
  - Double sidded inner ladders :
  - Priority to r.o. speed & spatial resolution
  - 2 faces: resolution / speed (elongated pixels)
  - > Pitch  $16x16\mu m^2/16x64\mu m^2$  + binary charge encoding
  - t<sub>read-out</sub> ~ 50μs/10μs ; σ<sub>res</sub> ~ 3 μm/6μm
     2012: Mimosa-30 prototype (AMS 0.35 μm)
  - 2012: Mimosa-30 prototype (AMS 0.35 μm) with 2 sided read-out
  - Outer ladders: power dissipation
  - Minimize P<sub>diss</sub> while keeping good spatial resoution
  - > Pitch ~  $35x35 \ \mu m^2$  + ADC 3-4 bits
  - t<sub>read-out</sub> ~ 100 μs
  - 2012: Mimosa-31 prototype (AMS 0.35 μm) with 4-bit ADC

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## Ongoing evelopments

#### Applications driving the R&D

- ALICE Internal Tracking System: 50  $\mu$ s with 4  $\mu$ m and 10<sup>7</sup> hits/cm<sup>2</sup>/s
  - Require readout acceleration
- AIDA Single Arm Large Area Telescope: Sensor sensitive area = 25 cm<sup>2</sup>
  - Require stitching
- CBM Micro-Vertex Detector
  - Require acceleration & radiation tolerance

#### Advanced functionalities

- MIMOSA-32/34: further optimisation of q-collection, noise, ampli.
- MIMOSA-22-THR: pixel matrix + col-level discriminators
  - single and double rows read-out
- SUZE-02: zero-suppression circuitry
- AROM-0: matrix with in-pixel discriminator
- MIMADC: matrix with in-pixel 3-bits ADC

#### Full Scale Basic Blocs (FSBB)

- = complete functionality over ~1 cm<sup>2</sup>
- Q4/2013: col-level discri. approach (→MISTRAL)
- Q4/2015: in-pixel discri. approach (→ASTRAL)

#### Final sensors

- Q4/2014: MISTRAL 22x33 µm2 pitch with 30 µs integration time (15 µs possible)
- Q4/2016: ASTRAL 15 µs integration time (2 µs possible)
- 2015: AIDA large area (4×6 cm2) beam telescope sensor.

#### Auguste Besson



- Change from to Tower-Jazz
   0.18 µm CIS 2D process
- First validation in 2011-2012: see Auguste Besson's talk





0-suppression stage



## Evolving to an optimal process: Tower-Jazz 0.18 $\mu m$



- CMOS  $0.35\mu m$  process does not allow to fully exploit the potential of CPS
- Main limitations of 0.35µm:
  - Feature size ⇒ in pixel circuitry, r.o. speed, power comsumption, radiation hardness
  - Number of metal layers ⇒ in pixel circuitry, r.o. speed, insensitive area
  - Clock frequency ⇒ data output
  - Epitaxial layer flexibility: (thickness and resistivity) ⇒Charge collection/sharing
- Tower-Jazz 0.18 μm
  - Smaller feature size process
  - Stitching  $\Rightarrow$  multi chips slabs (yield ?)
  - 6 metal layers ⇒in pixel discri.
  - Deep P-well  $\Rightarrow$  small pitch in pixel discri.
  - higher epitaxial resistivity (1-6 k $\Omega$ .cm), epi thickness 18-40  $\mu$ m
    - Enhances signal
  - ⇒ Higher read-out speed, higher radiation tolerance
  - ⇒ Faster and smarter pixels



## The PLUME project

### Collaboration with

- DESY + University of Bristol
- Formerly with University of Oxford

### ▶ Previous achievements ≤ 2012

- Ladders with material budget 0.6 % X<sub>0</sub>
  - Full VTX inner layer geometry
- Operated with air cooling on beam test
- Operation with power pulsing in preparation (single sensor achieved)—

### Moving toward final goal

- Expected material budget 0.35 % X<sub>0</sub>
  - Lighter (alu) flex cable & mechanical support
  - Two flex designs for symmetry and final ladder geometry
- Readiness
  - First cables validated, rest to be produced
  - New assembly setup in production
  - First ladder by end of summer 2013





# Rationale for double-sided ladders

- Mechanics
  - One support for 2 sensitive layers = benefit material budget hence resolution
- Safety
  - ▶ Hit redundancy ➡ benefit efficiency
- Technology
  - Mixing 2 different sensor optimizations = alleviate technology limitation

### Alignment

- Additional geometric constraints benefit #tracks needed for a given precision
- Tracking
  - 2-hits make a mini-vector => additional angular information
    - ➡ improve hit-track association

## Tracking @ ILD



#### Silicon standalone tracking

- The problem at low  $p_{T}$  is track-seeding ►
  - 3 real 3D hits needed **b** -
- With current strip-SIT configuration ►
  - Either not efficient enough ×. 80% at p<sub>T</sub> 500 GeV/c
  - Either two slow (270 s /event) when considering all combinations
- Pixelated-SIT with 2 double-layers option
  - Offers 4 3D hits & mini-vectors
  - Cellular automaton algorithm under evaluation Þ.

Track extrapolation TPC→SIT→VTX

Impact of pixelated-SIT (double-layers)

	strip		pixel	
	σ <sub>s.p.</sub> (μm)	t <sub>int</sub> (μs)	σ <sub>в.р.</sub> (μm)	t <sub>int</sub> (µs)
SIT - 1	7( <i>R</i> -φ)	< t <sub>BunchX</sub>	4/15	100/7
SIT - 2	50 (z)		4	100

- Efficiency TPC→SIT strips > pixels
  - Benefit of short t<sub>int</sub> / beam Background
- Efficiency SIT > VTX similar / both options ١.
  - BUT pixel timestamping layer mandatory Þ

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# Beam test results on Ladder

#### Beam test with 120 GeV π in November 2011

- → efficiency > 99% for fake hit rate<10<sup>-4</sup>/pixel
- → σ(point)=3 μm
- → σ(angle)=0.1°
- Analysis ongoing / alignment & cracks





- With next 0.35% X0 prototype
- Power pulsing in magnetic field

Þ



air outlet, cable out



#### Idea from R. De Oliveira, W.Dulinski

- Embed sensor one at time
  - ➔ Alleviate alignment difficulty
  - ➔ Allow individual testing before assembly (yield)
- Processing of further metal layers decoupled from sensor embedding

### Questions

- x Insensitive area in-between sensors?
  - ➔ Possibility to overlay embedded sensors



