

Study of HV CMOS Sensor for the upgraded ATLAS tracker in the High Luminosity LHC

Jian LIU 16/Dec/2013

Outline

- ATLAS inner detector upgrade
- Inner tracker upgraded options and HV-CMOS Concept
- HV CMOS TCAD simulation
- HV CMOS prototype test results
- Conclusion and next steps

LHC Upgrade Potential Schedule



ATLAS Pixel Detector Perspective

ATLAS has decided to replace the entire Inner Detector with a new, all-silicon Inner Tracker (ITk). The ITk must satisfy the following criteria(w.r.t. ID):

•higher granularity,

•improved material budget

•increased radiation hardness of all components

At the moment, the ITk project is in R&D phase.



HL-LHC Environment

• The HL-LHC will operate at a nominal instantaneous luminosity of $5 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1}$ Silicon 1 MeV-equivalent flux

Fluence at 5 cm radius: $\sim 2 \cdot 10^{16}$ neq cm⁻² ~ 1500 MRad

The new Inner Tracker should be rad-hard and cope with high occupancy.

- Presently, one possibility for upgrade is to use a hybrid pixel detector concept:
- •Sensor: thin silicon planar or 3D (reduce drift distance), diamond...
- •Readout-Out Chip: deep-submicron rad-hard ICs (130nm,65nm)=>high granularity=> high resolution, low occupancy



Main drawbacks:

- •Expensive hybridisation,
- •Non-standard sensor processes
- •Yield issue
- •Material budget
- •Very HV after irradiation

Rad-hard & Low Price?

- Ways to reduce price:
 - •Commercial processes
 - •Large wafer size
 - •Cheaper interconnection technologies

Explore industry standard CMOS processes as sensors:

•Basic requirement is Deep N Well(DNW)=>allow high substrate bias voltage=>drift=>rad-hard

•Existing in many processes, especially in HV CMOS technologies, such as AMS 0.18um HV CMOS, GF 0.13um BCDlite and LF 150nm technology...





Main advantages:

•Commercial CMOS technology \rightarrow lower price per unit area.

•Can be thinned to tens of $um \rightarrow material$ budget reduced.

- •Pixel size can be reduced.
- •Biasing voltage can be no higher than 60V.
- Ist amplifier in-sensor → capacitive coupling to a specific digital part by gluing (compatible with ATLAS FE-I4).

Questions:

→Radiation hardness (sensor / transistors).
→Signal to Noise Ratio / Efficiency.

HV CMOS Sensor Concept

- Implemented in commercial HV CMOS technology
- "In sensor" electronics
- NMOS and PMOS surrounded by Deep N well(DNW)
- Substrate can be biased to high voltage, typical reverse bias voltage is 60V and the depleted region depth ~10um.



TCAD Simulation

- In order to verify the feasibility of specific HV CMOS technologies, we need to understand the DNW electrical behavior carefully → 3D TCAD (Technology Computer Aided Design) simulations were and are being performed using Silvaco.
- At first, a low voltage DNW based on Chartered 0.13um technology was simulated.
- Presently, a 3-pixel array based on AMS 0.18um technology design rule is being simulated.

LV DNW Simulation

5) Chartered







We measured a breakdown voltage of 33V for the LV DNW.

Low Voltage devices into Low Voltage Deep Nwell.

Based on Chartered 130nm design rules, performed 3D DNW simulation using Silvaco.

Breakdown voltage ~19V=>get 5µm depleted depth=>MIPS : 400e-



Jian LIU/CPPM

HV2FEI4_AMS_p2 Simulation

Using Silvaco Devedit3D to build 3D device structure.



Simulation Top View

3 pixels (A, B and C) + 4 peripheries (D, E, F and G) + 1
 p+ scribe line (H, surrounds the chip)



Jian LIU/CPPM

Preliminary Results

Depletion region @Vsub=-60V

Depletion depth is 8.42um @Vsub=-60V

Leakage current is $\sim 8x10^{-13}$ A/per pixel, which agrees with test results ($\sim 7x10^{-13}$ A). Radiation effect simulation is ongoing.

TCAD Simulation Conclusion

- In simulation, 5um depletion can be obtained at 20V bias voltage using low voltage DNW, which corresponds to 400e-/MIP.
- Obtained correct leakage current and depletion behavior for HV2FEI4_AMS_p2 Silvaco simulation.

HV-CMOS Proof of Concept Prototypes: HV2FEI4_AMS

- Up to now, several prototypes have been designed and tested.
- The first prototype we received is HV2FEI4_AMS_p1 (Ivan Peric, Heidelberg University) fabricated in AMS 0.18 technology and have been tested since August/2012.

The pixel contains a charge sensitive amplifier, a comparator and a tune DAC.
The transistor layout was not made rad-had (proof of concept only!).

And a second	
	-
	î
	*
	1.0
	1

HV2FEI4_AMS Test Results

- Two damage mechanisms: nonionizing and ionizing effects are investigated.
- 3 HV2FEI4_AMS p1 chips were tested at CERN PS(24GeV proton beam)
 - 1 chip at ambient temperature
 - The first irradiation test for CCPD
 - After 195 Mrad still see protons on Amplifier, not on Discriminator
 - After 435 Mrad and 3 weeks annealing and tuning chip parameters (Vcasc=380mV) still see injection signals both on Amplifier and Discriminator
 - 2 chips at -8° C
 - Amplifier and discriminator were killed up to 440Krad and 550Krad respectively t=-8deg
 - After 2-24 hours 28deg C annealing, amplifier partially recover, but discriminator was still no signal.
 - CCPD8 amplifier works up to 80Mrad.
 - CCPD9 amplifier works up to 70Mrad.

HV2FEI4_AMS Test Results

The first three chips proton test results reveal obvious ionizing damage effect.

- But neutron irradiation to 10¹⁶ neq/cm2 (chips off during irradiation, only nonionizing damage) => No evidence of signal decrease.
- After that, HV2FEI4_AMS p2 with rad-hard pixels (ELT transistor implemented) was designed and tested using x ray source=> detectors can work up to 862MRad with amplitude decrease.

Rad-hard pixels 1volt injection

HV2FEI4_AMS Test Conclusion

- HV2FEI4_AMS p1 was not radiation hard.
- Specific modification has been made to transistors in order to enhance radiation hardness in p2. Sensors still work with reduced amplitude after 10¹⁶neq/cm² and 860 Mrad.
- ► Ionizing effect should be the main reason for efficiency reducing instead of NIEL (Non ionizing energy loss) → fixed in p2!!!

HV-CMOS Proof of Concept Prototypes: HV2FEI4_GF

- Why GlobalFoundries
 - GlobalFoundries is the world's second largest independent foundry
 - It is a member of the Common Platform (IBM, Samsung, GF). The joint development began at 90nm and below (65nm, 45nm, 32nm, 20nm)
 - GlobalFoundries merged with Chartered Semiconductor in 2010. The 0.13µm LP Chartered technology was chosen by Tezzaron to develop the 3D-IC solutions.
 - The 0.13µm LP Chartered technology was extensively qualified to be a good candidate for the ATLAS B-layer replacement., both for the 3D (FETC4 chip) and the 2D developments(FEC4 chips) (rad-hard up to 600Mrads, SEUless..)
 - 130nm BCDlite technology is used for 3D process.
 - High resistivity wafers might be supported.

HV-CMOS Proof of Concept Prototypes: HV2FEI4_GF

33µm x 125 µm Pixel size

Top Pads : Test structures

- Linear and ELT transistors (short and narrow channels).
- Pixel behavior

• HV2FEI4 Pinout compatible.

Additional HV2FEI4 test

lian LIU/CPPM

- The HV2FEI4 GF version is a 26 columns and 14 rows matrix pixels, 100% HV2FEI4 AMS version pixel compatible (same size, same physical layout).
- The HV2FEI4 GF version will be glued to the FEI4

From Patrick Pangaud , HV2FEI4_GF: a 0.13µm Global Foundries version, ATLAS Upgrade Week, May, 2013.

Recent Results: HV2FEI4_GF X Ray Test

20

In order to investigate ionizing effect on the sensor surface and verify the chip's radiation hardness, we performed X ray irradiation test from OMRad to 1GRad.

Xray source is 103.5Krads/mn: ~16 hours=>100MRad

Two special pixels and test transistors were investigated up to 1GRad

PIXEL_ALONE : identical pixel architecture, but only the preamplifier part was implemented.

PIXEL_DNW : use two parts : The DNW part only to capture charge into DeepNwell and the preamp part tied to VDDA, used only to amplify the charge from the DeepNwell.

Recent Results: HV2FEI4_GF X Ray Test

After 1GRad irradiation, Alone pixel's amplifier is still alive. DNW pixel is dead after 600MRads

After 2MRads, DAC output appears erratic \rightarrow looks like some configuration transistors do not work correctly. Weak buffers!!!

Amplifier output vs. Dose

Alone pixel can detect Fe55 source at 400MRad

Jian LIU/CPPM

Recent Results: HV2FEI4_GF X Ray Test

HV2FEI4_GF X Ray Test Conclusion

- After 1GRad X ray irradiation, Alone pixel is still alive but DNW pixel dead at 600MRad (might not really be dead, probably configuration error).
- Configure the chip has some erratic errors after 2Mrad. Weak buffer, shift register...
- ELT nmos transistor show good radiation tolerance. Positive sign to use this technology in a high radiation environment.

Conclusion and Next Steps

- HV2FEI4_AMS_p1 prototype was tested to radiation levels up to 400 MRad. Sensor tolerance seemed positive, but the electronics itself suffered from radiation.
- The second AMS version prototype using specific rad-hard layout technologies was alive after 862MRads irradiation. Both sensor and electronics radiation damage effects need to be studied carefully.
- First GF prototype also indicate positive radiation hardness. HV2FEI4_GF gluing on FEI4 has finished. Some specific tests will be performed.
- Porting to LF 150nm technology is ongoing.

My current works:

- TCAD simulations show good agreement with our test. Now optimize the 3D meshing, investigate ionizing radiation effects to understand X ray irradiation damage behavior. Then I will perform precise sensor irradiation simulation.
- Investigate different high voltage sensor implementations, try to find a way to reduce leakage current.
- ▶ Irradiation studies GF (CERN) + data analyzes (CPPM).

Thanks for your attention !

Jian LIU/CPPM