ATLAS Upgrade
focus on calorimeter and tracker plans.

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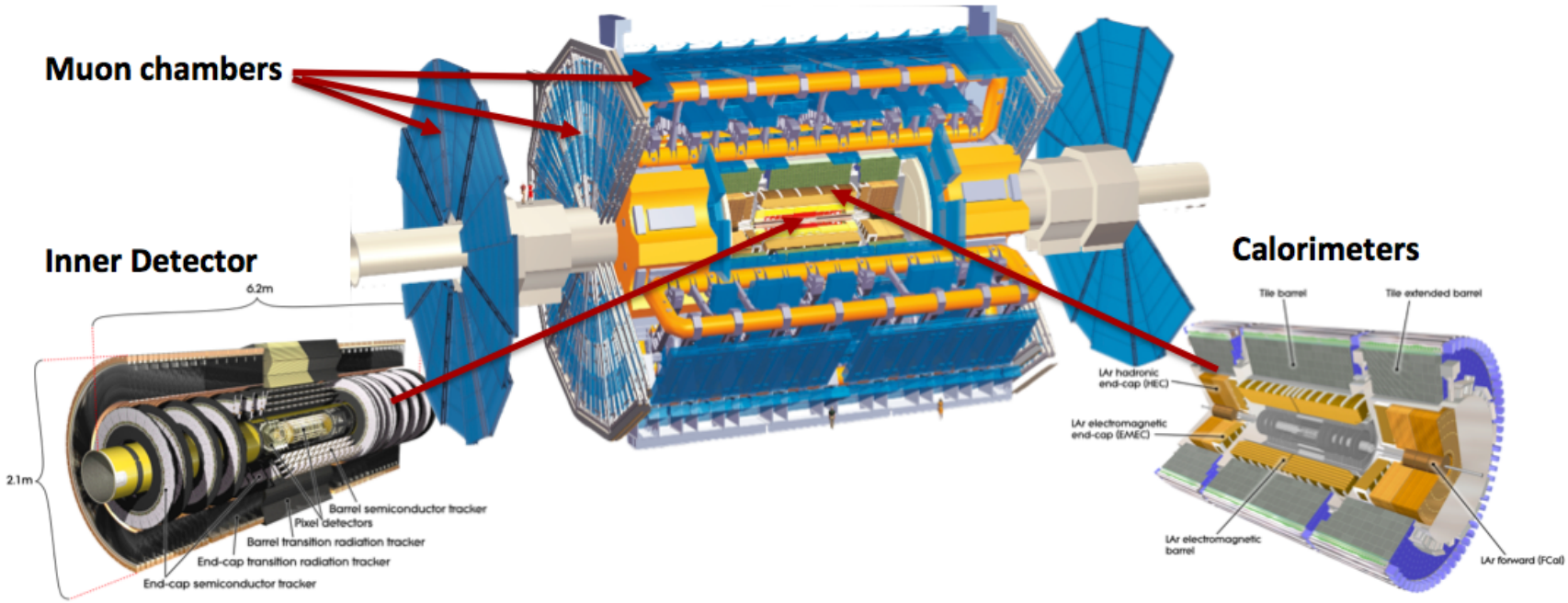
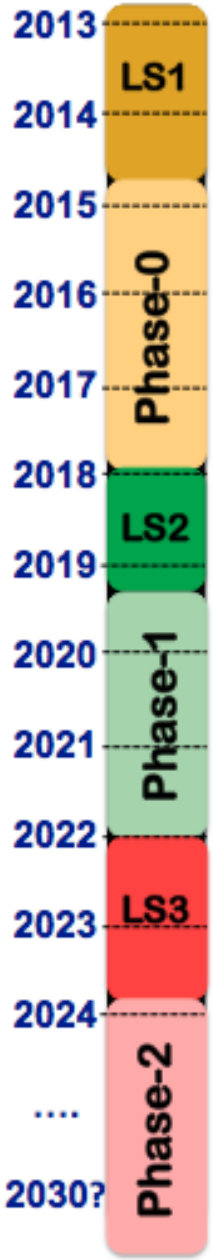
Outline

- LHC upgrade time-line and plans.
- Current status of the ATLAS detector.
- Motivation for ATLAS upgrades.
- Multiphase upgrade plan for ATLAS:
  - Phase 0, Phase 1 and Phase 2.
  - Upgrade details focusing on LAPP and LPSC contributions.
- Conclusions.



LHC foreseen schedule



$< \mu >$: Mean number of interactions per crossing.

LS1 $\rightarrow$ Phase-0

- Design energy: $\sqrt{s} = 13 - 14$ TeV.
- Nominal luminosity: $\mathcal{L} = 10^{34}$ cm^{-2}s^{-1} ($< \mu > \sim 27.5$).
- Bunch spacing 25 ns.
- Expect to collect $\sim 75 - 100$ fb^{-1} per experiment by 2017.

LS2 $\rightarrow$ Phase-1

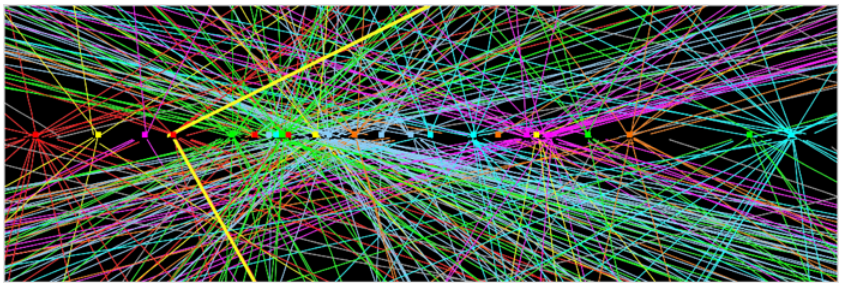
- Design energy: $\sqrt{s} = 14$ TeV.
- LHC peak luminosity: $\mathcal{L} = 2.2 \times 10^{34}$ cm^{-2}s^{-1} ($< \mu > \sim 60$).
- Bunch spacing 25 ns.
- Collect a total luminosity of 300 fb^{-1} per experiment by 2021.

LS3 $\rightarrow$ Phase-2 (HL-LHC)

- Design energy: $\sqrt{s} = 14$ TeV
- LHC peak luminosity: $\mathcal{L} \sim 5 \times 10^{34}$ cm^{-2}s^{-1} ($< \mu > \sim 140$)
- Collect a total luminosity of 3000 fb^{-1} per experiment by the early 2030.

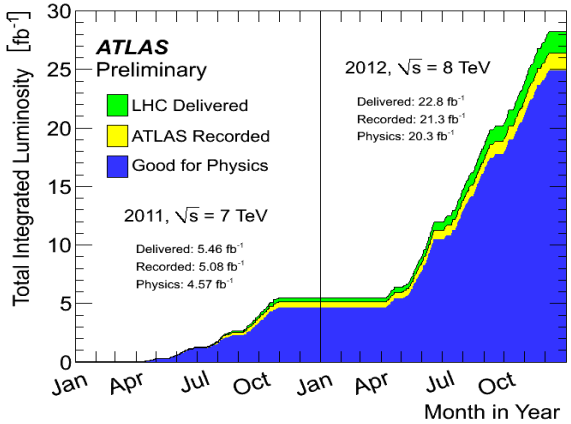
Current ATLAS performance

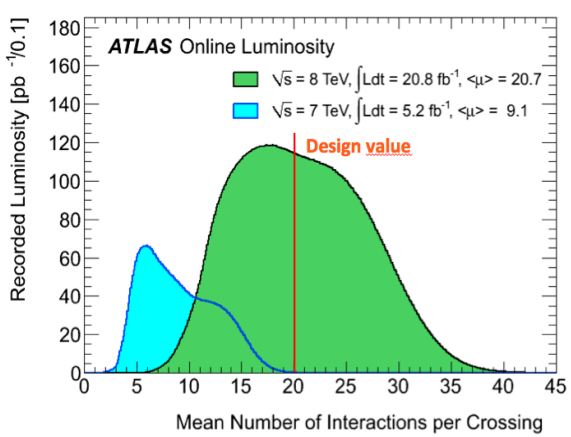
- High detector operation and data quality efficiency:
  - Detectors, trigger and DAQ systems working very well.
  - Average fraction of operational channels very close to 100% for all subsystems.
- Pileup challenge:
  - Reach higher values of pile-up without degrading performance.
  - Twice more pileup in 2012 than in 2011.

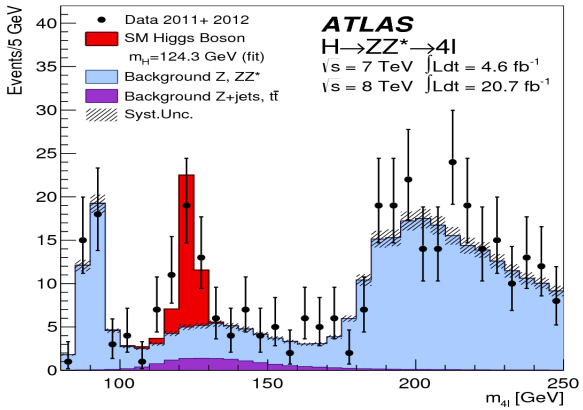


$Z \rightarrow \mu\mu$ event recorded on April 15th 2012 (25 reconstructed vertices).

- Excellent physics results $\rightarrow$ 265 public papers.







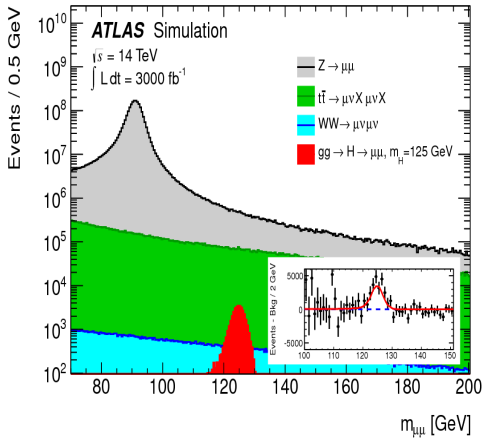
Physics motivation for upgrading - Higgs Sector

Signal strength: $\mu = (\sigma \times BR)/(\sigma \times BR)_{SM}$

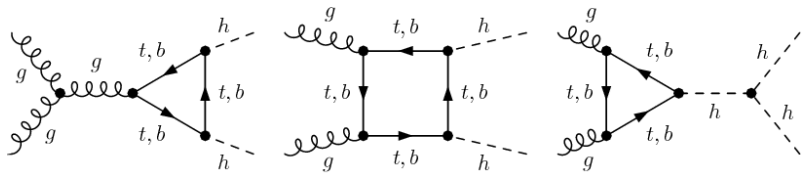
- Spin and CP violation in Higgs sector.
- BSM Higgs boson searches.
- High event rate will allow measuring existing channels with higher precision.
  - Observation of rare Higgs processes & couplings measurements.
    - e.g. $H \to \mu^+\mu^-$ channel allows the coupling to 2^{nd} generation fermions to be probed.

$L[fb^{-1}]$	300	3000
Signal significance	2.3σ	7.0σ
$\Delta\mu/\mu$	46%	21%

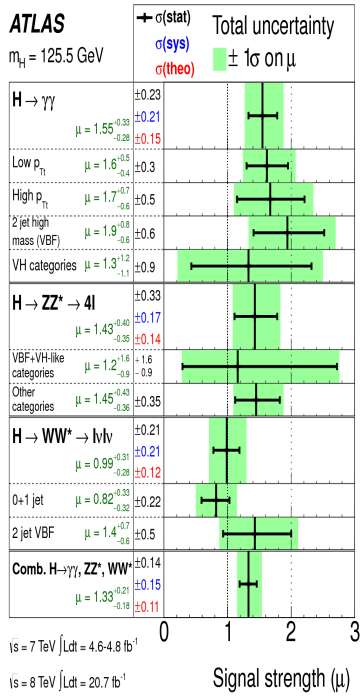
Inclusive $H \to \mu\mu$ expectation (ATL-PHYS-PUB-2013-007).



- Higgs self-coupling.

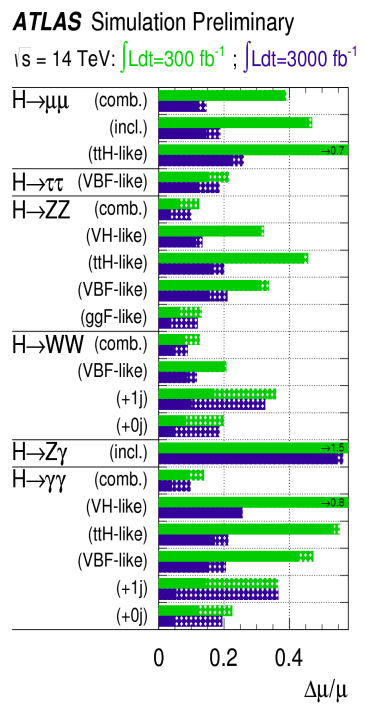


Current ATLAS result:



μ for a SM—like Higgs boson (Phys. Lett. B 726 (2013), pp. 88-119).

Expected ATLAS performance:



Uncertainty on μ for a SM—like Higgs boson (ATL-PHYS-PUB-2013-014).

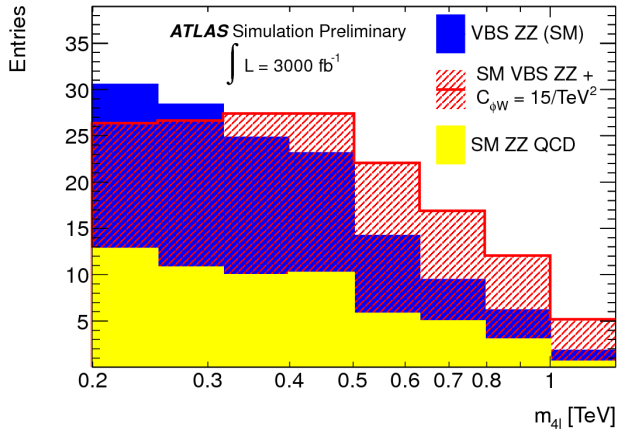
Physics motivation for upgrading - BSM Sector

More energy and luminosity will extend the search energy range for specific BSM scenarios:

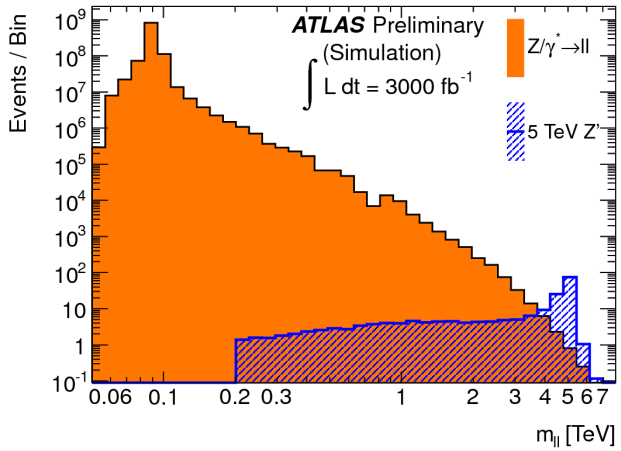
- Vector boson scattering (WW, ZZ and WZ).
  - Crucial test of EWSB dynamics and the nature of the Higgs.
- Exotics searches.
  - e.g. high-mass $t\bar{t}$ resonances or Z' with di-lepton resonances.

model	300 fb^{-1}	3000 fb^{-1}
$g_{kk} \to t\bar{t}$	4.3 (4.0) TeV	6.7 (5.6) TeV
$Z'_{topcolor} \to t\bar{t}$	3.3 (1.8) TeV	5.5 (3.2) TeV
$Z'_{SSM} \to ee$	6.5 TeV	7.8 TeV
$Z'_{SSM} \to \mu\mu$	6.4 TeV	7.6 TeV

- FCNC top-decays.
- Supersymetry searches.



Reconstructed 4-lepton mass spectrum for $ZZ + jj \to \ell\ell\ell\ell + jj$ with $m_{jj} > 1$ TeV (ATL-PHYS-PUB-2013-006).

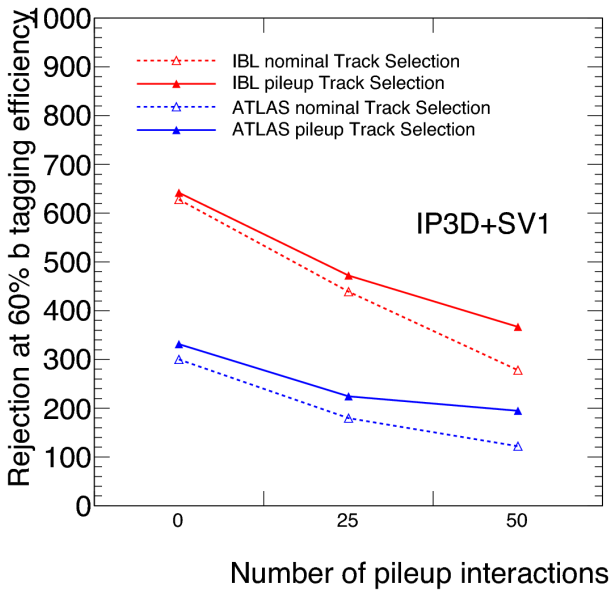


Reconstructed di-electron mass spectrum for the Z' search (ATL-PHYS-PUB-2013-007).

Ongoing ATLAS upgrade during LS1 (2013-2014) → Phase0

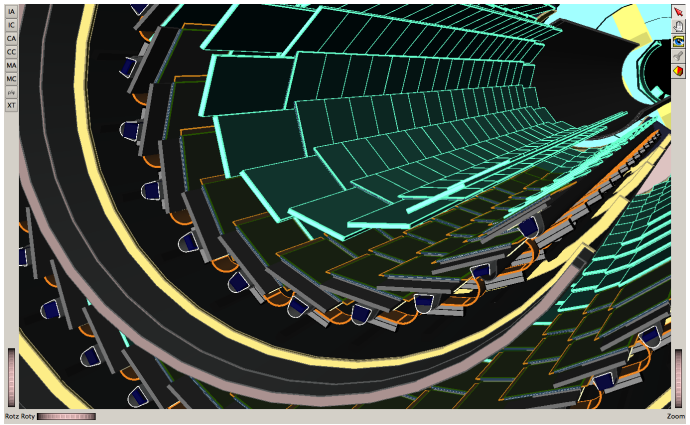
- New components:
  - **New 4^{th} layer for current Pixel detector: Insertable pixel b-layer (IBL) (ATLAS-TDR-19).**
    - IBL improves tracking, vertexing & b-tagging & robustness of Inner Detector (ID)
  - New Service Quarter Panel (nSQP).
    - To move the optical link components to an accessible location.
  - New Diamond Beam Monitor (DBM).
  - Added Endcap Extension (EE) Muon Chambers to improve acceptance for $1.0 < |\eta| < 1.3$.

Light jet rejection in $t\bar{t}$ events for 60% b-tagging efficiency vs average n° of pileup interactions (CERN-LHCC-2010-013).



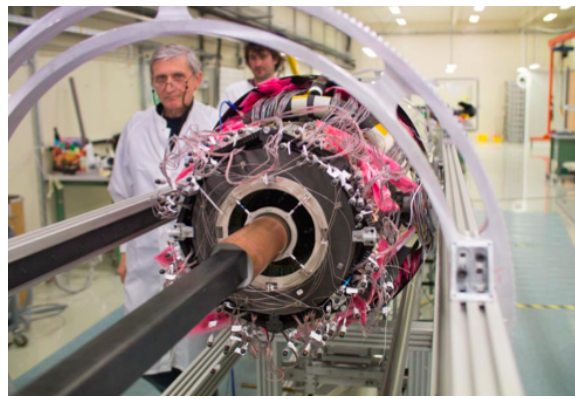
- Consolidation of existing detectors:
  - New Al (forward region) and Be (central region) beam pipes.
  - Upgrades to Level-1 Central Trigger.
  - Replace all calorimeter Low Voltage Power Supplies.
  - New neutron shielding in toroid end-cap.
  - Upgrade the magnets cryogenics.

Insertable B Layer (IBL)



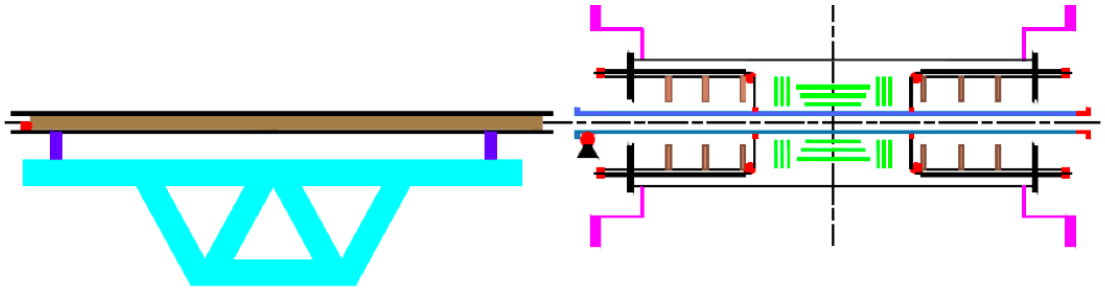
- IBL features:
  - Proximity to IP ($5.05 \rightarrow 3.27$ cm).
    - Improvement of impact parameter resolution.
  - Radiation harder than current 1^{st} pixel layer.
    - Improved radiation hardness to withstand 2×10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$.
  - Small pixel size ($50 \times 400 \rightarrow 50 \times 250 \mu m^2$).
    - Higher resolution and reduction of occupancy.
  - New technologies: planar pixel sensors, 3D sensors, new readout chip.

- Integration into the pixel detector:
  - April 2013 - pixel detector on surface.
  - July 2013 - inserted Inner Support Tube (IST) to separate IBL from the remaining Pixel Detector.
  - October 2013 - pixel detector is completely assembled.
    - Detector efficiency has been improved (95% to 99%).
  - December 2013 - pixel detector back in cavern.
  - May 2014 - installation underground of IBL in the pixel detector.
  - Will stay until the end of Phase-1.



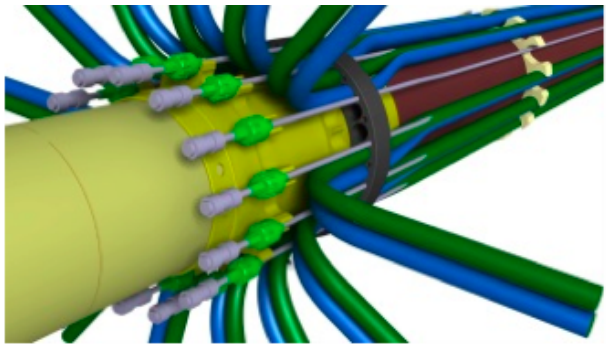
Insertable B Layer (IBL) - Integration & services

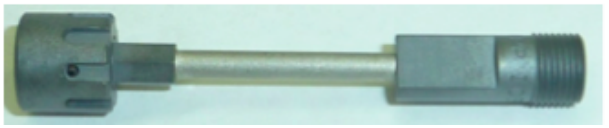
- Insert IBL in between the support tube and beam pipe is very challenging
  - LPSC group designed the Insertion/Extraction table to guarantee the movement, in and out of the IBL and IST inside the cavern.



- LAPP is responsible for the design and construction of cooling components from IBL staves to splitter:
  - Developed the cooling titanium connectors (sphere on cone).
  - Axon electric connectors (tiny format).

  Stringent requirements:
  - Small clearance ($\sim$ 10 mm) to fit inside a limited volume and minimize budget material.



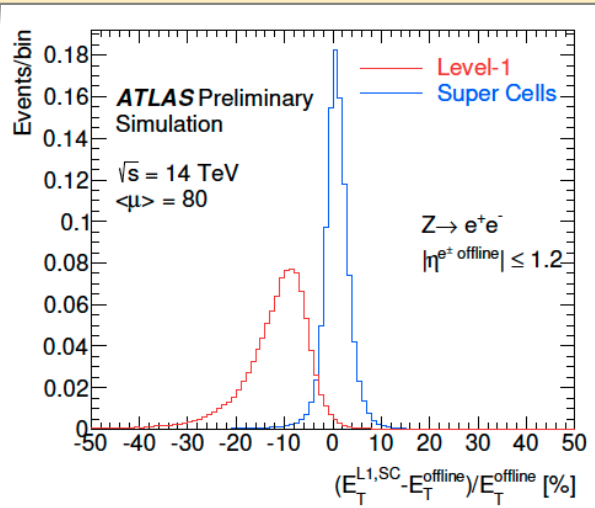


- Design of the services layout, installation between the USA15 and the IBL package and production of the cables (LPSC & LAPP).

ATLAS Upgrade plans for LS2 (2018) $\rightarrow$ Phase1

- Higher precision and finer granularity are required by the Level-1 trigger system in order to keep low thresholds.
  - **Partial upgrade of the Liquid Argon calorimeter trigger (ATLAS-TDR-022).**

Energy resolution using 3 $\times$ 2 Super Cell cluster E_T and the existing Level-1 E_T (ATLAS-TDR-022).

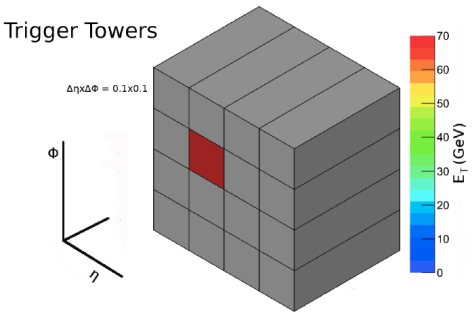


- Fast Track trigger (FTK) (ATLAS-TDR-021).
- Upgrades to Trigger and DAQ (ATLAS-TDR-023).
- New Muon Small Wheels (NSW) for the forward muon spectrometer (ATLAS-TDR-020).
- ATLAS Forward Physics: new forward diffractive physics detectors under study.

All upgrades compatible with Phase-2.

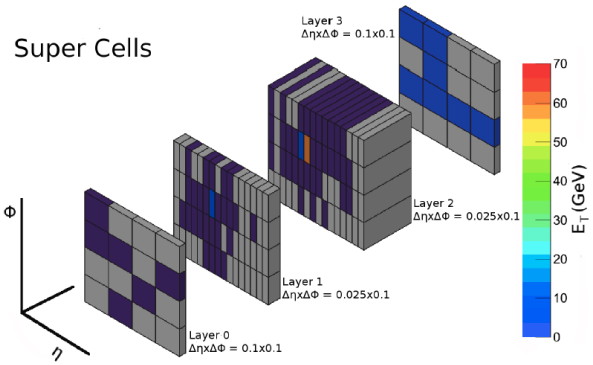
Calorimeter trigger upgrade

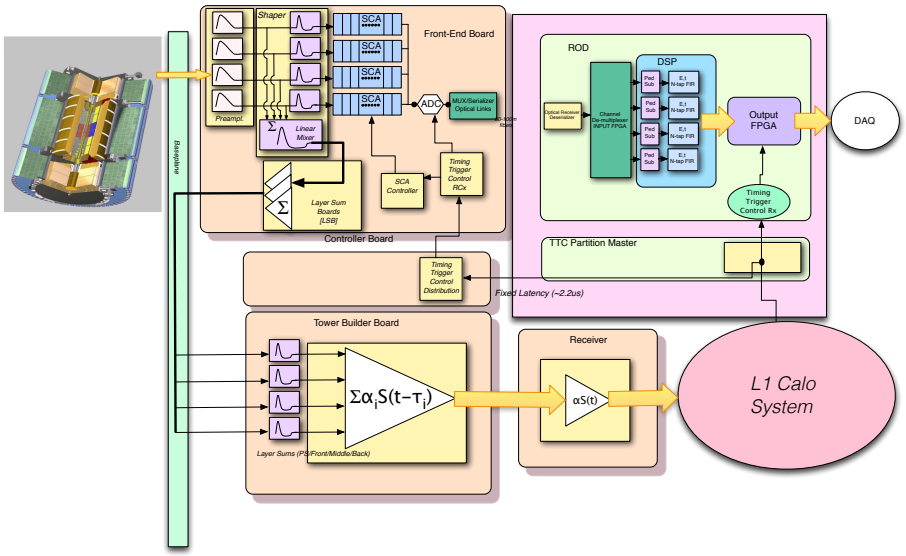
Current system

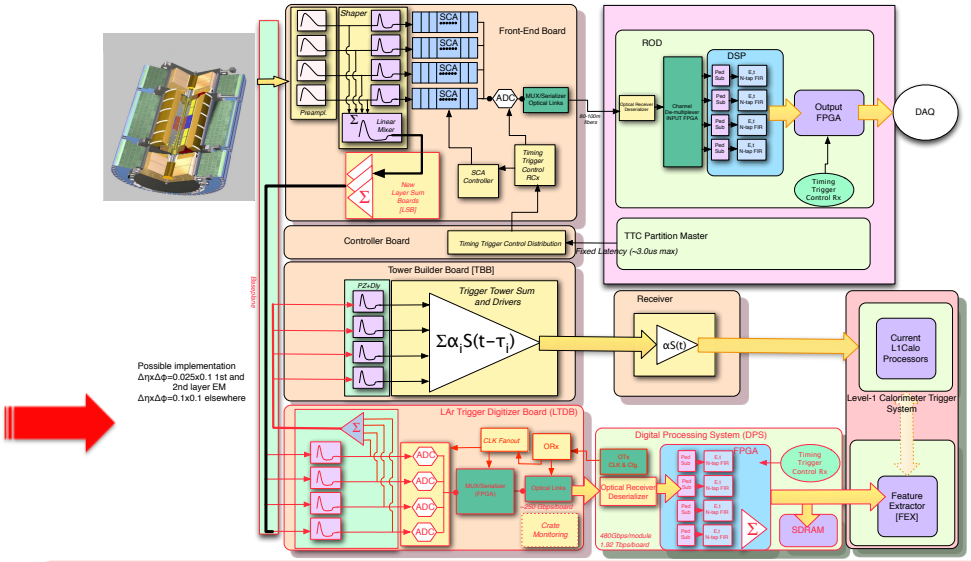


New finer trigger granularity
10 ”Super cells” per Trigger Tower

Upgraded system

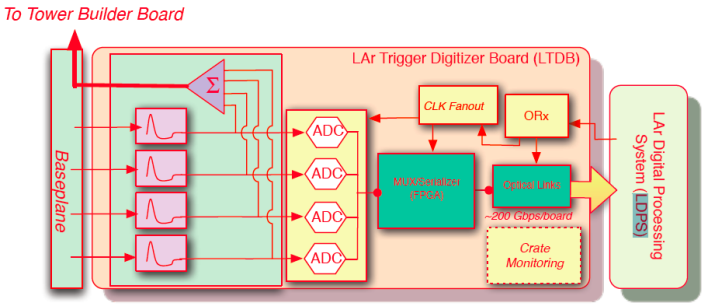






- LAr Trigger Digitizer Board (LTDB)
  → digitization of Super Cell signals (ADC).
- LAr Digital Processing Board (LDPB)
  → extract $E_T^{SuperCell}$ every 25 ns and send to Level-1.

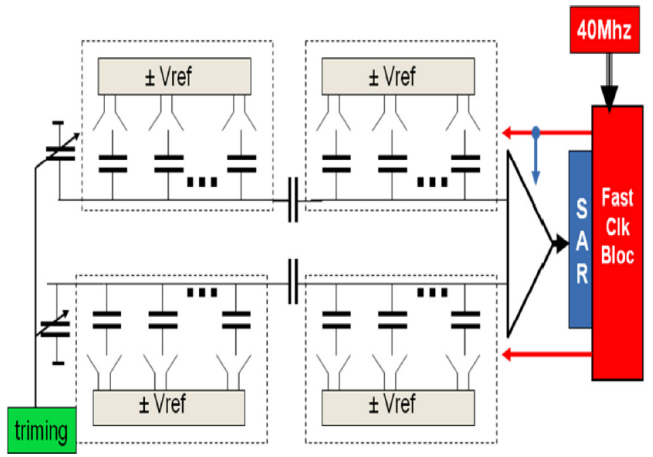
LAr Trigger Digitizer Board (LTDB) - PEALL ADC



- Main components of LTDB:
  - Analog section to provide the appropriate signals to the ADC (handle noise).
  - ADC to digitize the Super Cell signals.
- Stringent specifications for the ADC:
  - High frequency (40 $\mathrm{MS/s}$) and low latency (< 70 ns).
  - Small footprint and large dynamic range (12 bits).
  - Radiation hardness and low consumption (< 100 mW per channel).

- Three ADC have been considered for the LTDB:
  - A comercial ADC (Texas Instruments ADS5272).
  - Two ASIC developments based on the IBM 130 nm technology (approved by CERN):
    - 4-stage SAR-based pipeline ADC.
    - A full SAR-based architecture ADC.
- LAr collaboration will choose the ADC by March 2014.
- LPSC group designs the 12-bit, Power Efficient and Low Latency (PEALL) SAR ADC.
  - short latency (~ 25 ns) and a high speed clock internally generated from the 40 MHz clock and the comparator outputs
    $\rightarrow$ low power dissipation~ 30 $\mathrm{mW/ch.}$

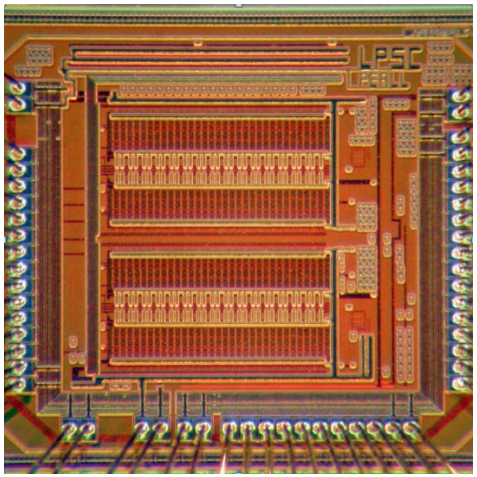
PEALL ADC schematic block diagram with an array of capacitors segmented in two.



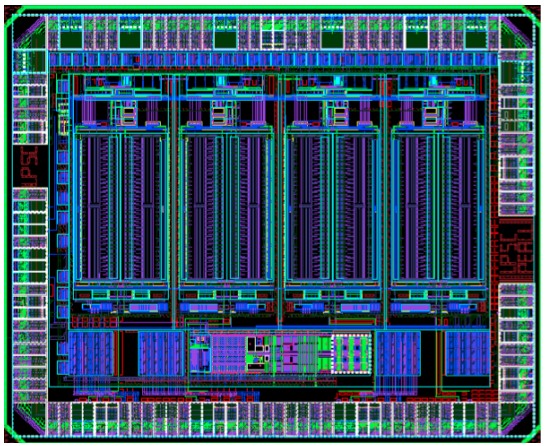
PEALL SAR ADC

INL: Integral Non-Linearity
LSB: Least Significant Bit

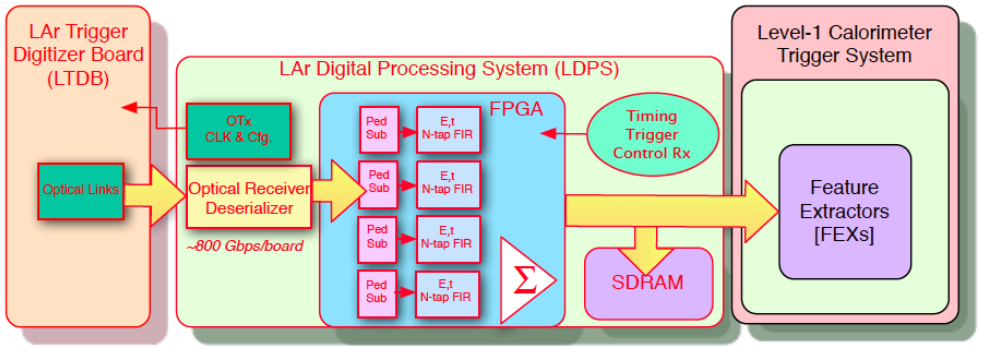
- A 1st prototype with 2 channels and with external reference voltage (V_{ref}) was tested on May 2013.
  - Local clock generator was working properly.
  - The power consumption per channel was estimated to be below 10 mW.
  - The design suffers from sampling noise at the V_{ref} (INL $= \pm 4$ LSB).



- A 2nd prototype with 4 channels and embedded V_{ref} was submitted on August 2013 and will be received on December 2013.
  - The linearity simulation results confirmed the proper functioning of the new integrated reference (INL $= \pm 1$ LSB).

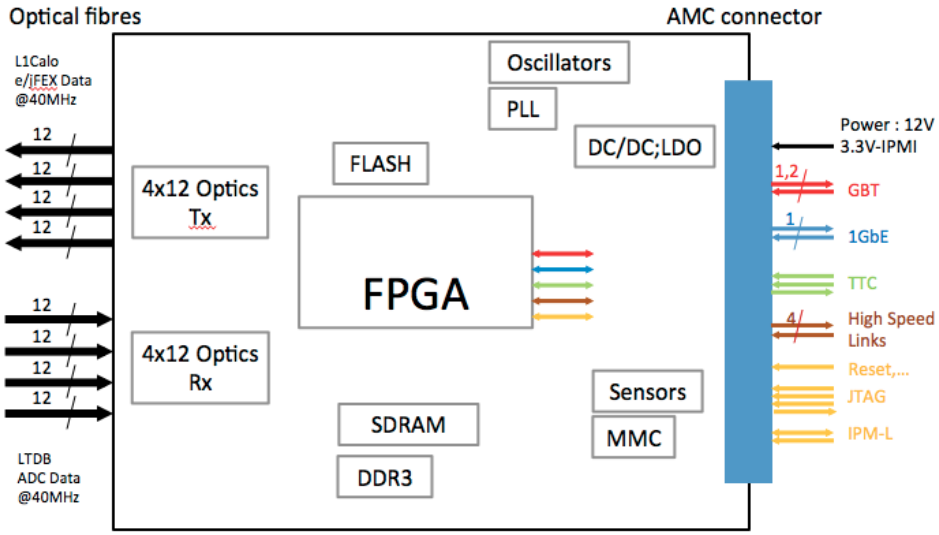


LAr Digital Processing System (LDPS) - ATCA board



- Key component of the Back End electronics upgrade to treat data coming from ADC:
  - 31 LAr Digital Processing Blades (LDPBs) in 3 ATCA (Advanced Telecom Computing Architecture) shelves.
  - each LDPB contains 4 Advanced Mezzanine Cards (AMCs).

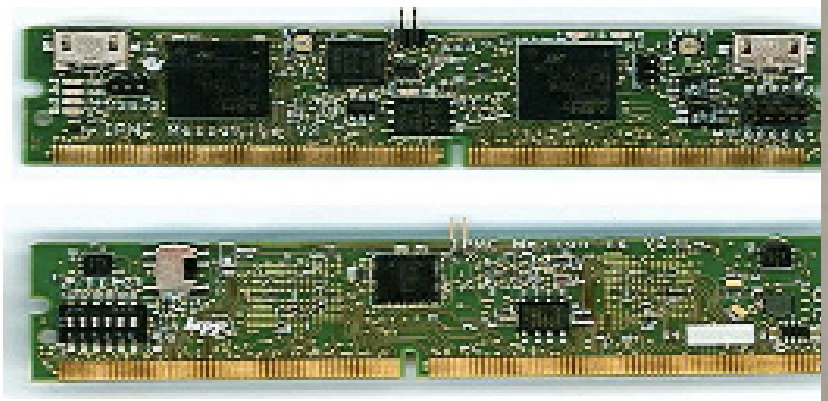
- Important contribution of LAPP group in the validation of the LDPS:
  - Design a test board to validate the commercial ATCA.
  - Design a new controlled board (IPMC).
- LAPP is responsible of the AMC PU on the ATCA boards.
  - High-bandwidth FPGA capable to reconstruct $E_T^{SuperCell}$ per bunch crossing with best resolution and high efficiency.

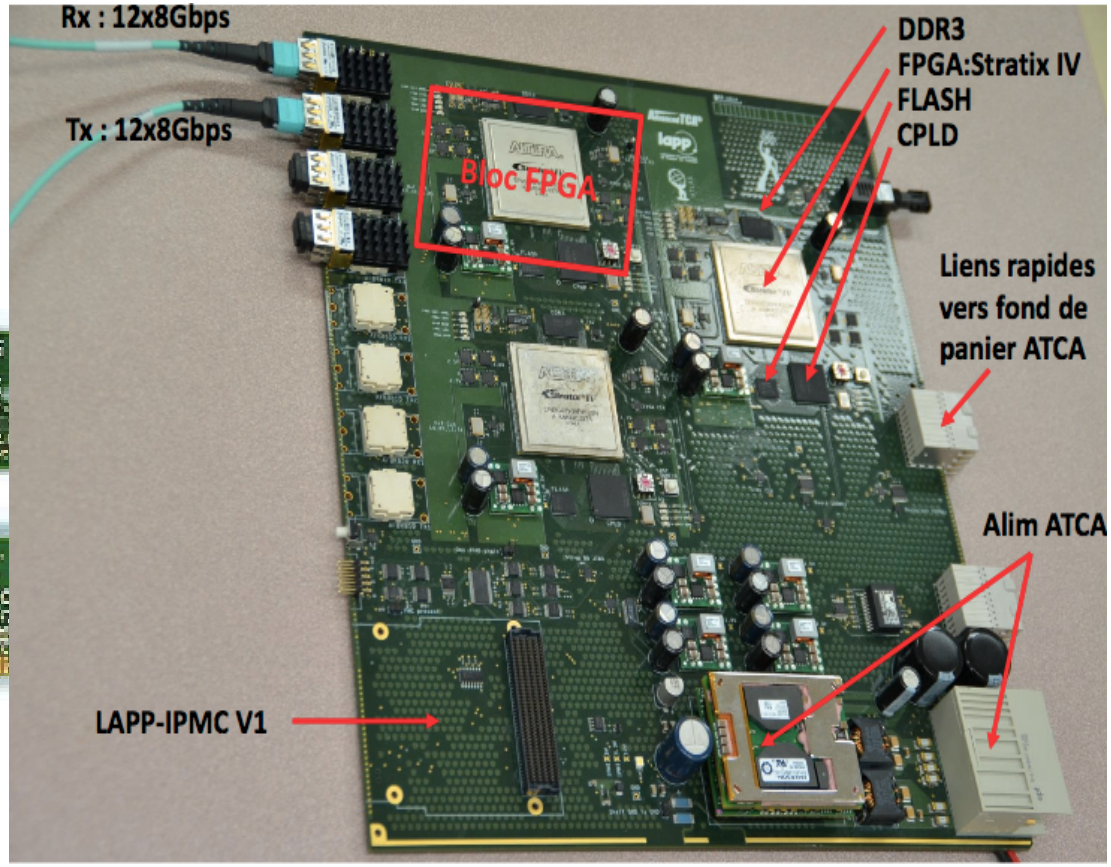


Block diagram of an AMC.

LAr Digital Processing System (LDPS) - pre-prototype

Controller mezzanine:
IPMC-V2.1





- The ATLAS Liquid Argon community plans to validate and install during LS1 a in-situ demonstrator to evaluate the proposed upgrade calorimeter trigger system.
- LAPP is involved on the validation of the whole Front-End chain on the surface.
- LAPP and LPSC will contribute on the trigger demonstrator installation and commissioning.

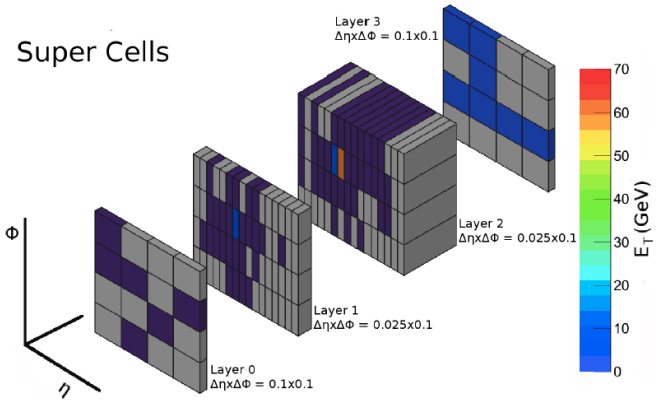
Figures of merit

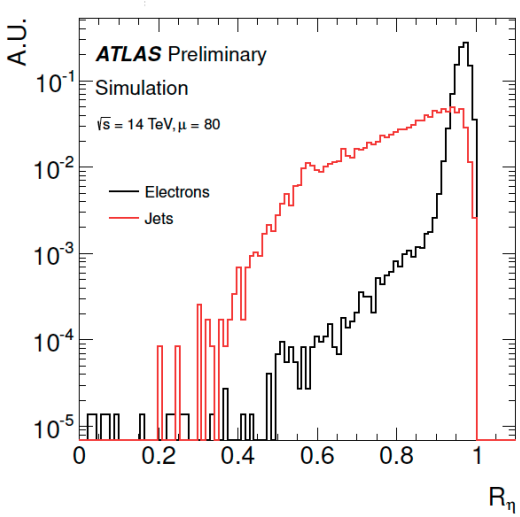
- Keep the Level-1 trigger rates at the current level:
  Exploit shower shape difference (e/γ vs. jets) at Level-1, similar to what is done today at the High Level Trigger

R_η: Transverse energy ratio defined by:

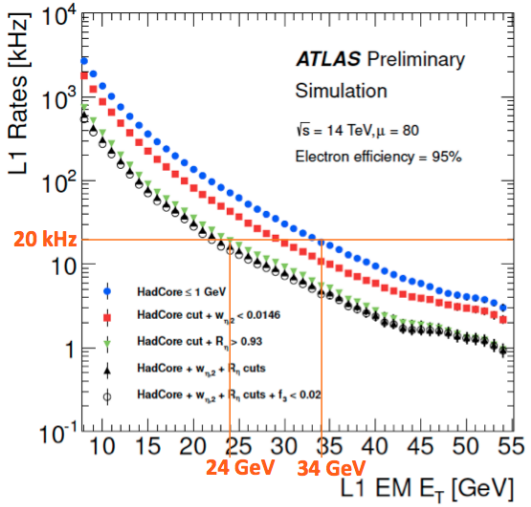
$$R_\eta = \frac{E^2_{T,\Delta\eta\times\Delta\phi=0.075\times0.2}}{E^2_{T,\Delta\eta\times\Delta\phi=0.175\times0.2}}$$

As expected narrower distribution for electrons compared with jets
$\rightarrow$ rejection of jet backgrounds.





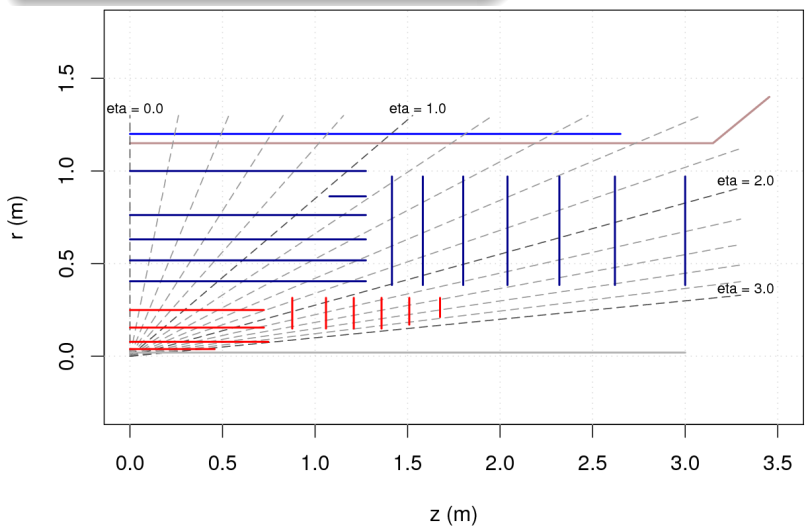
For an E_T threshold of 21.5 GeV the trigger rate decrease by a factor of 4 when selecting on R_η variable at 95% trigger electron efficiency.



ATLAS Upgrade plans for LS3 (2022-2023) $\rightarrow$ Phase2

- ATLAS detector needs to maintain the performance in a very challenging environment ($< \mu > \sim 140$):
  - **New Inner Detector.**
    - The current Inner Detector will reach the end of lifetime (radiation damage) by 2021.
    - Complete replacement of the entire Inner Detector (all Si).
    - Several options are considered for the pixel part:
      - Baseline layout
      - Conical layout.
      - Five pixel layers layout.
      - **Alpine pixel layout.**

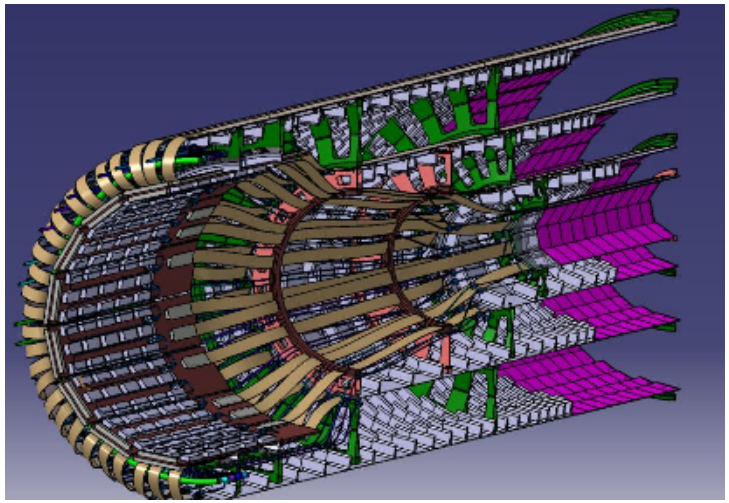
Baseline layout.



  - **Calorimeter electronics replacements.**
  - New forward calorimeter under study.
  - Trigger and data acquisition upgrades.
    - New Level-0/Level-1 trigger scheme.
  - Muon electronics replacements.

Alpine pixel detector

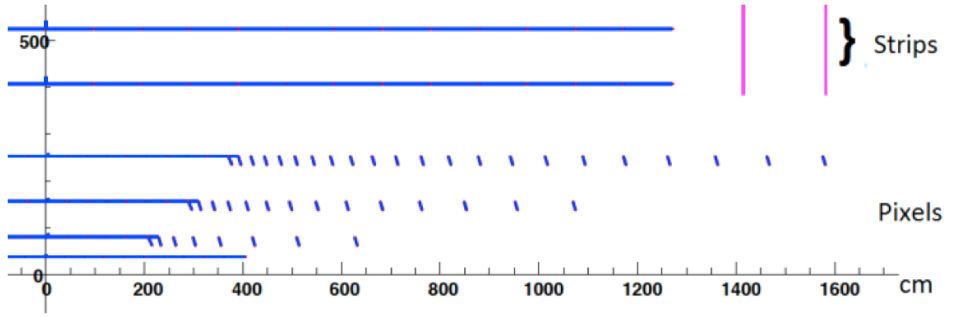
- Motivations:
  - Keep current tracking performance at HL-LHC.
    - Improve tracker granularity and the readout rates.
    - Possible forward extension for $2.5 < |\eta| < 4.0$. $\rightarrow$ Useful for forward jet selection (for Vector Boson Fusion) and forward electron selection reconstruction (for $H \rightarrow ZZ \rightarrow 4e$ and Vector Boson Scattering).
  - Due to extreme radiation conditions $\rightarrow$ more modular solution is needed.
    - Be able to replace damaged tracker elements.
- Ideal layout:
  - Sensors crossed perpendicularly by track coming from the IP to minimise material.
  - Constant track density per sensor across η.
- The Alpine pixel detector is a very innovative design proposed by LAPP inspired in this ideal solution.



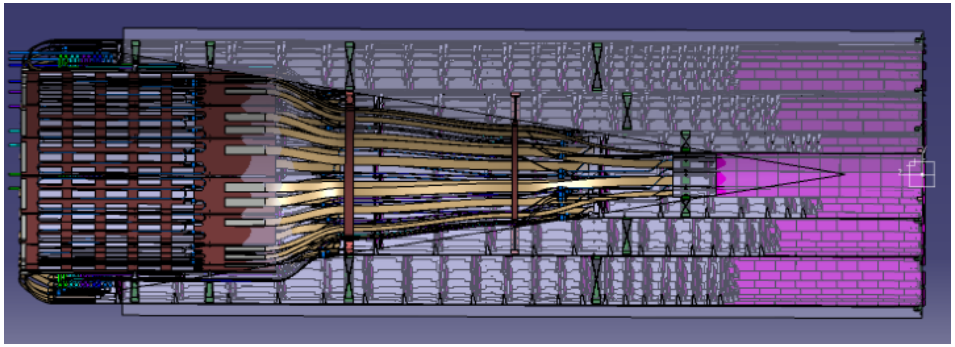
1/4 view of the Alpine geometry of the pixel tracker.

Alpine stave concept

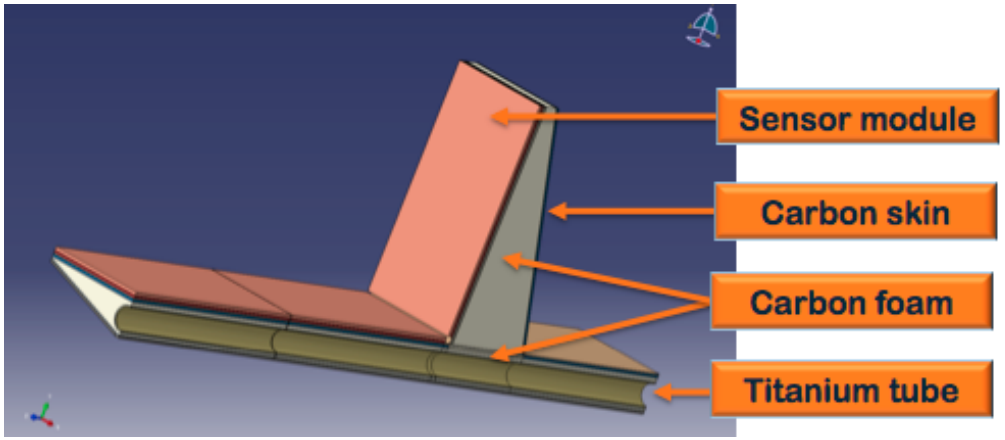
- Geometry layout:
  - The pixel sensor modules will be located at high rapidity ($1.0 < |\eta| < 2.7$) and increasing inclination angle (Alpine Stave).
  - Barrel part has baseline design.



- Advantages:
  - Reduce the amount of Si (from 8.2 m^2 to 4.6 m^2)
    $\rightarrow$ Reduce the cost.
  - All services out of tracking acceptance
    $\rightarrow$ Reduction of the dead material.

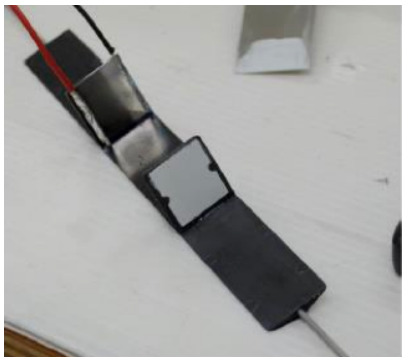


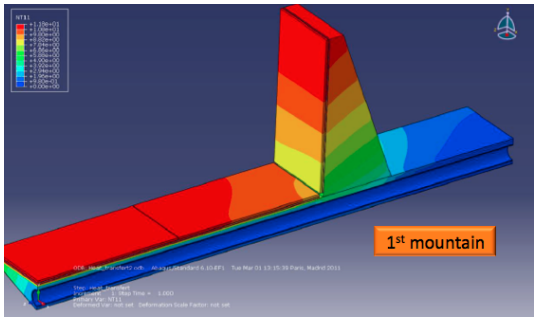
- Adapt cooling technologies successfully tested in IBL.
  - The IBL stave with carbon foam hold and cool sensors seen to be very efficient.
  - Need to be adapted to the new Alpine geometry.

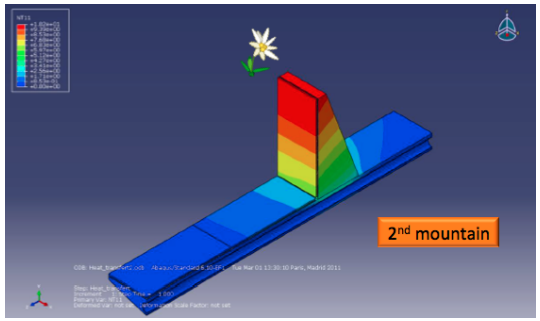


Performance and prospectives

- A mechanical prototype has been tested at LAPP.
  - The Alpine prototype is equipped with heaters and cooling to validate the thermal simulations.
  - The measurements show as expected a thermal spread of a few degrees and compatible results with simulation.
    - Ensure uniform response over sensor surface.





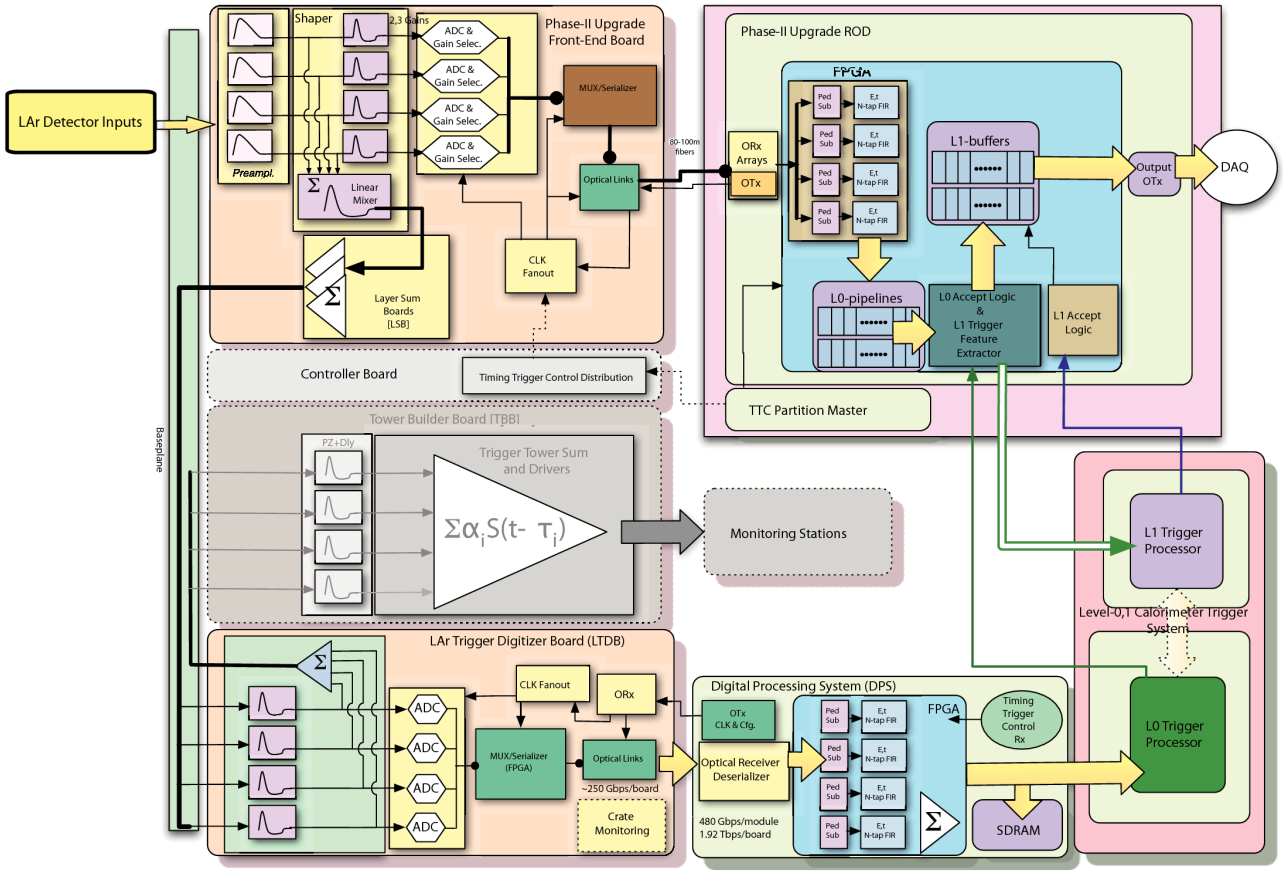


- A second real size prototype (1 m) is expected by early 2014.
- The final choice of the tracker design is planned to occur in 2017.

- Prospectives:
  - The ALPIX pre-project has been submitted by LAPP, LPHNE and LPSC for 2014 ANR campain:
    - LAPP will build a full Alpine Stave prototype and manage the thermal and electrical studies together with LPNHE.
    - LPSC will adapt the Alpine Layout to the full silicon tracker layout including the forward component.

Replacement of the calorimeter readout

- LPSC and LAPP plan to contribute in the Phase-2 calorimeter upgrade using their extensive expertises in LAr Calorimeter electronic.



New ROD for Phase-2 Upgrade will be designed.

- Large contribution of LAPP is expected (LAPP co-responsible of the RODs in the current system).

Front-end electronics will be replaced.

- LPSC starts to design a new ADC with largest dynamic range (14 bits).

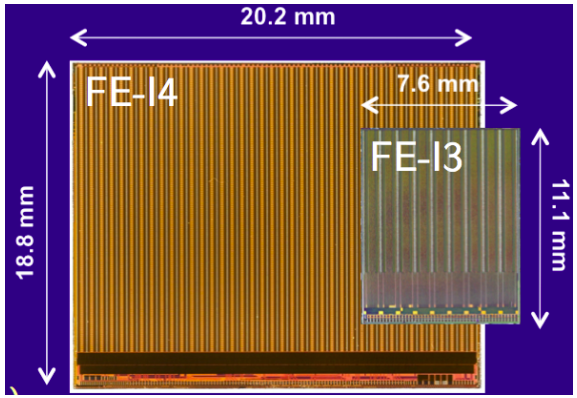
Conclusions

- ATLAS collaboration has planned an ambitious and extended upgrade program to reflect the changes in the LHC conditions towards the High-Luminosity LHC without loosing quality.
- Simulation studies confirmed that thanks to the upgrade program, ATLAS will be able to measure with very good precision the Higgs properties, study rare decay modes and look beyond the Standard Model.
- At each of the three upgrade phases LAPP and LPSC ATLAS group have an important contribution in the key elements of the upgrade program: Liquid Argon calorimeter and Inner detector upgrades.
  - Alpine pixel layout for HL-LHC is a very innovative design, close to the ideal layout and with a strong potential to be the next generation of tracking detectors.
- LABEX ENIGMASS funded two post-doc positions to work on ATLAS upgrade projects:
  - For LAr Calorimeter trigger upgrades (Started on May 2013).
  - For Alpine project (will start on 2014): http://inspirehep.net/record/1256985

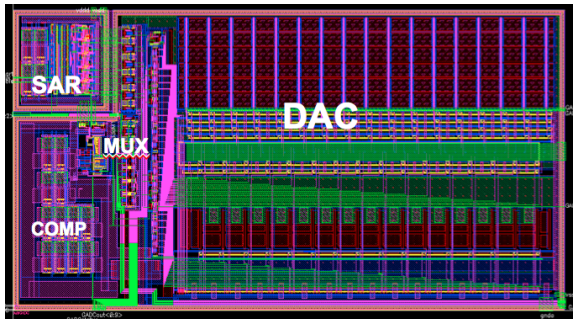
BACKUP

Insertable B Layer (IBL) - Readout technology

- New front-end chip (FE-I4) with new internal architecture;
  - To fulfil high occupancies and bandwidths.
- Features:
  - 4 cm^2: the largest ASIC in high energy physics.
  - 26880 channels
  - CMOS 130 nm technology.
  - 160 $\mathrm{Mb/s}$ data transfer.

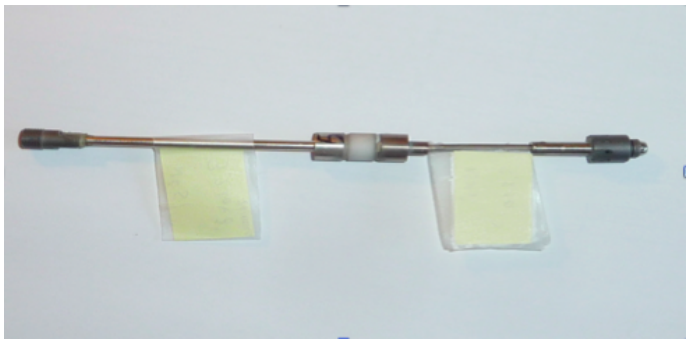


- LPSC and LAPP collaborated to design a general purpose ADC for monitoring and slow control with Successive Approximation Register (SAR) architecture and 10 bit precision.



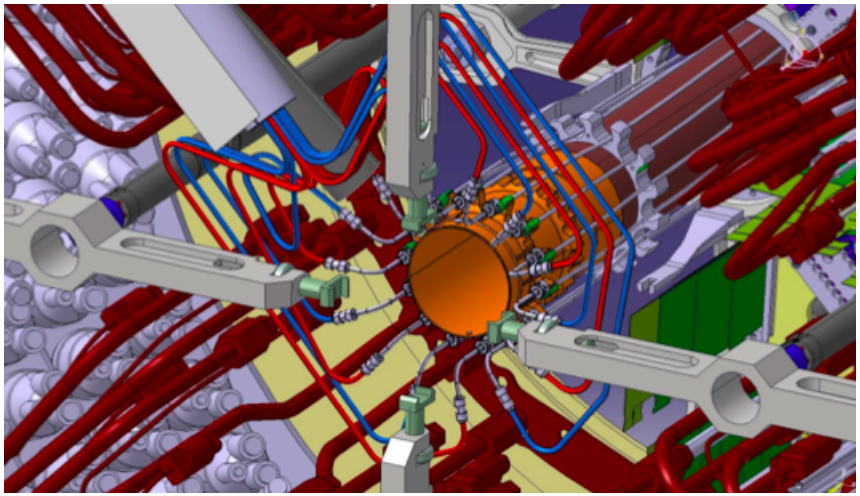
Insertable B Layer (IBL) - Cooling

LAPP responsible for the design and construction of cooling components from IBL staves to splitter.



Electrical insulator (new with this size):
Stainless steel Ceramic - Titanium

Routing of cooling lines from cooling on IBL staves to splitter
(blue and red tubes)
Including integration mockup



LAr Phase-1 time-line

Table 26. LAr Phase-1 Upgrade key dates for main deliverables. As explained in the text, these dates take into account constraints arising from shutdowns and periods of access to the detector and as such represent the latest dates for which these activities should be scheduled

Item	# units	Prod end	Prod start	PRR	FDR	PDR
Front-End						
Baseplane	124	5-2017	11-2016	9-2016	2-2016	
LSBs	2328	9-2017	9-2016	7-2016	12-2015	
Integrated LTDB	124	9-2017	3-2017	1-2017	6-2016	5-2014
Analog section	124*4	1-2017	10-2015	9-2015	4-2015	
Digital Components						
ADC	124*80	1-2017	10-2015	9-2015	4-2015	3-2014
ASIC Serializer	124*20	1-2017	10-2015	9-2015	4-2015	
ASIC Laser Driver	124*40	1-2017	10-2015	9-2015	4-2015	
VCSEL mezzanine (TOSA)	124*20	1-2017	10-2015	9-2015	4-2015	
DC Powering	124	1-2017	10-2015	9-2015	4-2015	
Optical pigtails	124*4	1-2017	7-2016	5-2016	10-2015	
Cooling plates	124*2	1-2017	7-2016	5-2016	10-2015	
Long Fibers	58	7-2017	1-2017	11-2016	4-2016	
Back-End						
LDPB	34	1-2017	10-2015	9-2015	4-2015	
AMC & FPGA	34*4	1-2017	10-2015	9-2015	4-2015	10-2014
IPMC	34*1	1-2017	10-2015	9-2015	4-2015	
MMC	34*4	1-2017	10-2015	9-2015	4-2015	
Optical pigtails	34*4	1-2017	10-2015	9-2015	4-2015	
MicroPod Cooling block	34*4*8	1-2017	10-2015	9-2015	4-2015	
Carrier Board & RTM	34	1-2017	10-2015	9-2015	4-2015	10-2014