

R&D on inner-tracking at BESIII with CMOS Pixel Sensors

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introduction

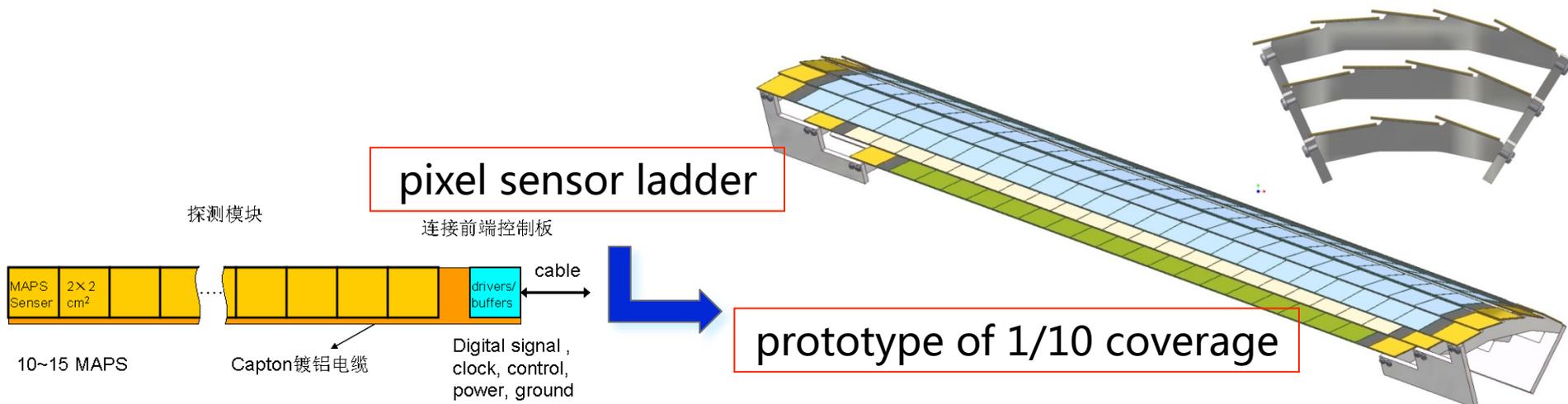
- about BESIII-CPS project
 - R&D for upgrading inner layers of BESIII Main Drift Chamber with CPS (CMOS Pixel Sensors)
 - aimed to build a prototype of 1/10 coverage
 - obtained NSFC support: 2.8 MRMB, 2013 – 2016
- the collaboration
 - IHEP, Beijing: **OUYANG Qun**, JIANG Xiaoshan, DONG Mingyi, QIN Zhonghua, MA Xiaoyan, ZHANG Hongyu, WU Linghui et al.
 - SDU, Jinan: **WANG Meng**, ZHANG Liang, LIU Qingyun
 - IPHC, Strasbourg: **Marc WINTER**, Christine HU et al.

collaboration activities

- regular group meeting between IHEP and SDU
- monthly teleconference between IPHC and IHEP
- visits
 - Apr. and Oct., Marc and Christine visited China twice
 - Oct, Meng visited Strasbourg
 - Dec, DONG Mingyi and QIN Zhonghua met Leo and Christine at CCUN to discuss visiting STAR-PXL group at Berkeley
- 20th Dec 2013, a dedicated workshop at SDU to discuss the project's plan and schedule
- this month, 4 people will visit Berkeley to learn chip test, ladder construction, mechanical design, etc

BESIII inner tracking requirements

- coverage: 3 layers, $1/10 \sim 800 \text{ m}^2$
- spatial resolution: $\sim 100 \mu\text{m}$
- counting rate: $\sim 10^4 \text{ Hz/cm}^2$
- material budget: $< 0.5\% X_0/\text{layer}$ ($< 1.5\% X_0$ all layers)
- power consumption: $0.2 - 0.3 \text{ W/cm}^2$
- room temperature operation

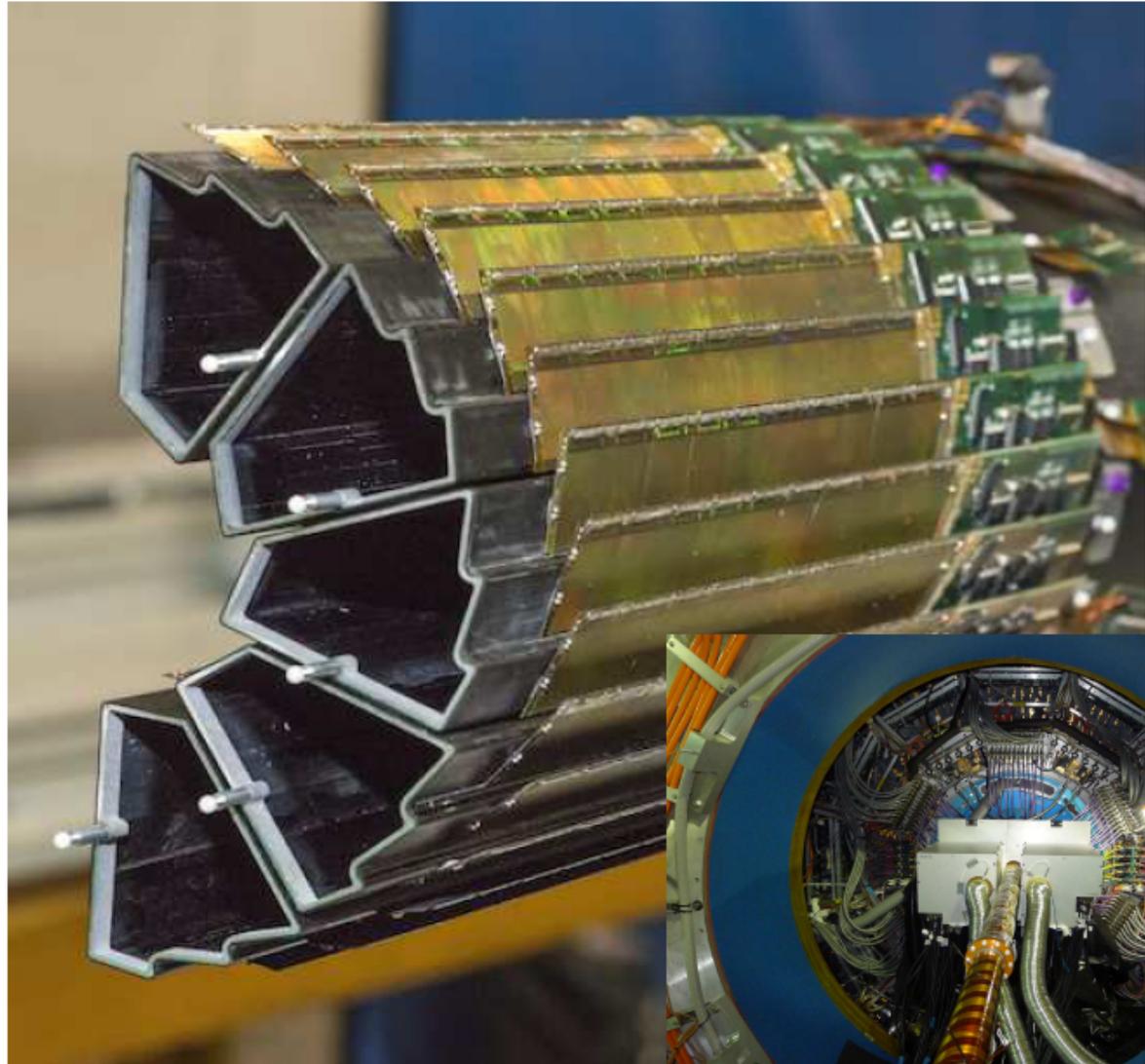


1st vertex detector using CPS

STAR-PXL

HALF-BARREL :

- 20 ladders (0.37% X_0)
- 200 sensors
- $180 \cdot 10^6$ pixels
- air flow cooling :
 $T \lesssim 35^\circ\text{C}$
- $\sigma_{sp} < 4 \mu\text{m}$
- rad. load \gg ILC values
- $t_{r.o.} \simeq 190 \mu\text{s}$
 \hookrightarrow ILC : $\mathcal{O}(10) \mu\text{s}$!



Full detector running with AuAu coll. since March 2014

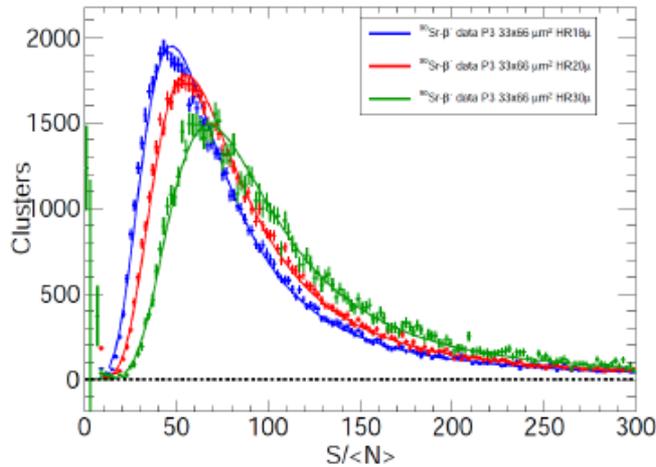
CPS for future large area tracking

- EVOLVING CPS FROM VERTEX DETECTORS TO (POSSIBLY LARGE AREA) TRACKERS :
 - * alleviated requirements on single point resolution & radiation tolerance
 - * more severe requirement on power consumption
- } New Trade-Off based on Large Pixels
- LIMITS IN ENLARGING THE PIXELS :
 - * Charge Collection Efficiency (CCE) decrease and pixel (bulk current) noise (TN) increase
 - ⇒ reduced SNR ⇒ potential degradation of detection efficiency
 - * Single point resolution degradation
 - MEANS TO MITIGATE THE SNR AND σ_{sp} DEGRADATION :
 - * Optimise sensing node geometry :
 - ↳ small diodes, large footprints (keeping P-wells away), ≥ 2 diodes/pixel, staggered diodes, ...
 - * Increase signal charge :
 - ↳ epitaxial thickness, depletion depth (epi resistivity, voltage)
 - QUESTIONS ADDRESSED WITH THE MIMOSA-34 SENSOR, FAB. IN 2013 :
 - * Sub-arrays composed of 16×64 pixels (30 diff. pixels \equiv sub-arrays)
 - * $22 \times 66 \mu m^2$ pixels tested on beam (4.4 GeV e^- , $T \simeq 30^\circ C$) in August 2013 (thinned to $50 \mu m$, EPI-20)
 - * $33 \times 66 \mu m^2$ pixels tested in the laboratory with ^{90}Sr source in 2014 (see next slides)

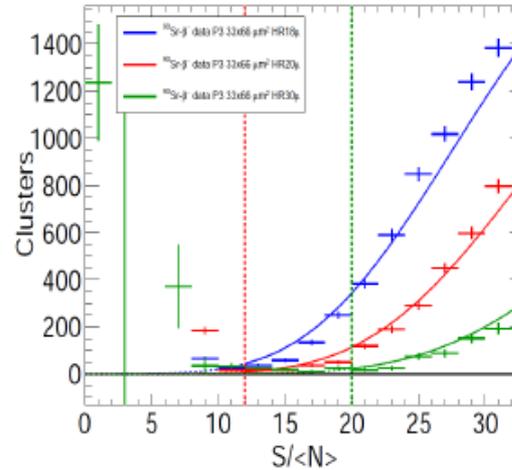
33 × 66 μm² pixels: SNR & ε_{det}

- 33 × 66 μm² pixels : SNR & ε_{det} obs. with β⁻ (⁹⁰Sr) for HR-18, HR-20 & HR-30

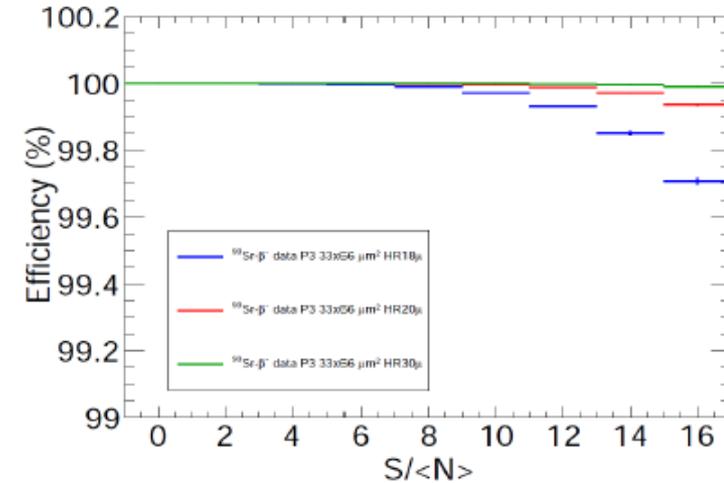
Seed pixel S/<N> for different HR Epi-layers



Seed pixel S/<N> for different HR Epi-layers



efficiency vs Seed pixel S/<N> cut for HR18 μm



- **Conclusions on the 33 × 66 μm² pixels :**

- * A single 8 μm² diode within 15 μm² footprint provides high SNR despite the large pixel
(≡ low sensing node density)
- * The HR-30 epitaxial layer leads to SNR ~ 70 (MPV) for ⁹⁰Sr β⁻ rays

⇒ **Safe to assume that 30 × 63/70 μm² pixels with in-pixel circuitry will be performing well (tbc)**

33 × 66 μm² pixels: spatial resolution

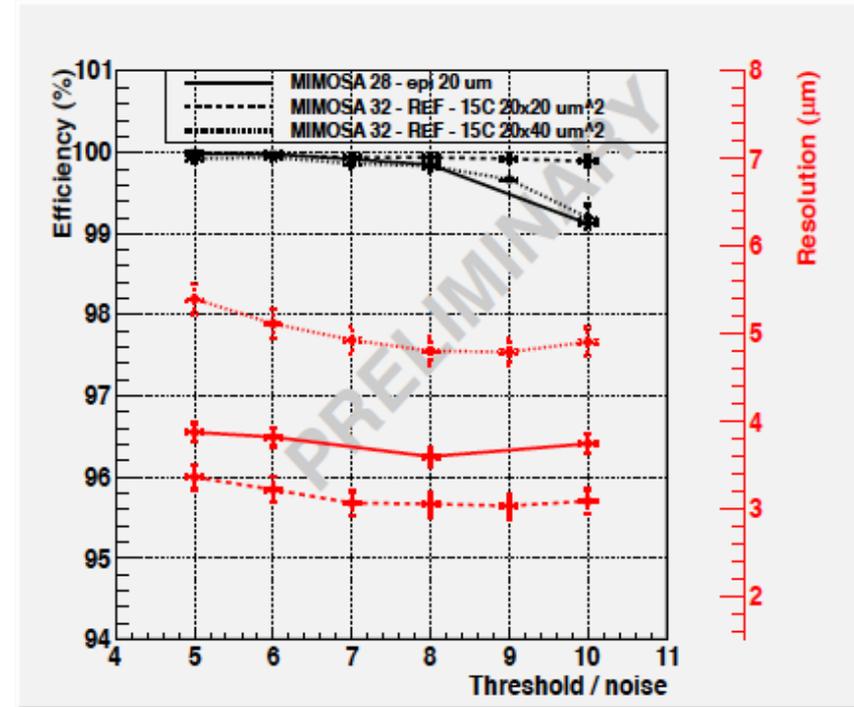
- Beam test (analog) data used to simulate binary charge encoding :

- ✳ Apply common SNR cut on all pixels using $\langle N \rangle$

- ↪ simulate effect of final sensor discriminators

- ✳ Evaluate single point resolution (charge sharing) and detection efficiency vs *discriminator threshold* for 20x20; 22x33; 20x40; 22x66 μm² pixels

- Comparison of 0.18 μm technology ($> 1 \text{ k}\Omega \cdot \text{cm}$) with 0.35 μm technology ($\lesssim 1 \text{ k}\Omega \cdot \text{cm}$)



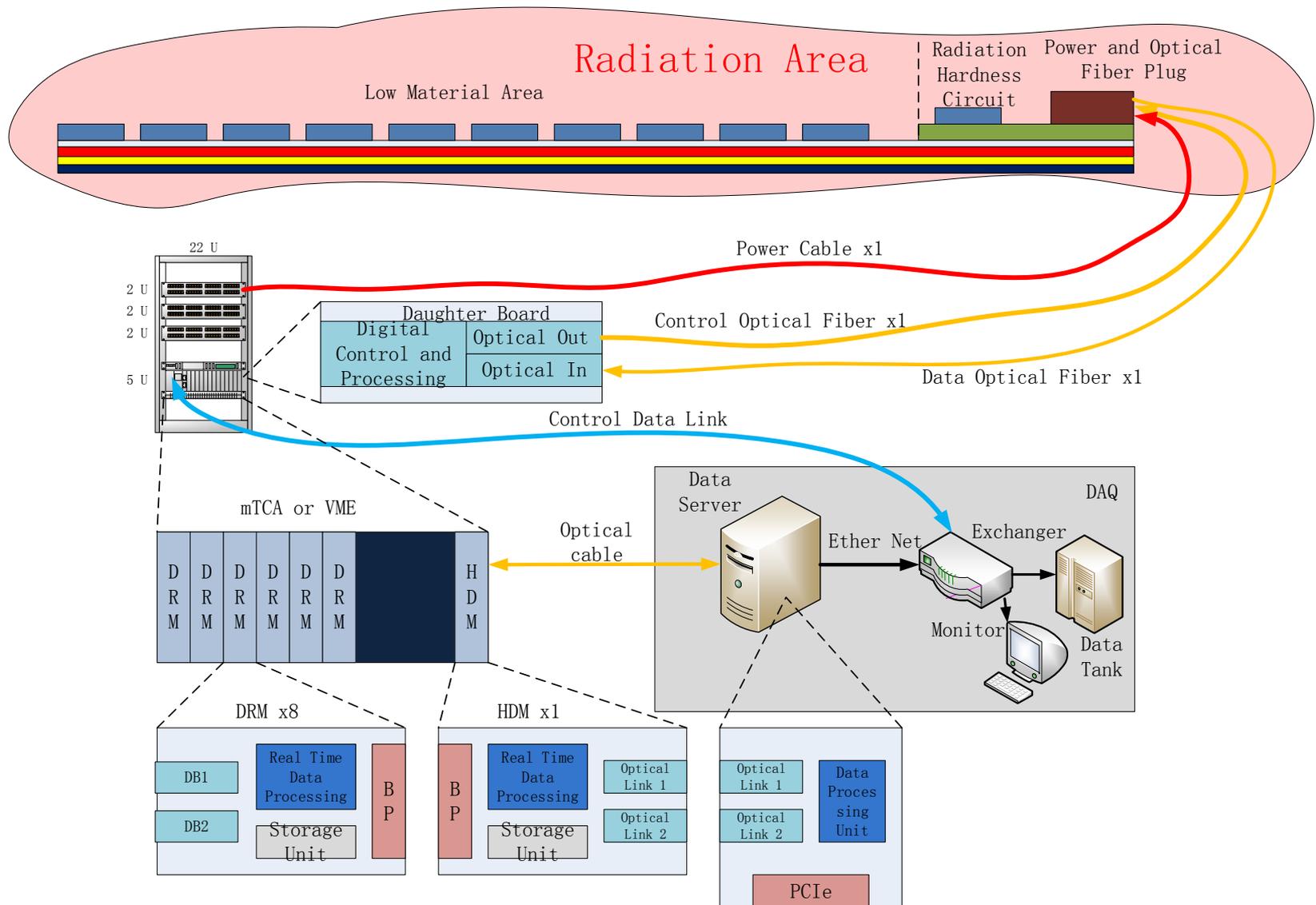
Process ▷	0.35 μm		0.18 μm			
Pixel Dim. [μm ²]	20.7×20.7	20×20	22×33	20×40	22×66	33×66
σ_{sp}^{bin} [μm]	3.7 ± 0.1	3.2 ± 0.1	~ 5	5.4 ± 0.1	~ 7	~ 10 μm ?

CPS FOR BESIII

prototype

- new layout
 - 3 single-sided layers
 - φ direction: 2 , 3 and 4 ladders for the 1st, 2nd and 3rd layer respectively
 - Z direction: 2 sets of ladders each layer
 - 20 chips with dimension of 2cm×2cm in each ladder

electronics – system scheme



electronics – progress

- design of front-end (10 chips per board)
 - design of the Schematic has been finished
 - discussed with PCB factory → production of Pi with the Aluminum line is possible
- DRM (Data Read Module)
 - The VME version is finished
 - The mTCA version is in developing
- Power Control Module
 - in developing
- HDM (High performance Data Procedure Module)
 - The VME version is finished
 - The mTCA version is in developing
- PCIe Card
 - The PCIe Optical Fiber Card is finished

simulation

- A full simulation package based on Geant4 for CPS is developed in BESIII offline software system.
- A tracking software has been developed. Track finding is implemented based on combination of CPS track seeds and MDC track segments. Kalman track fitting is used to provide accurate track parameters.
- Preliminary Monte Carlo study shows that both the momentum resolution and vertex resolution are significantly improved.
 - For 1 GeV muon track, momentum resolution is improved to 0.46% from 0.53% and vertex resolution in z direction is improved to 0.2mm from 1.6mm.

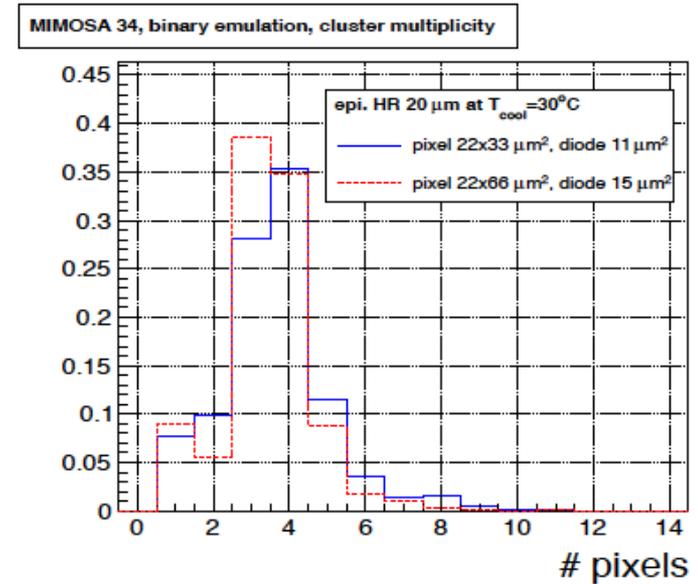
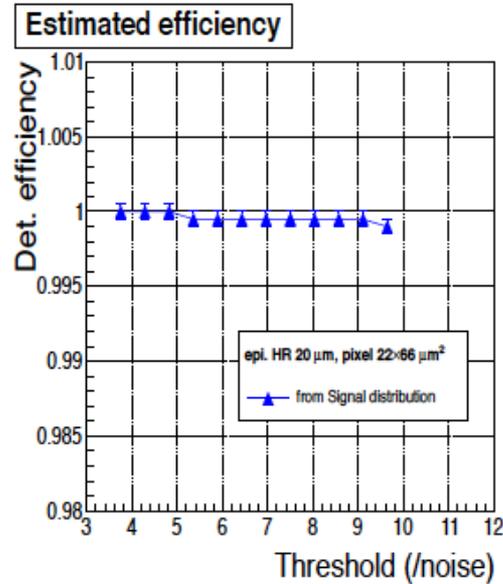
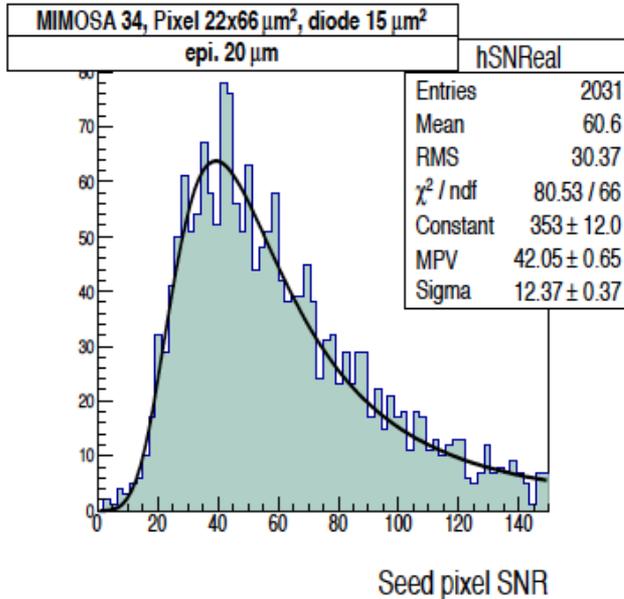
summary & outlook

- IHEP-SDU-IPHC partnership has been active in adapting CPS for BESIII inner tracking.
- The PICSEL group at IPHC has demonstrated that large pixels can achieve excellent detection efficiency ($33 \times 66 \mu\text{m}^2$) and very good spatial resolution ($\sim 7 \mu\text{m}$ for $22 \times 66 \mu\text{m}^2$).
- Progress has been made in prototype design, electronics and simulation.
- milestones in plan
 - 2014.12 ladder assembly study
 - 2015.4 first ladder
 - 2016.5 prototype construction

backup

Large Pixel Detection Performances

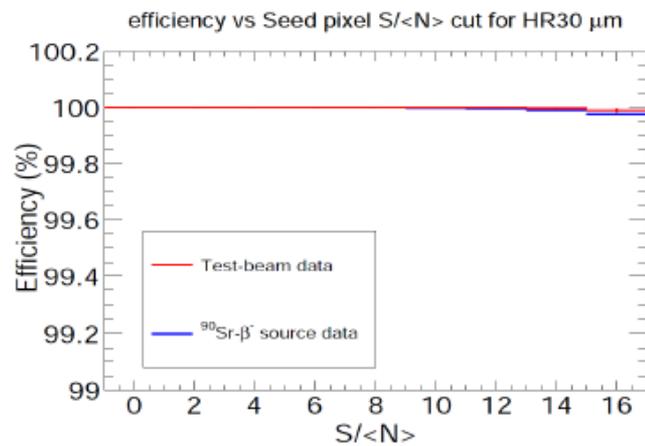
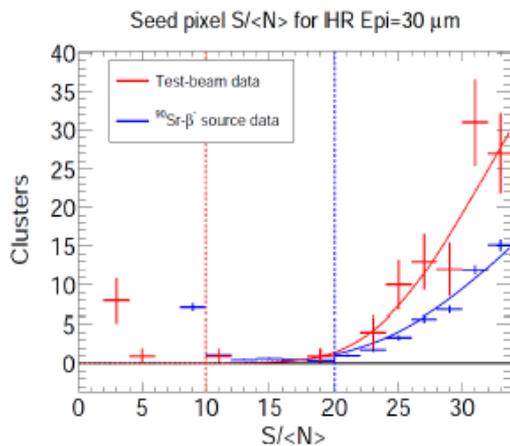
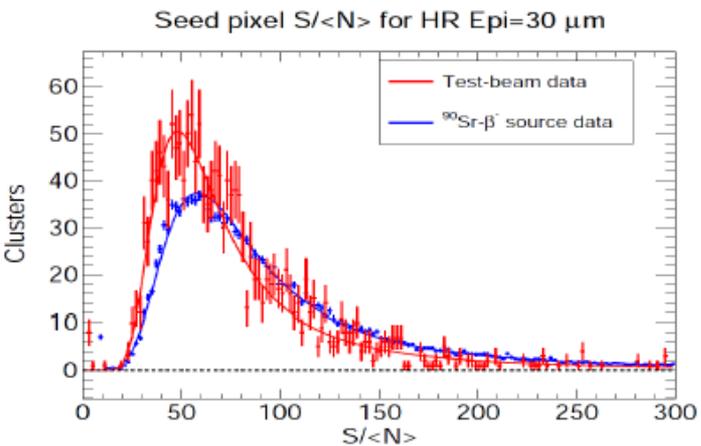
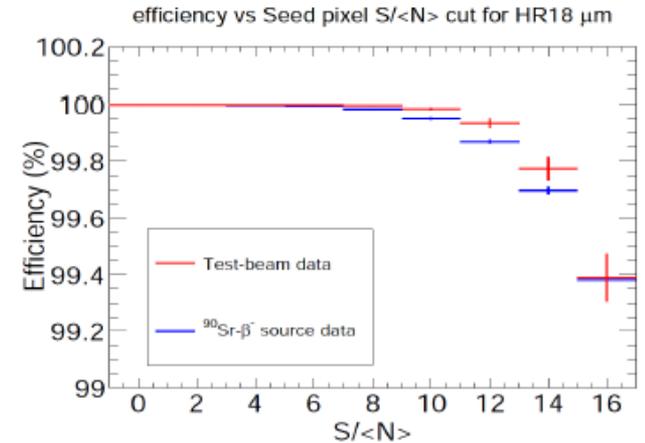
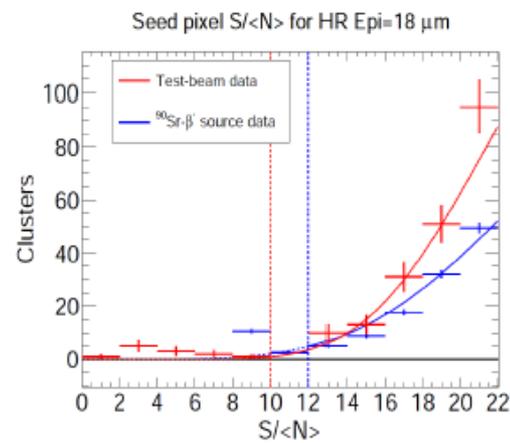
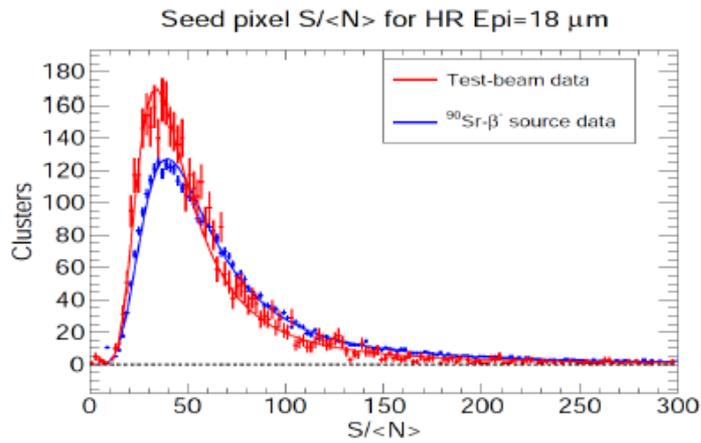
- MIMOSA-34 : $22 \times 66 \mu\text{m}^2$ pixels ($15/15 \mu\text{m}^2$ diode/footprint) tested at DESY in August 2013



- Difficulty : keep high CCE (all over the pixel) without substantial (capacitive) noise increase and gain loss
- Results : tests with 4.4 GeV electrons, no in-pixel CDS, no RTS noise mitigation
 - * $\text{SNR}(\text{MPV}) \simeq 42.1 \pm 0.7 \Rightarrow \epsilon_{\text{det}} \simeq 100 \%$
 - * cluster multiplicity (22×66) \simeq cluster multiplicity (22×33) $\simeq 3$ (mean)

22 × 66 μm² Pixels : β⁻ (⁹⁰Sr) vs 4.4 GeV e⁻

- 22 × 66 μm² pixels : SNR & ε_{det} observed with β⁻ (⁹⁰Sr) compared to 4.4 e⁻ for HR-18 & HR-30 (& HR-20)

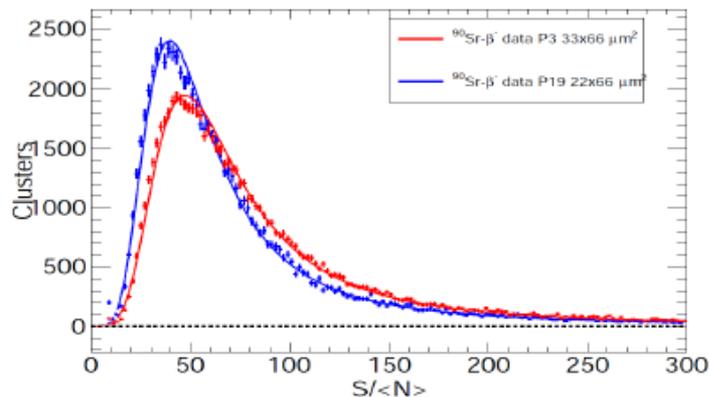


- Ccl : lab tests with β⁻ (⁹⁰Sr) source allow estimating the detection efficiency

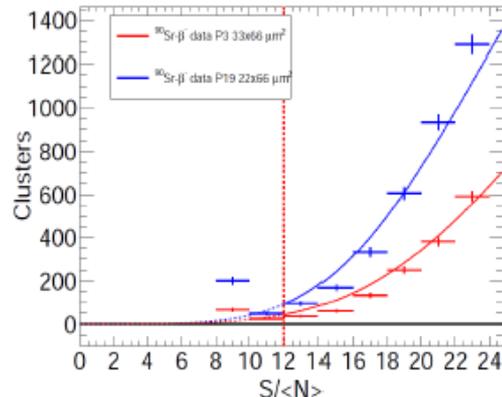
Moving from $22 \times 66 \mu m^2$ to $33 \times 66 \mu m^2$ Pixels

- $33 \times 66 \mu m^2$ vs $22 \times 66 \mu m^2$ pixels : SNR & ϵ_{det} obs. with β^- (^{90}Sr) for HR-18 & HR-30 (& HR-20)

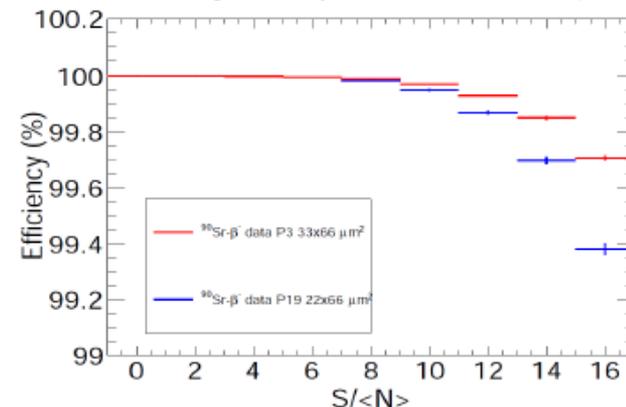
Seed pixel $S/\langle N \rangle$ for HR Epi=18 μm



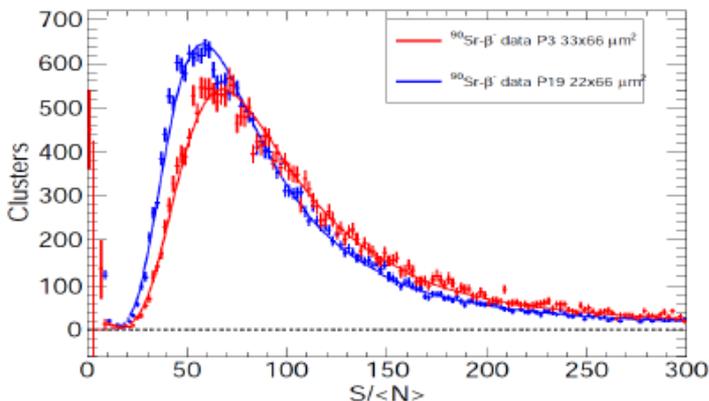
Seed pixel $S/\langle N \rangle$ for HR Epi=18 μm



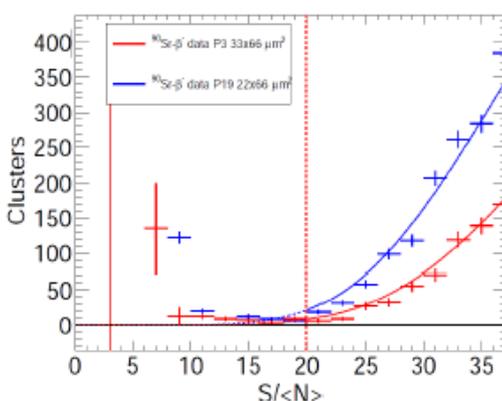
efficiency vs Seed pixel $S/\langle N \rangle$ cut for HR18 μm



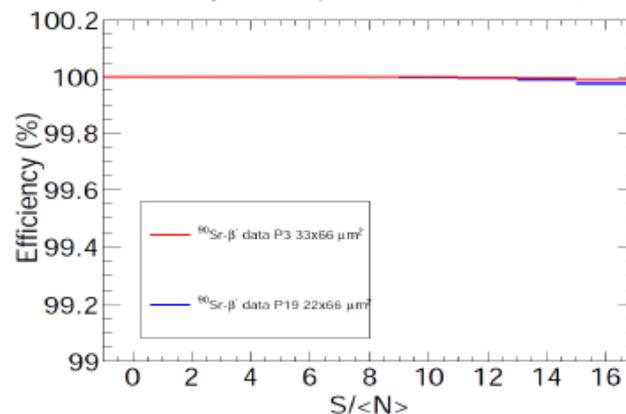
Seed pixel $S/\langle N \rangle$ for HR Epi=30 μm



Seed pixel $S/\langle N \rangle$ for HR Epi=30 μm



efficiency vs Seed pixel $S/\langle N \rangle$ cut for HR30 μm



- Ccl** : $33 \times 66 \mu m^2$ ($8/15 \mu m^2$ sensing node) pixels exhibit high SNR \rightarrow high ϵ_{det}

SUMMARY & CONCLUSION on Large Pixels

- **Modifications to be applied to CPS for tracking systems :**
 - * Trade-off between resolution and power fosters large pixels
 - * Large pixels may suffer from degraded detection efficiency and spatial resolution
- **Results of measurements performed with MIMOSA-34 chips :**
 - * Excellent detection efficiency obtained with largest pixels tested ($33 \times 66 \mu m^2$)
 - * Very good spatial resolution obtained with $22 \times 66 \mu m^2$: $\sim 7 \mu m$ in both directions
↳ presumably $\sim 10 \mu m$ for $33 \times 66 \mu m^2$ pixels
- **Next steps :**
 - * Assess larger pixel array integrating full FEE chain
 - * Assess radiation tolerance vs pixel dimensions and sensing node parameters