# Summary of the ILC and Future detectors/accelerators session

Philip BAMBADE & WANG Meng

*7th FCPPL Workshop, Clermont-Ferrand, 2014.4.10*

# Tuesday 08 April 2014

## Parallel session: ILC and Future detectors/accelerators (13:00-17:00)

- **Conveners: BAMBADE, Philip; WANG, Meng**

| time | title | presenter |
|---|---|---|
| 13:00 | French-Chinese collaboration on detector studies and physics optimisation for CEPC & FCC | RUAN, manqi |
| 13:40 | SDHCAL: Results and prospects | LAKTINEH, imad |
| 13:55 | Glass RPC for CMS phase-2 upgrade | LAKTINEH, imad |
| 14:15 | Study of HV CMOS Sensor for the Upgraded ATLAS Tracker in the High Luminosity LHC | LIU, Jian |
| 14:40 | Electronics in TUNE - ASIC and WR | LIU, Yinong |
| 15:00 | Coffee break | |
| 15:30 | Volcanoes tomography with muons | CARLOGANU, Cristina |
| 15:45 | Front-End electronics based on PARISROC ASIC for the LHAASO experiment | CHEN, Yingtao |
| 16:00 | R on using CMOS pixel sensors for tracking in BESIII | WANG, Meng |
| 16:15 | Diamond sensor development for beam halo and Compton process measurements at ATF2 | LIU, Shan |
| 16:30 | Theoretical computation and simulations of beam halo generation in ATF damping ring | WANG, Dou |
| 16:45 | Review of positron source R for linear colliders | CHEHAB, ROBERT |

- gaseous detector (GRPC) x2
- pixel detector x2
- electronics x2

# SDHCAL : Results and Prospects

I.Laktineh

IPNLyon

## OUTLINE

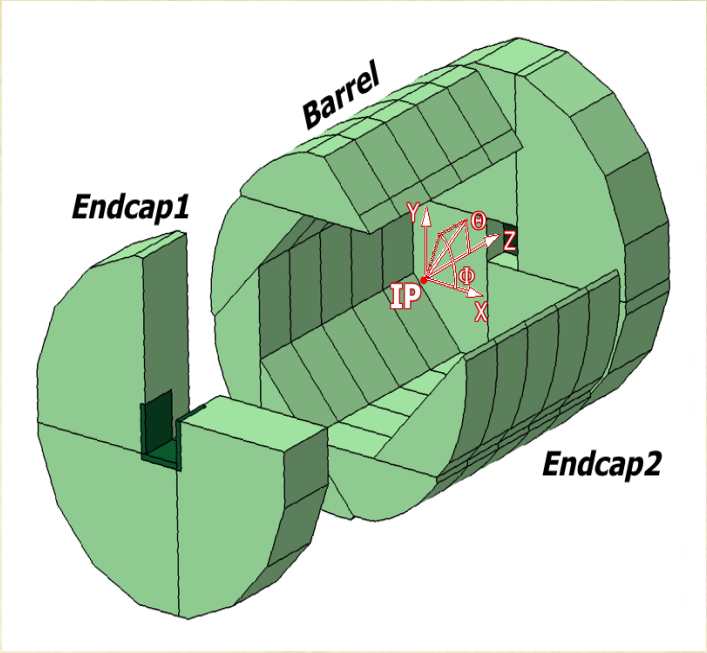
- SDHCAL for ILD
- SDHCAL prototype
- Prototype results
- Prospects
- Conclusion

SDHCAL collaboration :

France : **IPNL**, LAPP, LLR, LPC, OMEGA;
Spain : CIEMAT;
Belgium : UCL, Gent;
China : **Tsinghua** university, **NCEPU**;
Tunisia : Tunis university.

# SDHCAL-ILD

The SDHCAL-GRPC is one of the two HCAL options proposed in the **ILD L**etter **O**f **I**ntention (LOI). Modules are made of 48 RPC chambers ($6\lambda_I$) equipped with power-pulsing electronics readout.

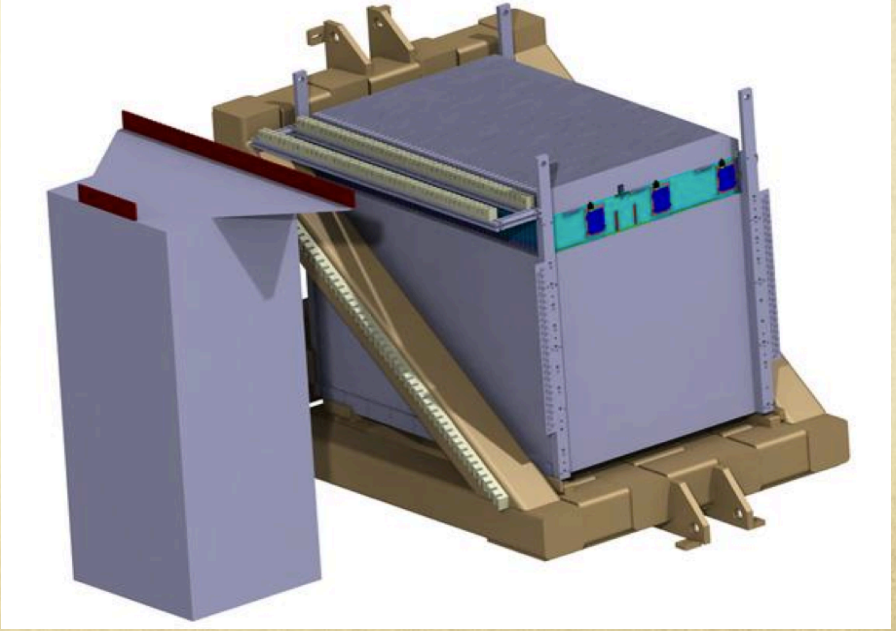



The structure proposed for the SDHCAL-ILD :

- Is self-supporting
- Has negligible dead zones
- Eliminates projective cracks
- Minimizes barrel / endcap separation (services leaving from the outer radius)

## SDHCAL Prototype

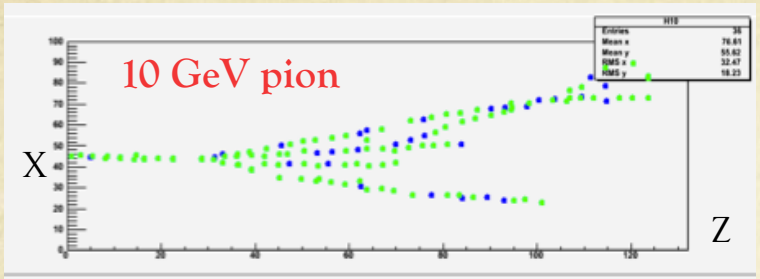
- Come as close as possible to the ILD module and be able to study hadronic showers
-48 units (active layer + absorber) fulfilling the ILD requirements.

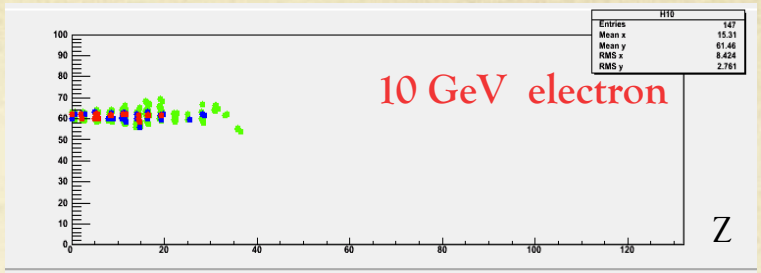


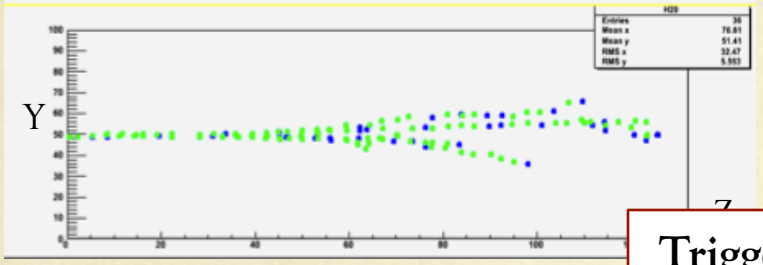
## Challenges

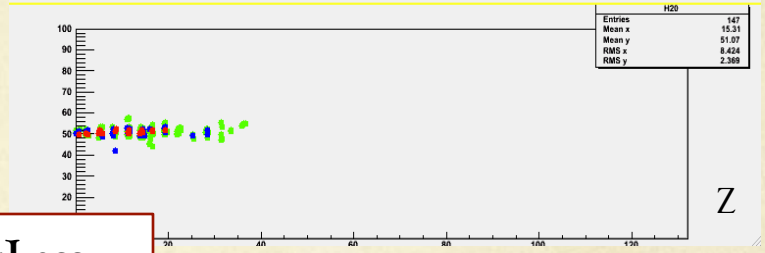
-Homogeneity for large surfaces
-Thickness of only few mms
-Services from one side
-Embedded power-cycled electronics
-Self-supporting mechanical structure

# Event display



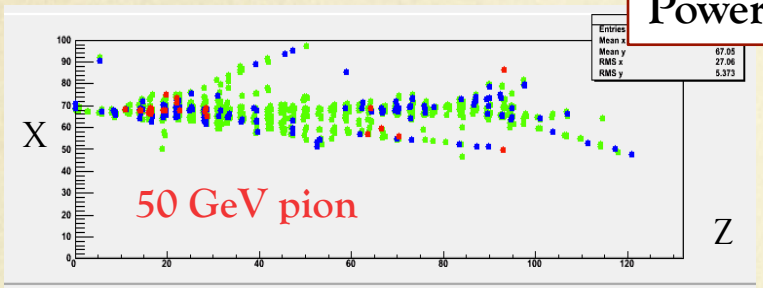



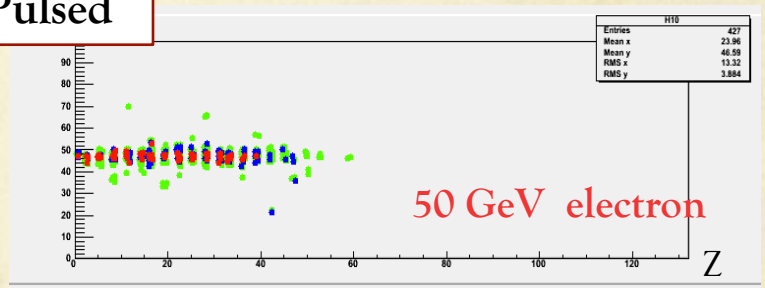



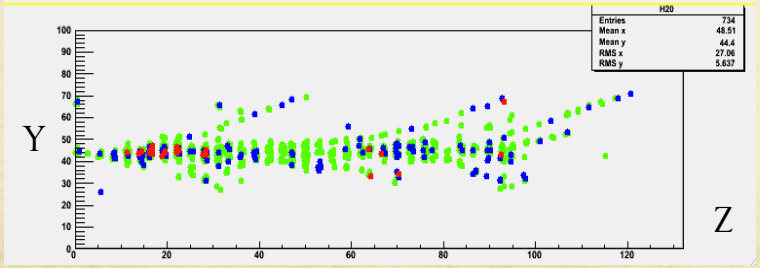



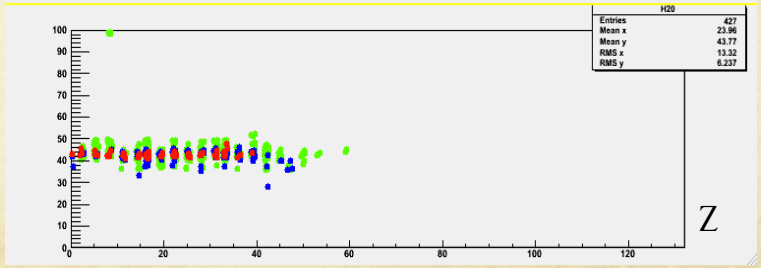

TriggerLess
Power-Pulsed

units in cm



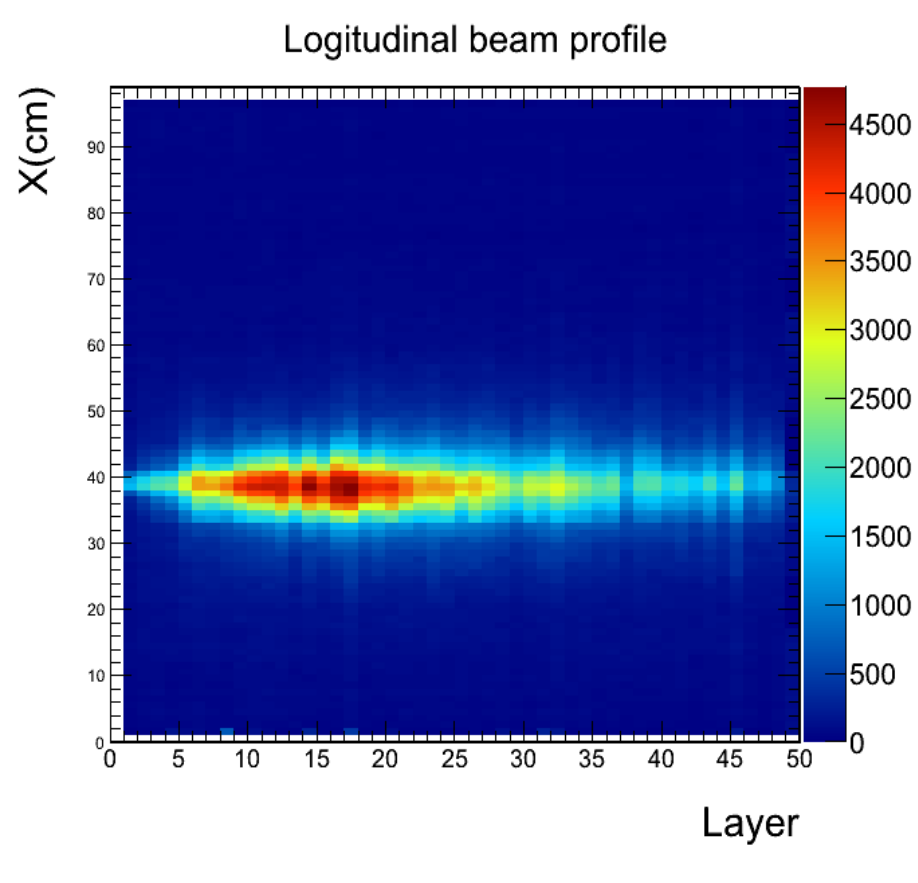



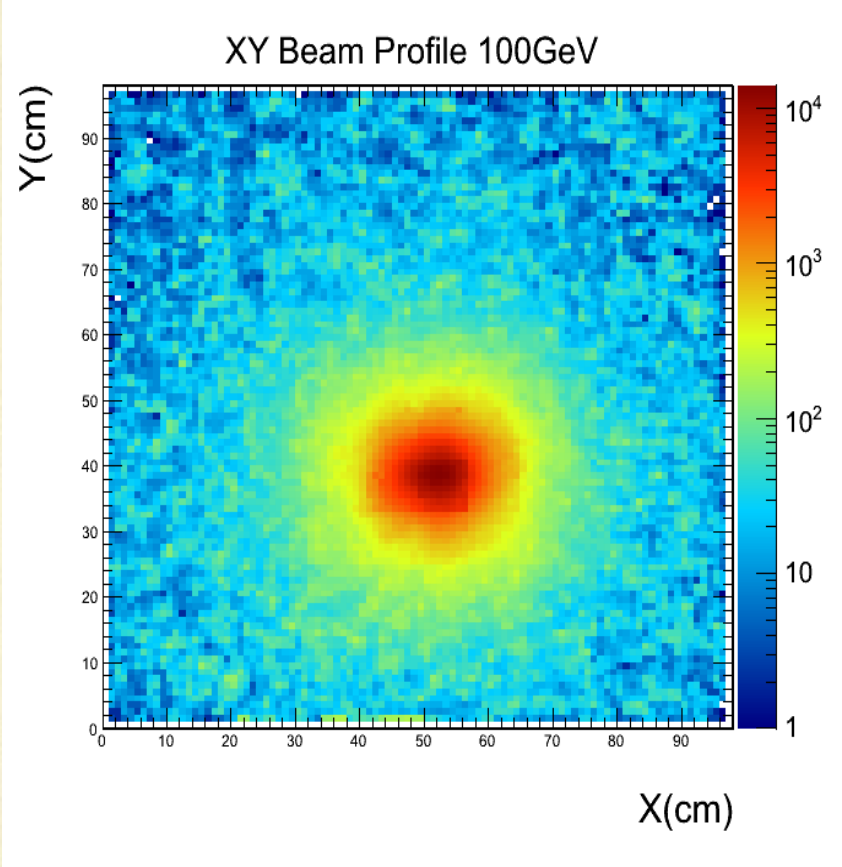




Colours correspond to the three thresholds: Green (100 fC), Blue (5 pC), Red (15 pC)

Raw data, no treatment except time hit clustering




100 GeV pions

# Conclusion and prospects

-The SDHCAL prototype is the first and up-to-now unique **technological** calorimeter prototype. Its success proves that SDHCAL is a serious option for ILD but not only….

-SDHCAL with its fine granularity is an excellent tool to develop and exploit PFA algorithms;

- R&D to validate completely the SDHCAL concept for ILD is ongoing.

-The project has led to several spin-offs (TOMUVOL, CMS,..);

# High rate, fast time precision GRPC for LHC experiments upgrade

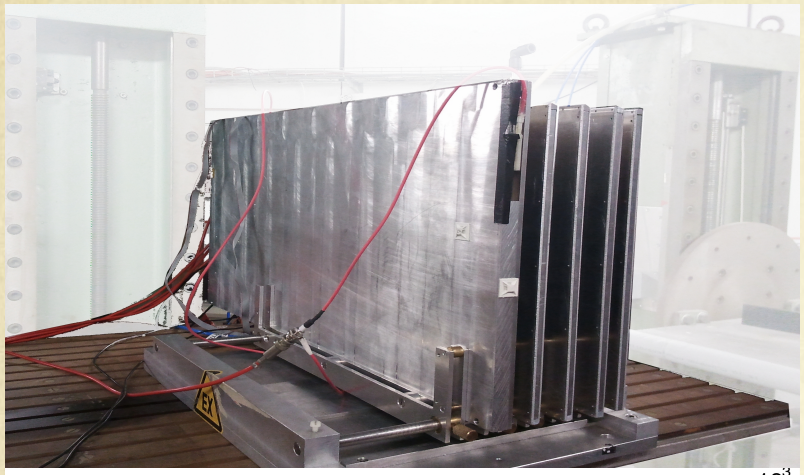
Imad Laktineh

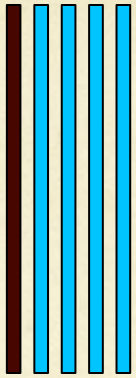
Outline:

- Motivation
- R&D on High Rate GRPC
- R&D on Fast Timing GRPC
- Conclusion

France : IPNL, OMEGA
China : Tsinghua, NCEPU
Italy, Romania....

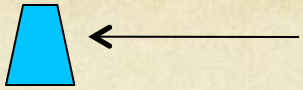
# R&D on high rate RPC





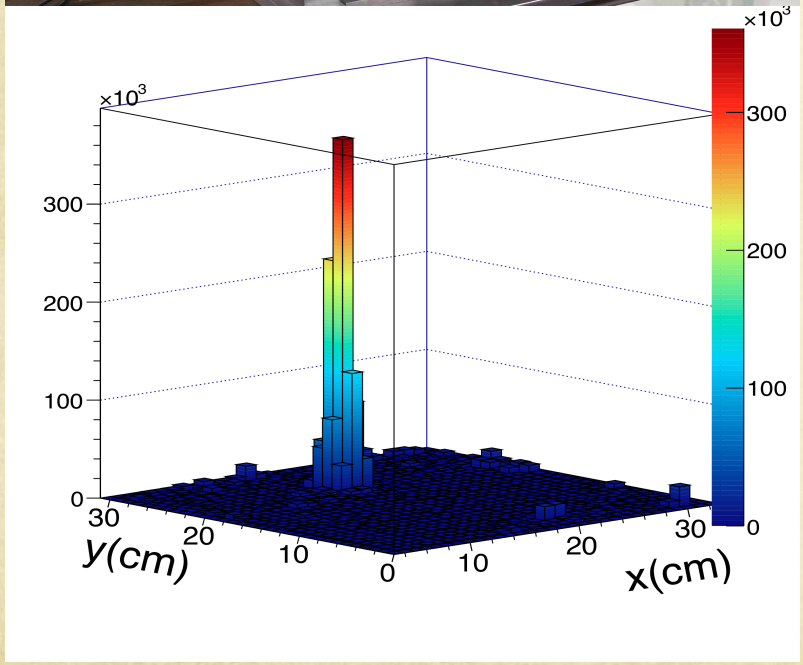
2 Scint-PM

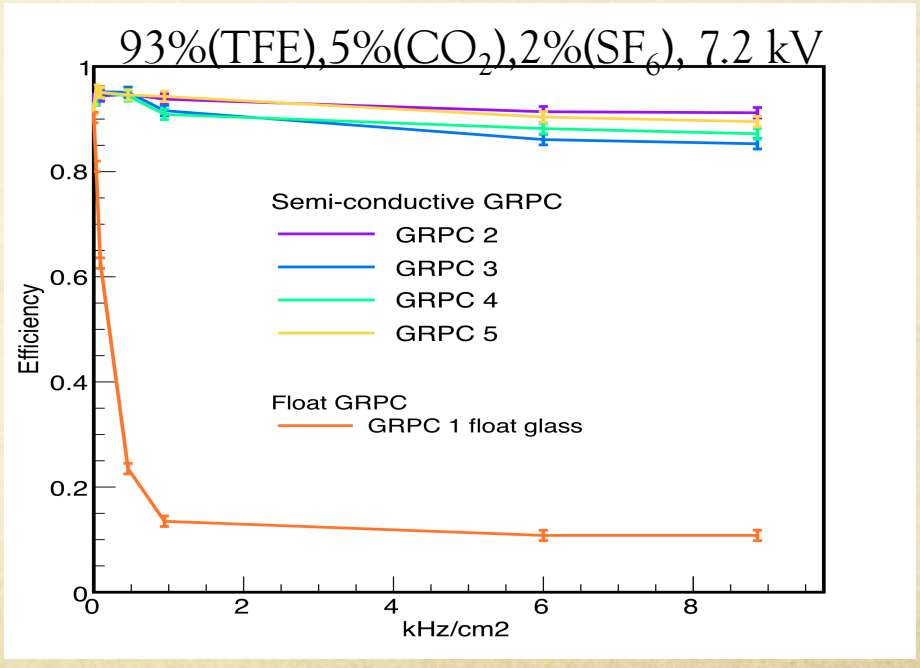
Beam counter
Scint-PM



DESY electron beam

1 standard GRPC+ 4 low-resistivity GRPC



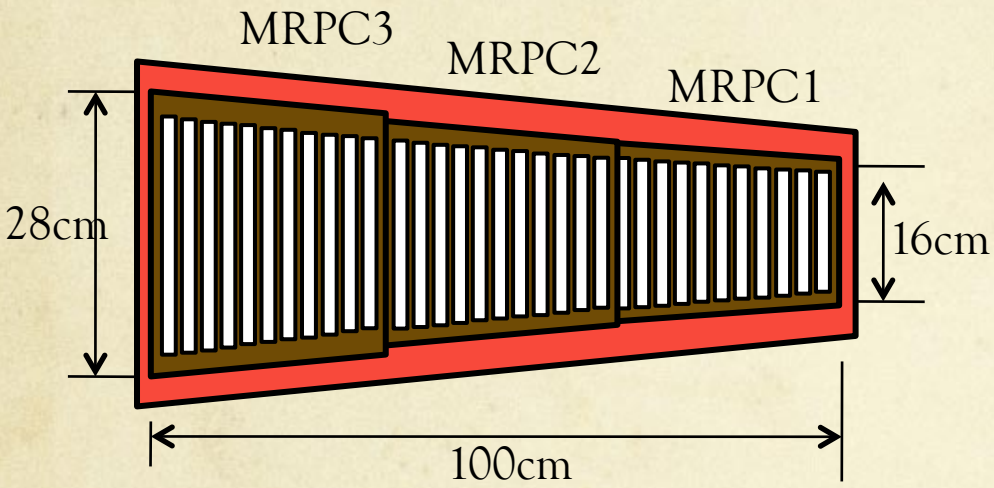



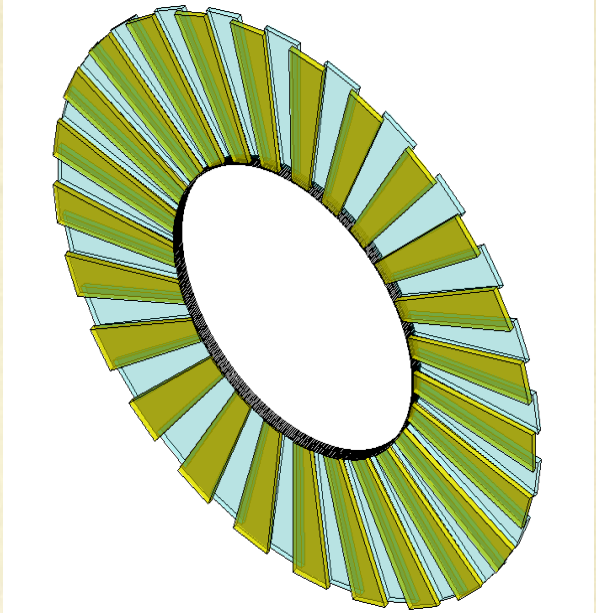

9 kHz/cm$^2$ is highest rate one can get at DESY

# R&D on high rate RPC

- Multi-gap

Tsinghua is working on a new large detector for the SoLID TOF



Main Requirements for TOF:

-Time resolution < 80ps

-Rate capability > 10kHz/cm$^2$

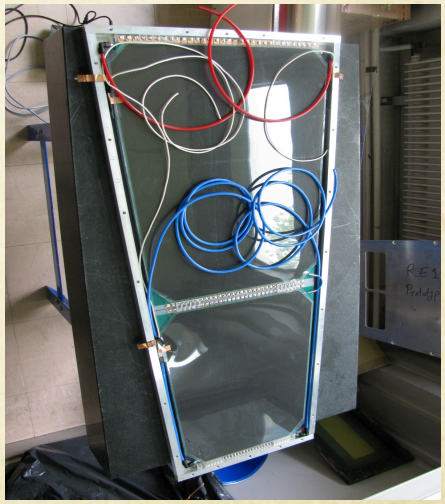
MRPC TOF wall is designed to contain 150 MRPC modules in total, with 50 gas boxes and 3 counters in each box, covering the area of 10m$^2$.

# R&D on high rate RPC for CMS

The small size of the semi-conductive glass is a limitation to build large RPC. However solution do exist: Gluing is one of them





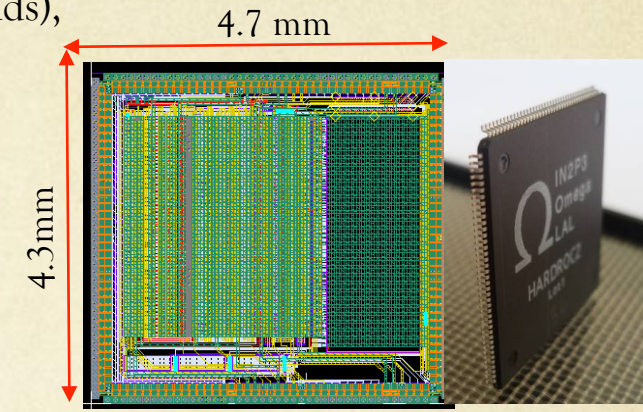



2-gap large chamber a la CMS is built by gluing

# R&D on fast timing RPC

If only 1-2 nanoseconds are needed then the first option is to use

-Use the HARDROC ASICs (well tested and available)
HARDROC : 64-channel, 2-bin readout (three comparators, 3 thresholds),
Dynamic range : 10fC-10pC.




- Use SDHCAL DAQ (available).

- Use a TDC with 100 ps time resolution (available) per ASIC
(use the **U64** available signal for each of the three comparators
as input)
- Design new PCB with pick-up strips (pitch of 2.5 mm)
on the two faces of the PCB with 1 mm staggering between the two faces.
ASICs are embedded on the PCB.

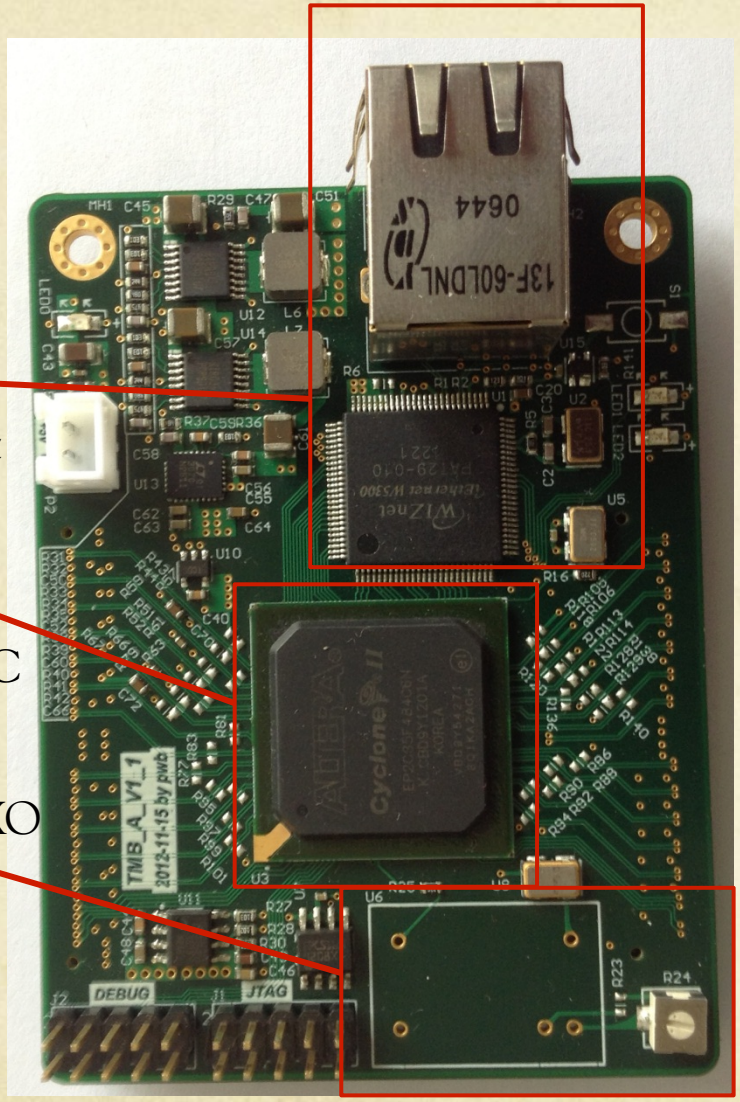
The new PCB can be used to equip the small GRPC already tested or new ones with the same electronics adding an external TDC and then use cosmic rays to check the sub-nanosecond time resolution.

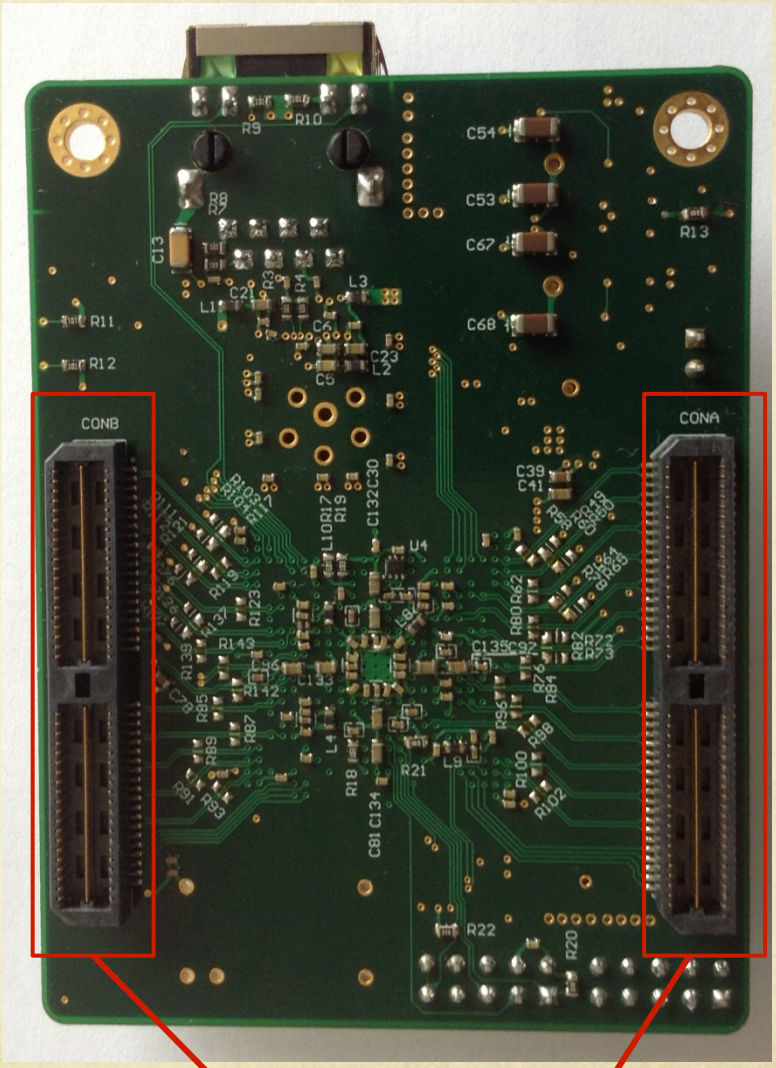
# 24Ch 25ps TDC module

100M Ethernet Readout with TCP/IP support

Cyclone-II FPGA EP2C35F484C6

Socket for TCXO (opt.)




Tsinghua university

Differential input connector

# Conclusion and perspectives

-R&D on high rate and fast timing GRPC is very active.

-High rate capability is demonstrated. Single–gap detectors using Tsinghua low-resistivity glass are still efficient with few kHz/cm2 rate.

-The exploitation of the excellent time precision of the RPC is pursued by developing/exploiting high performance TDC and ASIC. 10-20 ps timing precision seems to be reachable.

-The first aim of this R&D is to check the robustness of the proposal we made to equip the high $\eta$ of CMS with cost-effective muon detectors capable of supporting high rate and providing timing information.

Tsinghua has recently joind CMS collaboration as an associated university

The time precision will allow to exploit fairly the fourth dimension. New area of applications could benefit form this developments: medical application, astroparticles….

# Study of HV CMOS Sensor for the Upgraded ATLAS Tracker in the High Luminosity LHC

## GF Prototype Test Results and TCAD Simulation Studies

FCPPL 2014 — Clermont-Ferrand, France

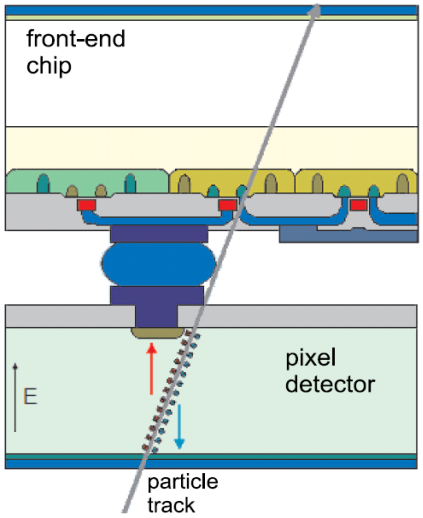
Jian LIU — SDU/CPPM (co-PhD student)

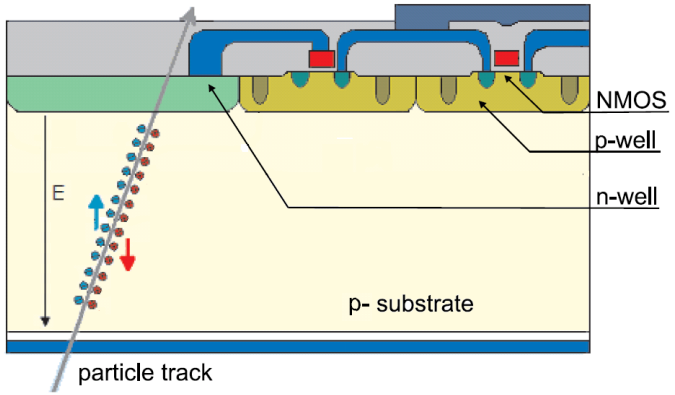
8 April 2014

On behalf of the HV CMOS ATLAS Collaboration

中國科學院高能物理研究所
Institute of High Energy Physics Chinese Academy of Sciences

# From Hybrid to Monolithic




## Hybrid Pixel Detectors Properties:

**fine pitch flip-chip assembly of:**

**CMOS R/O chips (CSA + DSP per pixel)**

**Si (planar or 3D) or Diamond detectors**

**+ high density electronics**

**+ moderate - good SNR**

**- high material budget**

**- high cost (chip + sensor + hybridization)**

## Depleted MAPS for HL-LHC needed:

**large depletion depth d ~$(\rho V)^{1/2}$**

**AND full CMOS**

**AND low power**

**AND low cost**

Questions:

→Radiation hardness (sensor / transistors).

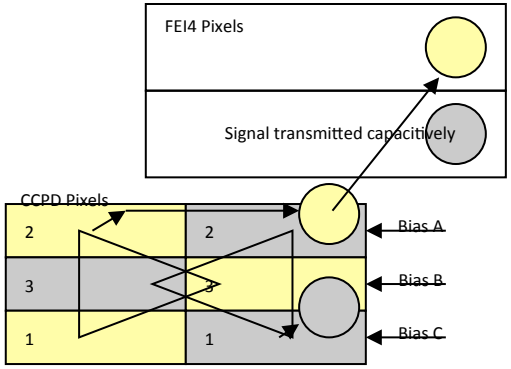
→Signal to Noise Ratio / Efficiency.

courtesy of Bonn University

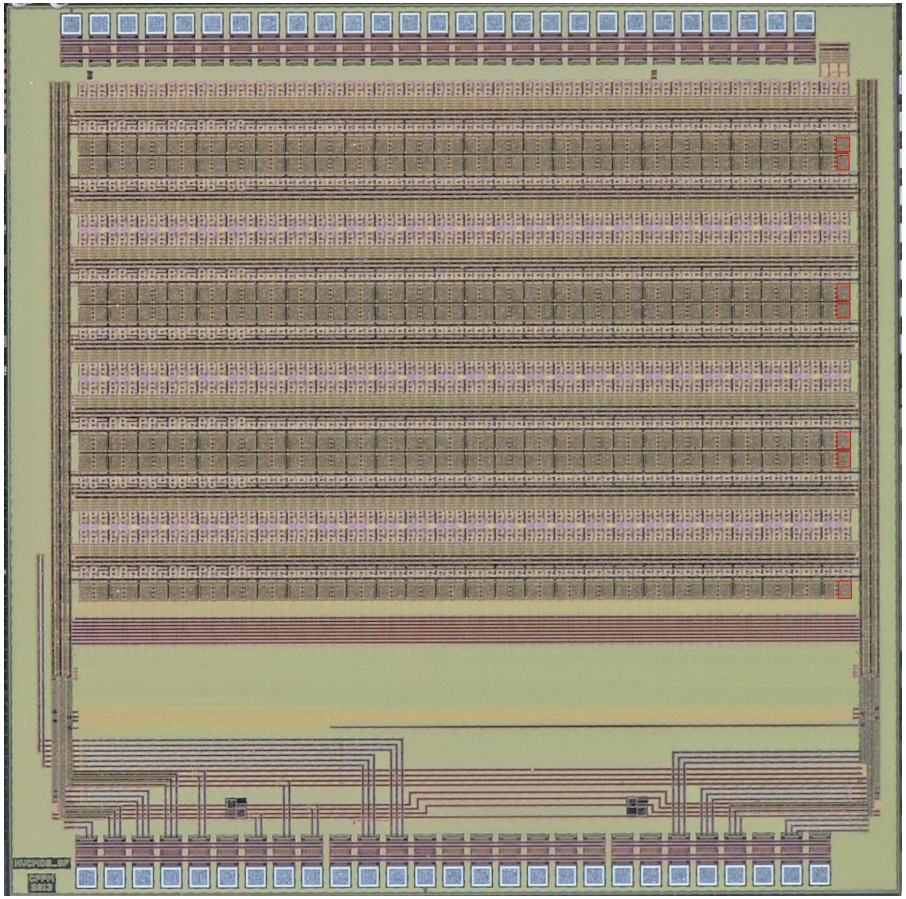
# The HV2FEI4_GF Chip

- The CPPM has submitted (June 2013) a new HV2FEI4 version in GlobalFoundries 0.13µm BCDLite technology. The HV2FEI4 GF version is a 26 columns and 14 rows matrix pixels.

- The HV CMOS sensor pixels are smaller than the standard ATLAS pixels, in our case 33µm x 125µm - so that three such pixels cover the area of the original pixel.




- The pixel chain contains charge sensitive amplifier, comparator and tune DAC.
- The HV2FEI4_GF chip contains additional test structures
  - Linear and ELT transistors (short and narrow channels).
  - Pixel behavior



# Conclusion and Perspective

- After 1GRad X ray irradiation, the Global Foundries 130nm BCDlite chip still works well with degraded functions.
- Transistor test shows good radiation tolerance. Positive sign to use this technology in a high radiation environment à la Phase II upgrade.
- HV2FEI4_GF gluing on FEI4 has finished. Test will start very soon.
- Porting to LF 150nm technology is ongoing (HR substrate).

- By TCAD simulation, ~77% p-region between pixels is un-depleted, which will reduce the fill factor and efficiency!! Alternative approach→ Normal 130nm LP Process with HR substrate.
- Both NIEL and TID effects and Transient TCAD simulation is necessary. Continue to perform some specific simulations.

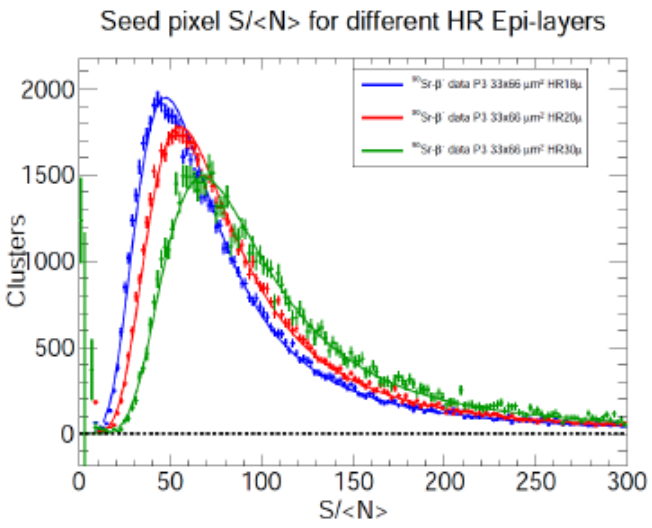
# R&D on inner-tracking at BESIII with CMOS Pixel Sensors

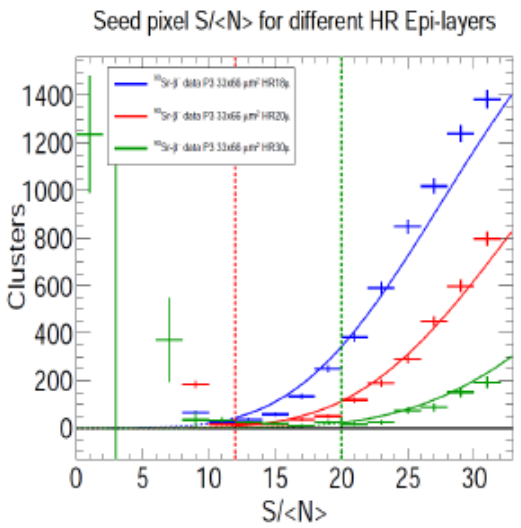
WANG Meng (王萌, Shandong Univ.)

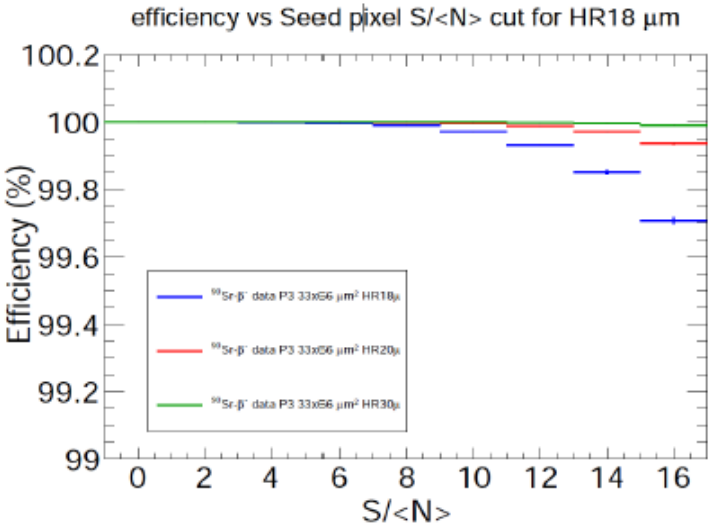
*7th FCPPL Workshop, Clermont-Ferrand, 2014.4.8*

# 33 × 66 µm² pixels: SNR & $\varepsilon_{det}$

- **33×66 $\mu m^2$ pixels :** SNR & $\varepsilon_{det}$ obs. with $\beta^-$ ($^{90}$Sr) for HR-18, HR-20 & HR-30



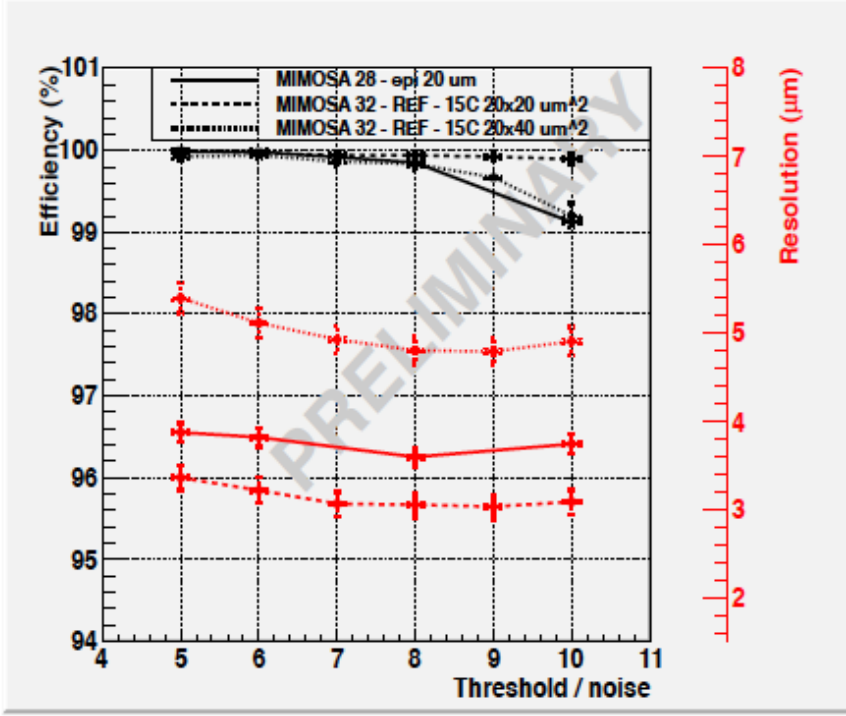




- **Conclusions on the 33×66 $\mu m^2$ pixels :**
  - A single 8 $\mu m^2$ diode within 15 $\mu m^2$ footprint provides high SNR despite the large pixel (≡ low sensing node density)
  - The HR-30 epitaxial layer leads to SNR ∼ 70 (MPV) for $^{90}$Sr $\beta^-$ rays

⇛ **Safe to assume that 30×63/70 $\mu m^2$ pixels with in-pixel circuitry will be performing well (tbc)**

# 33 × 66 μm² pixels: spatial resolution

- **Beam test (analog) data used to simulate binary charge encoding :**
  - ✳ Apply common SNR cut on all pixels using <N>
    ↪ simulate effect of final sensor discriminators
  - ✳ Evaluate single point resolution (charge sharing) and detection efficiency vs *discriminator threshold* for 20x20; 22x33; 20x40; 22x66 $\mu m^2$ pixels




- **Comparison of 0.18 $\mu m$ technology ($> 1\ k\Omega \cdot cm$) with 0.35 $\mu m$ technology ($\lesssim 1\ k\Omega \cdot cm$)**

| **Process** ▷ | 0.35 $\mu m$ | 0.18 $\mu m$ | | | | |
|---|---|---|---|---|---|---|
| **Pixel Dim.** [$\mu m^2$] | 20.7×20.7 | 20×20 | 22×33 | 20×40 | 22×66 | 33×66 |
| $\sigma_{sp}^{bin}[\mu m]$ | 3.7 ± 0.1 | 3.2 ± 0.1 | ∼ 5 | 5.4 ± 0.1 | ∼ 7 | ∼ 10 $\mu m$ ? |

# summary & outlook

- IHEP-SDU-IPHC partnership has been active in adapting CPS for BESIII inner tracking.
- The PICSEL group at IPHC has demonstrated that large pixels can achieve excellent detection efficiency (33 × 66 $\mu m^2$) and very good spatial resolution (~7 µm for 22 × 66 $\mu m^2$).
- Progress has been made in prototype design, electronics and simulation.

- milestones in plan
  - 2014.12 ladder assembly study
  - 2015.4 first ladder
  - 2016.5 prototype construction

# Electronics in TUNE

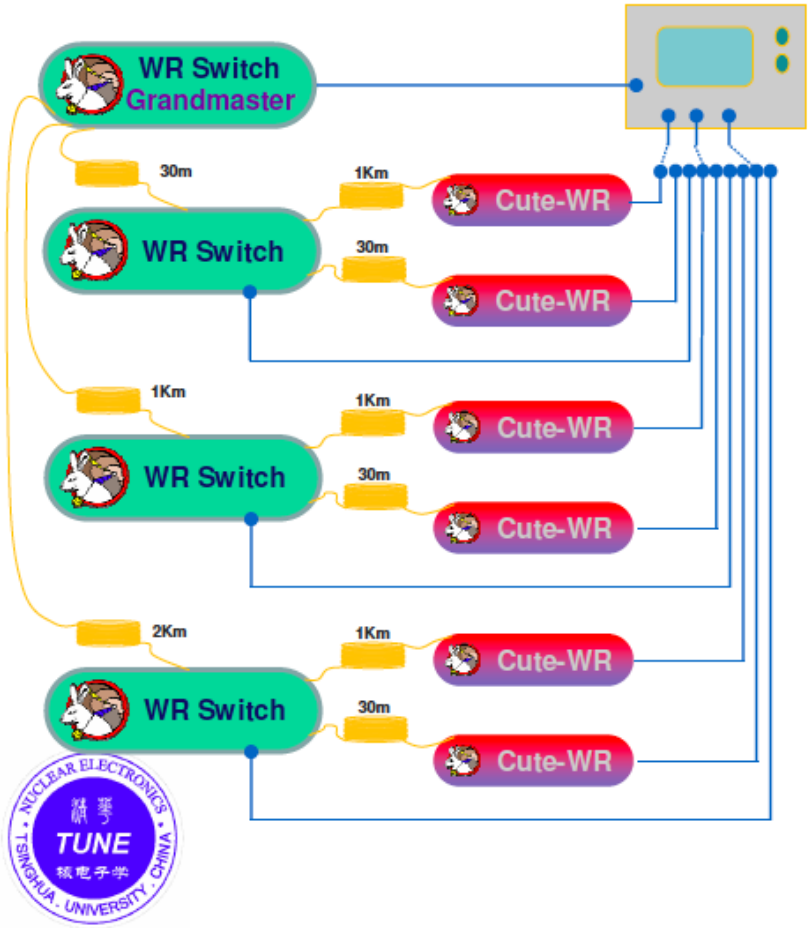
## - ASIC and WR

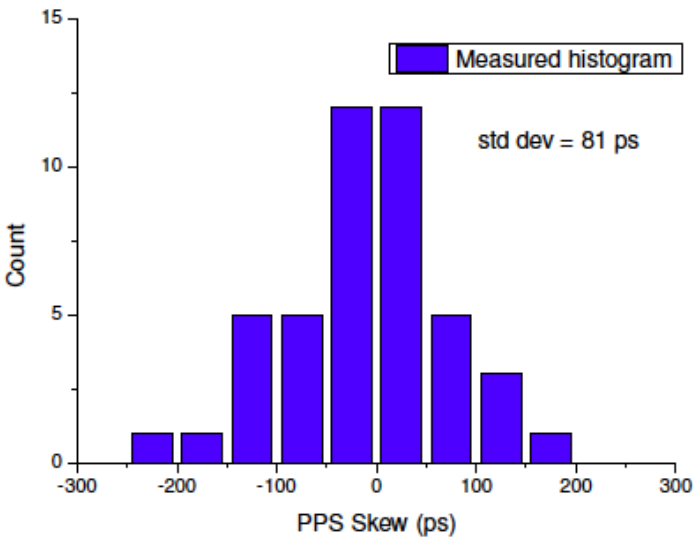
Prof. Yinong Liu
Department of Engineering Physics
Tsinghua University, Beijing, China

2014.4

- TUNE – Tsinghua Univ. Nuclear Electronics
- ASIC
  - low noise pre-amp.
  - CASAGEM, CAPS, PPC-HPGe, CAD (for MRPC), TIMPIC, SCA (Switch Capacitor Array)
- WR – White Rabbit
  - ethernet based, sub-ns time distribution network
  - LHAASO

# WR performance (@Tsinghua)




**Parallel topoloty**

# FRONT-END ELECTRONICS BASED ON PARISROC ASIC FOR THE LHAASO EXPERIMENT

Yingtao CHEN, IPNO, France/YNU, China

For 7th France China Particle Physics Laboratory (FCPPL) Workshop
Clermont-Ferrand, France April 8th-10th

# Wide Field of view Cherenkov/Fluorescence Telescope Array (WFCTA)

**Telescopes**

- The angular resolution: *< 0.4°*
- The energy resolution: *< 20%*
- The resolution of the location of shower maximum: *< 40 g/cm²*
- The Field of View (FOV) of a single telescope: *14° X 16°*
- Dynamic range: *3 orders of magnitude of the energy*
- Movable design for different purposes
- 24 identical telescopes divided into 3 groups with a distance of 100 m

**Electronics**

- Signal polarity: *Negative or positive*
- Dynamic range: *160 fC to 240 pC*
- Nonlinearity: *< 2%*
- Charge resolution: *< 20% @160 fC and <5% @ 240 pC*
- Time resolution: *20 ns (RMS)*
- Single channel event rate: *10 kHz*
- Signal width: *6 ns to 50 ns (Cherenkov)*
- Pedestal monitoring: *Sky and electronics*
- Channels: *1024 per telescope*
- Power consumption: *260 W*

Prototypes in YBJ, Tibet

*Technology: 0.35μm SiGe AMS*

## Photomultiplier ARray Integrated in SiGe ReadOut Chip

PARISROC 2 is designed by OMEGA Group

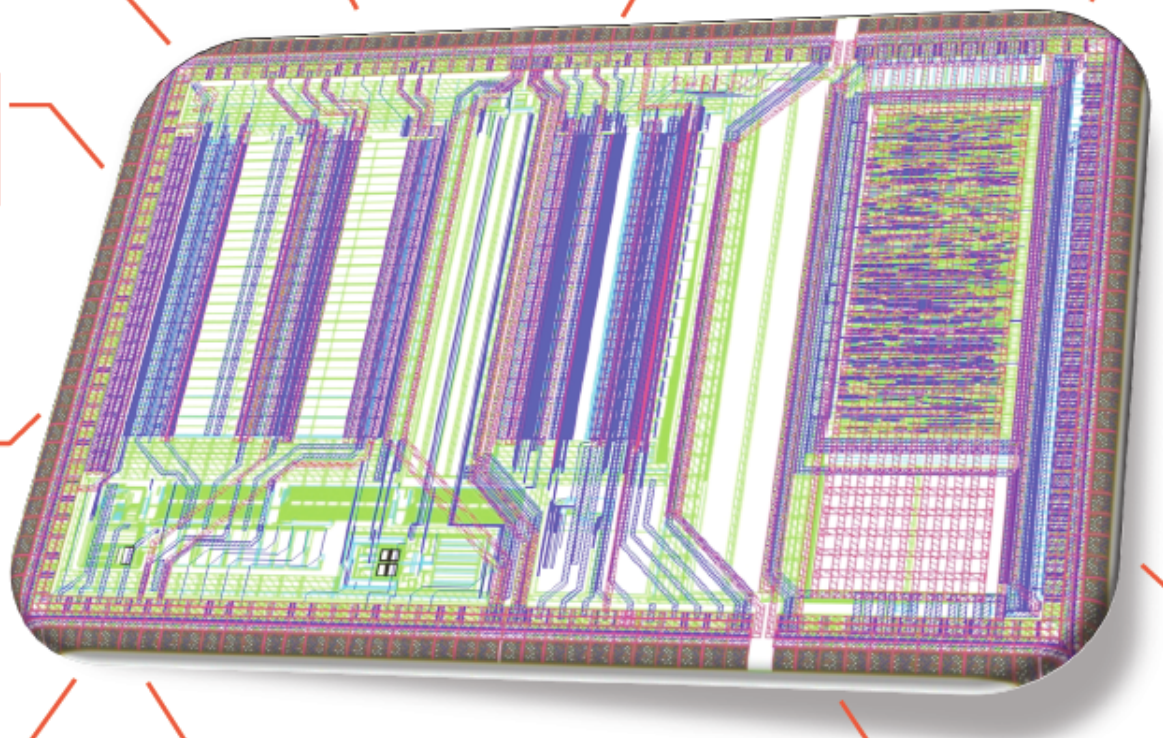
**Dual-gain Preamplifiers**

**Time measurement: tagging < 1 ns**

**16 Channels (neg.)**

**10 bit ADC internal conversion**

**TQFP160 5 mm X 3.4 mm**



A very complex SoC designed for multiple purposes and experiments

**Input range -0.8 V to 4.1 V**

**278 slow control parameters**

**Auto-trigger design**

**Charge measurement: 50 fC ~ 100 pC**

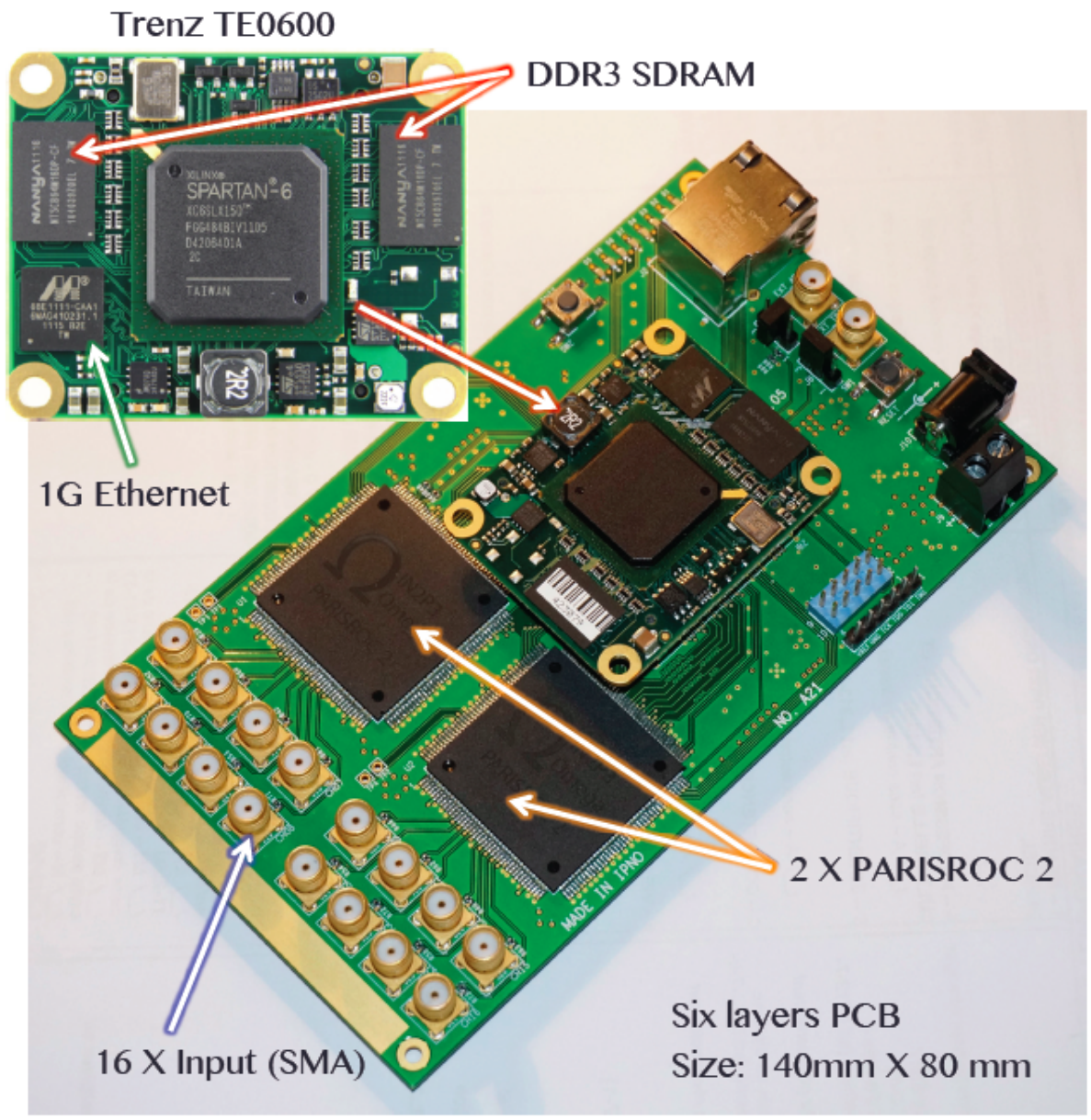
**15 mW / channel**

S. Conforti Di Lorenzo et al., NIM A 2009.05.135, arXiv:0811.2681.

# Picture of the FEE

## Trenz TE0600-01

- Spartan-6 LX150: 147K
- Size: **50 mm × 40 mm**
- **10M/100M/1000M Ethernet**
- 2 x 16-bit 256MB DDR3 SDRAM
- 128Mb (16 MB) SPI Flash
- Robust board-to-board connectors (B2B) LSHM up to 10 GHz / 20 Gbps
- Up to 52 differential I/O
- Up to 109 single-ended I/O



# Conclusions

- The ASICs are adapted for experiments like LHAASO at high altitude.
- The performances of the PARISROC 2 has been studied for WFCTA in Cherenkov mode.
  - Signal duration
  - Dynamic range
  - Nonlinearity
  - Event rate
  - Pedestal monitoring
- New FEE based on PARISROC 2 has been designed and tested.
- OMEGA plans to upgrade PARISROC this year.
  - Tests of the current FEE should be completed before May 2014.

# Summary on Summaries

- The collaboration in detector R&D is active, even extending towards education.
- Most of collaborations, as I know, have been formed with FCPPL.
- FCPPL provides an excellent framework of cooperation.
- We should KEEP MOVING.