Electronics in TUNE

- ASIC and WR

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The Laboratory

- TUNE – The Laboratory of Nuclear Electronics at Tsinghua University, Beijing, China
- Chinese “T清华U大学N核E电子学”

- Established since 1956

Education

- Courses
  - Nuclear Electronics
  - Nuclear Instrumentation
  - Electro-Magnetic Compatibility
  - Embedding System
  - Real-time operation system μCOS

Education

- Student Exercise
  - Preamp, Noise measurements
  - Pulse Shaping , Pulse Height Analyzer
  - Discriminator, Time
  - μC, FPGA
  - ARM freescale University program

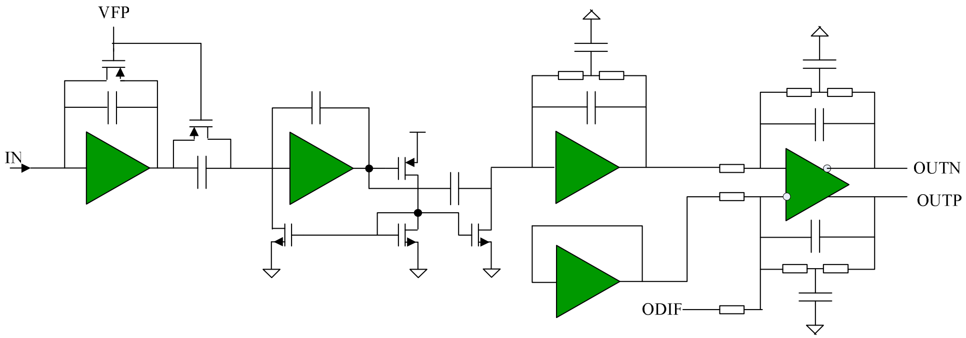
Research

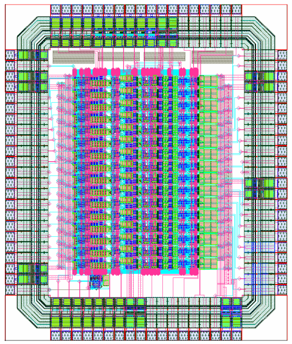
- Analog
  - ASIC – low noise amplifier
  - …
- Digital
  - WR – Ethernet based, sub-nanosecond time distribution network
  - …

ASIC – low noise

- Low noise preamplifiers
- CMOS MPW 0.6→0.35→0.18μm
- GEM, CZT, point contact HPGe
- Zhi Deng, Associate Professor

CASAGEM

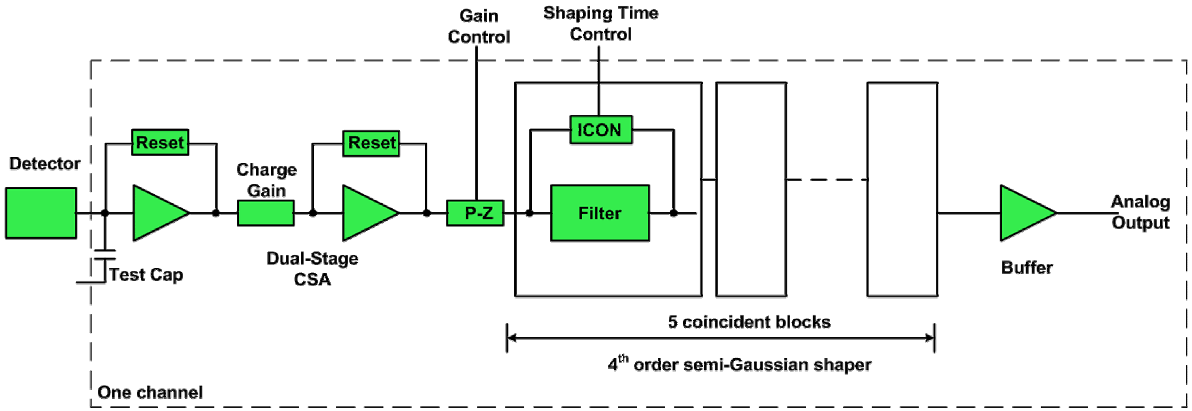


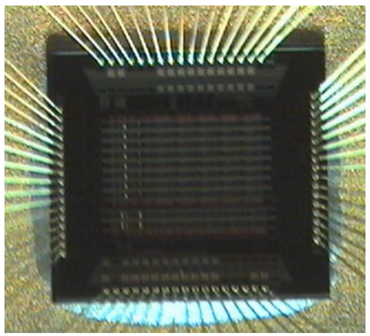


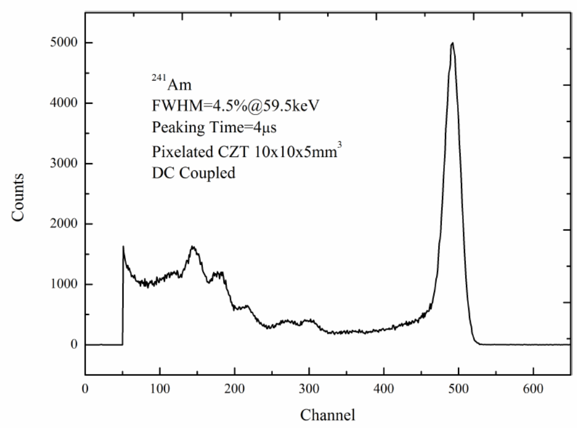
	CASA	PASA	LEGS-TPC	PCA
Noise	293-455e@7.7pF	560e@12pF	100e+25e/pF	270e@10pF
Gain	1-19mV/fC	12mV/fC	17-32mV/fC	9.5mV/fC
Pulse Width	100-400ns, peak	188ns, FWHM	600ns, peak	100ns, FWHM
Crosstalk	<0.98%	<0.1%	unknown	0.3%
Power	8.9mW/ch	11mW/ch	1.25mW/ch	10mW/ch
Process	0.35μm	0.35μm	0.25μm	0.13μm

CAPS

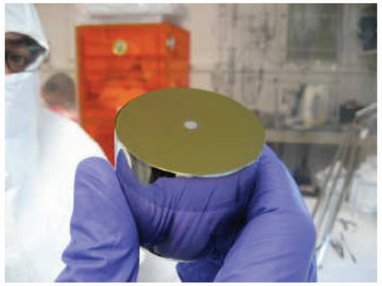
CZT, CSA, shaper



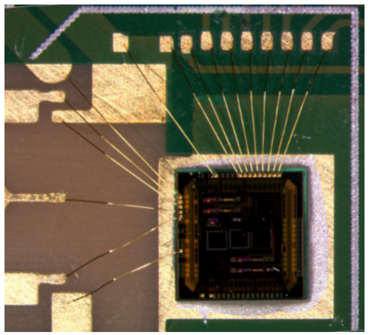


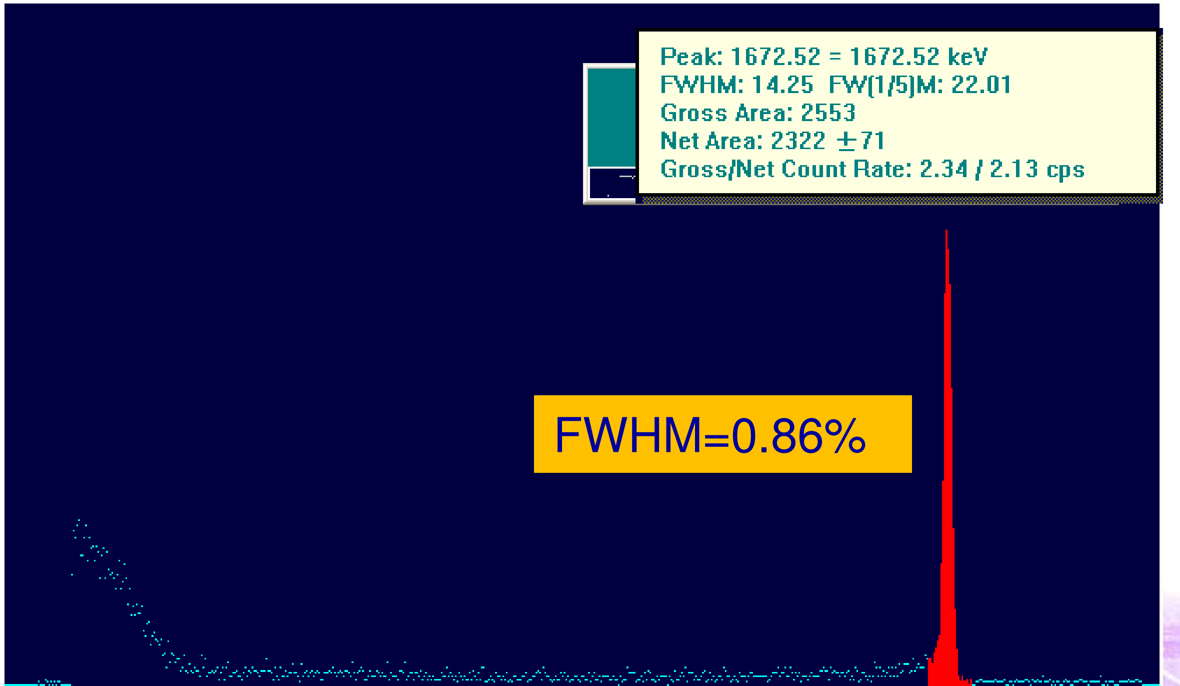


PPC-HPGe



~1pF capacitance

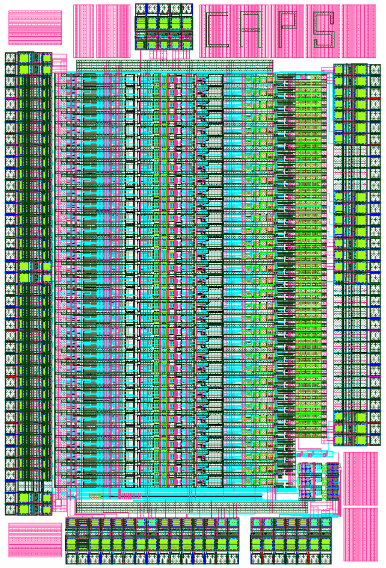


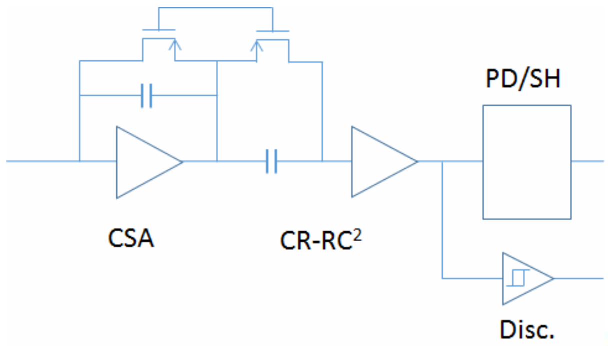


Am-241 Spectrum (Cd~3pF, Id=23pA)

CAPS

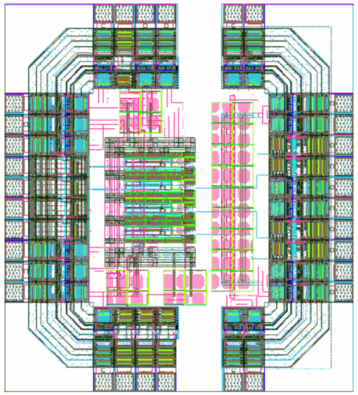
32 channels, CZT, CR-(RC)^2 shaper, discriminator, peak detection/holding, serial output

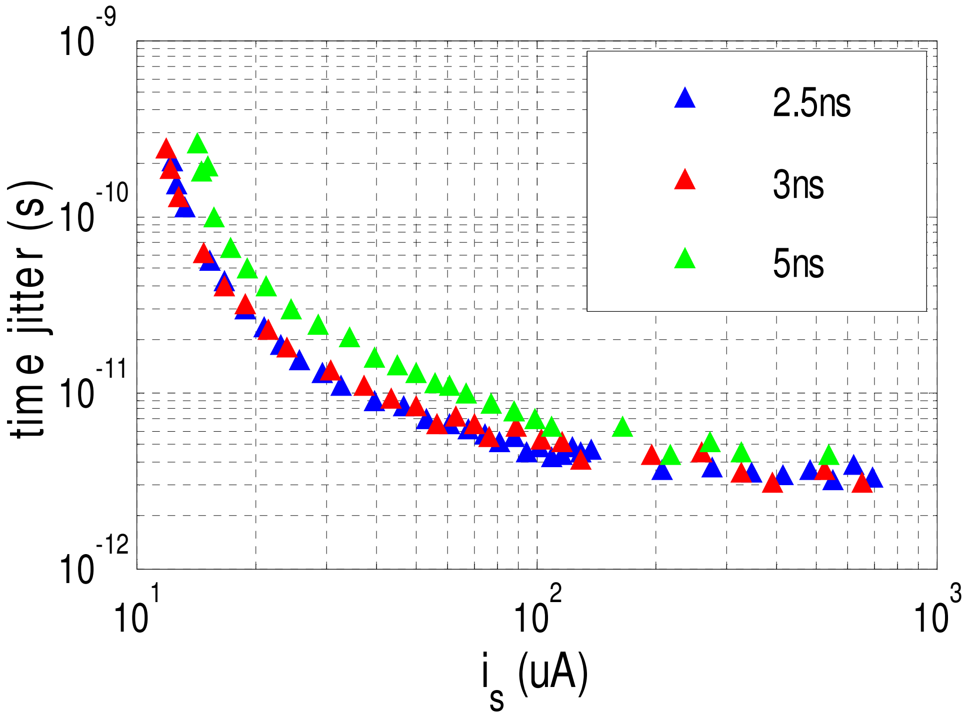




CAD

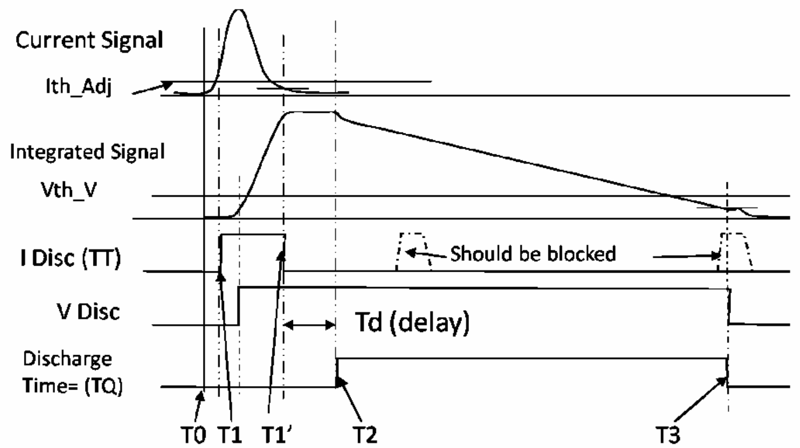
4 channels current amplifier and discriminator
jitter < 10 ps (i > 20 μA), for MRPC

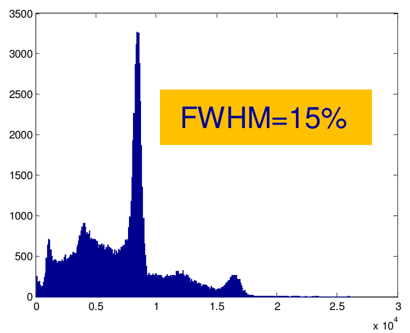




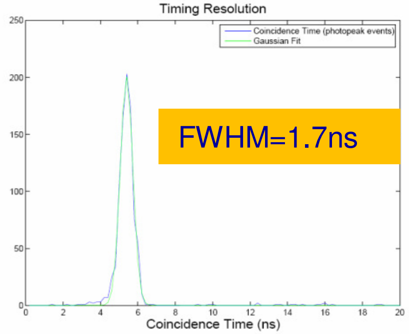
TIMPIC

16 channels, SiPM read out
time and amplitude TDC reading

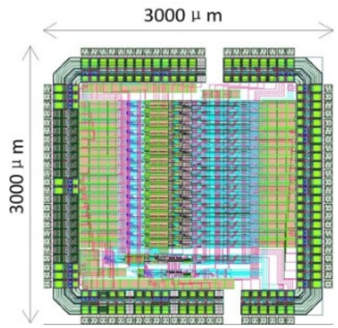




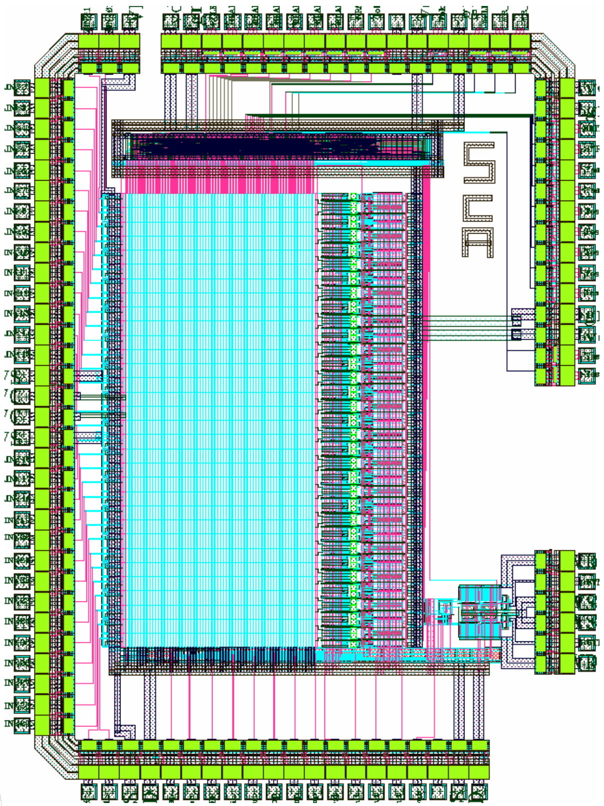
Na-22 spectrum with LYSO



CTR with LYSO

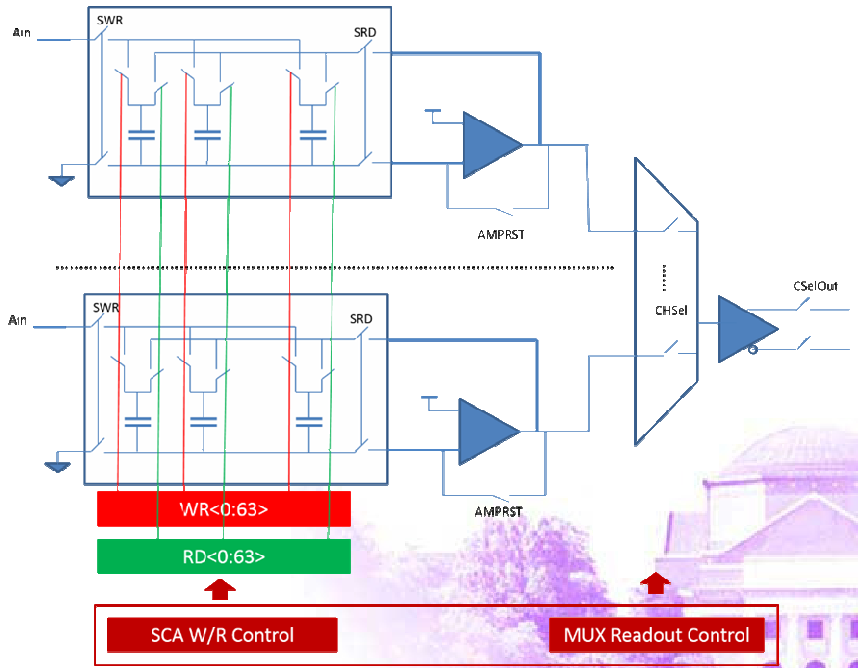


SCA



32 channels

Switch Capacitor Array

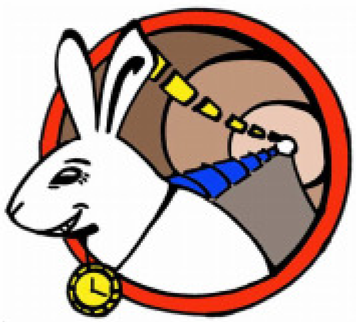


White Rabbit

- WR - White Rabbit
- Ethernet based, sub-nanosecond time distribution network
- Guanghua Gong, Associate Professor

White Rabbit

- Main features
  - Transparent, high-accuracy synchronization
  - Low-latency, deterministic data delivery
  - Designed for high reliability
- Accelerator's control and timing
- International Collaboration
- Based on Well-known technologies

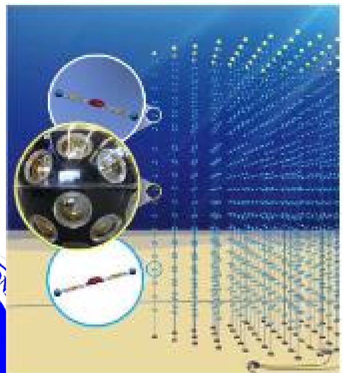


J. Serrano, et al., *The White Rabbit Project*, ICALEPCS, 2009

Applications of WR

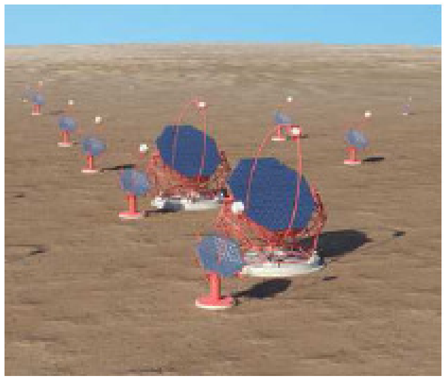
CERN Neutrinos to Gran-Sasso

Existing



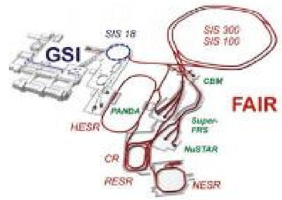
KM3NET

potential



CTA

LHC



GSI

Future

LHAASO

WR – sub-ns synchronization

Long distance： 10km
Multi Nodes ： 2000~10000
Accuracy ： <1ns
Precision ： 10ps

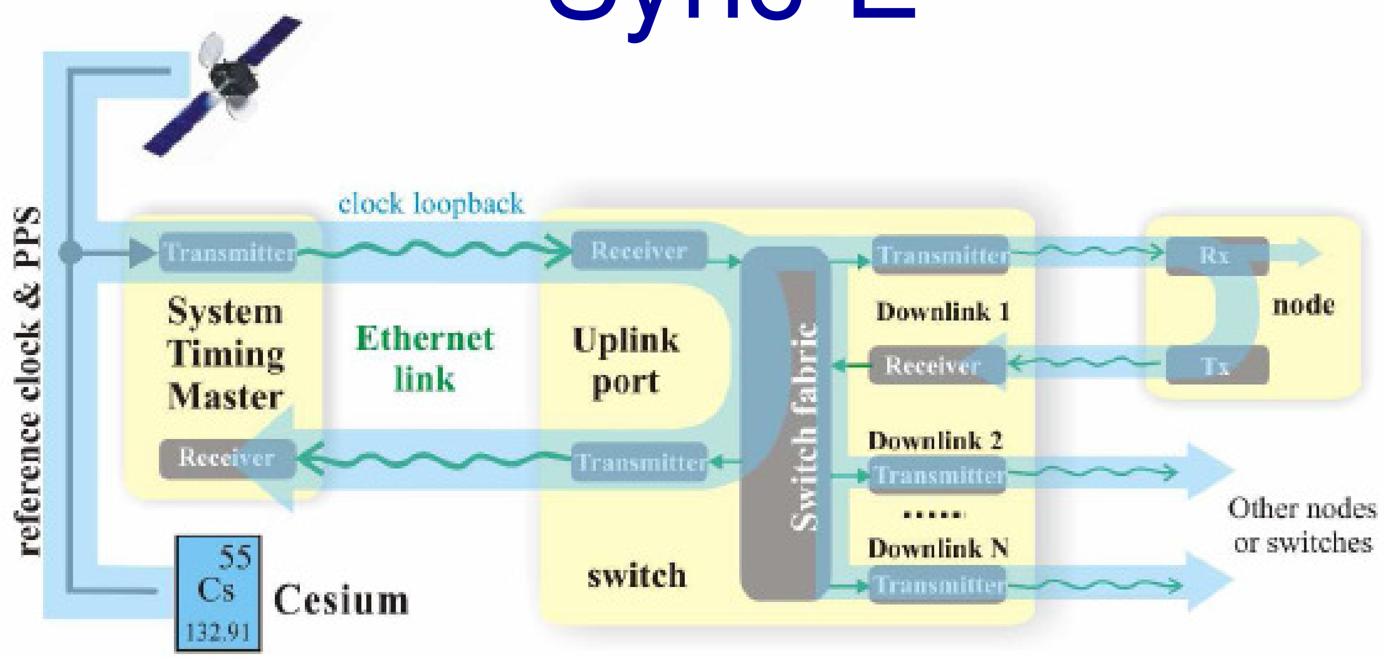
PTPv2 — Packet-based protocol — **Timestamp Synchronization**

Sync-E — Clock/Data encoder/recover — **frequency lock**

DMTD — Dual mixer time difference — **Phase alignment**

NUCLEAR ELECTRONICS · TSINGHUA · UNIVERSITY · CHINA
清华 TUNE 核电子学

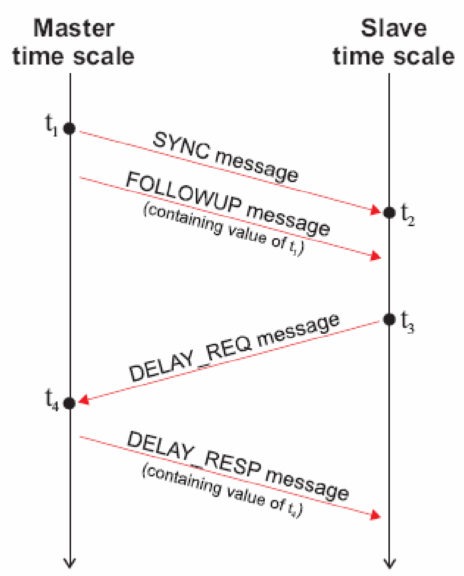
Sync-E



- Common clock for the entire network
  - All devices use the same physical layer clock
  - Clock encoded in the Ethernet carrier
  - Recovered by the receiver chip
  - Not affected by network traffic load

frequency lock

Precision Time Protocol (IEEE1588)



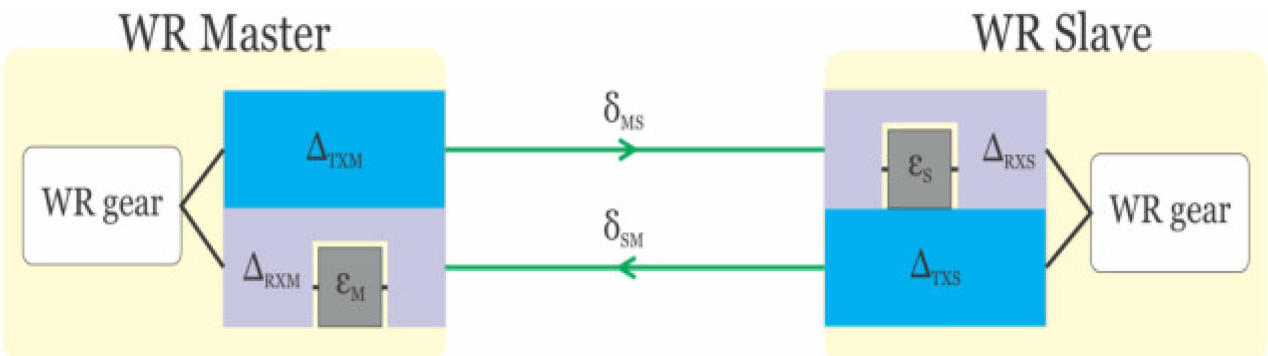
Having values of $t_1 \ldots t_4$, slave can:

- calculate one-way link delay:
  $\delta_{ms} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$
- syntonize its clock rate with the master by tracking the value of $t_2 - t_1$
- compute clock offset:
  $offset = t_2 - t_1 + \delta_{ms}$

Timestamp Synchronization

- Precision time protocol(IEEE1588-2008)
  - Targeted for LXI (LAN-based eXtensions for Instrumentation) application.
- Exchange of packages with timestamp embedded
- delay and offset are calculated and compensated.
  - ~100ns precision achieved

WR Asymmetric link model



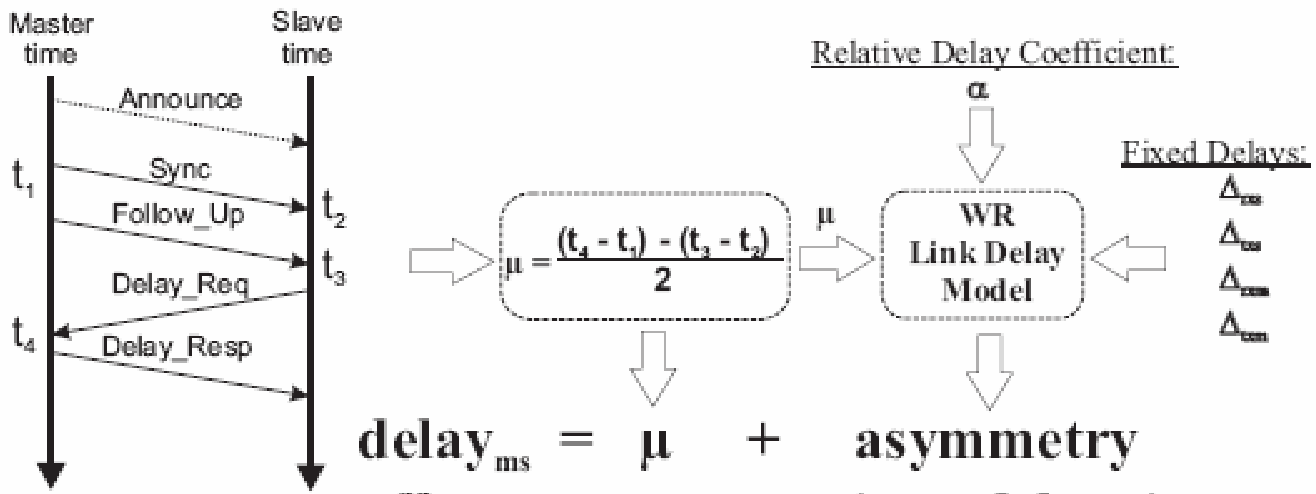
- Link delay
  - Propagation speed difference due to WDM

Fiber calibration

- Fixed delay
  - PCB layout delay
  - Pin-to-Reg delay inside FPGA
  - Fiber driver/Receiver delay

Node calibration

WR Asymmetric link model



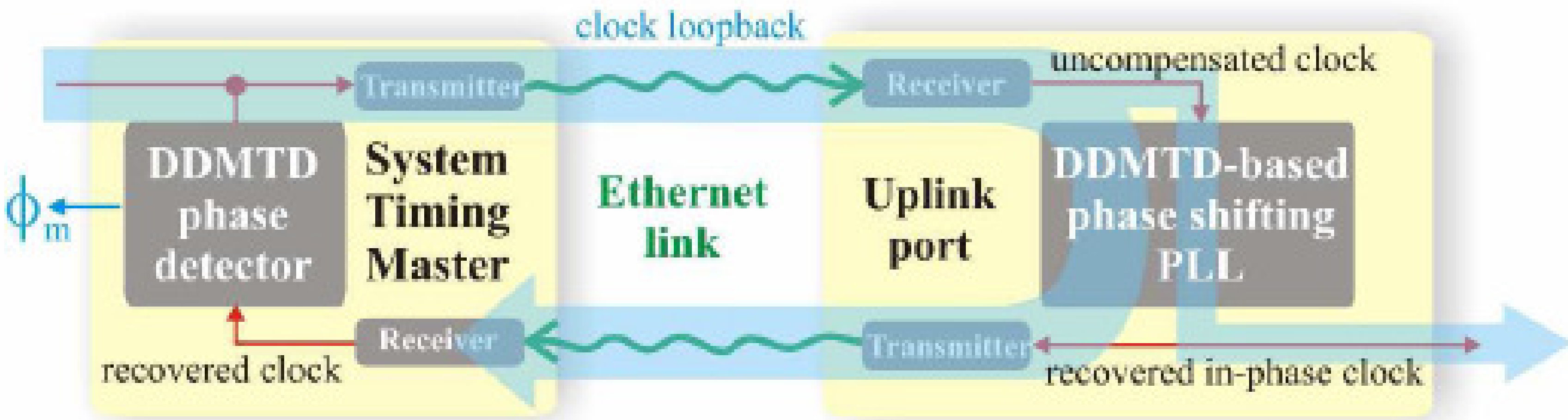
$$delay_{ms} = \mu + asymmetry$$

$$offset_{ms} = t_2 - (t_1 + delay_{ms})$$

Solution for Ethernet over a Single-mode Optical Fiber

$$asymmetry = \Delta_{tx_m} + \Delta_{rx_s} - \frac{\Delta - \alpha\mu + \alpha\Delta}{2 + \alpha}$$

DMTD



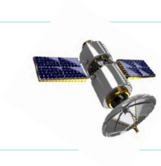
- PTP limitation
  - Clock-cycle granularity (8ns for 125MHz)
- Take advantage of SyncE and measure phase shift
  - tx/loopback clock phase shift measured at master side
  - Recovered clock adjusted by PLL at slave side
- Phase tracking by DDMTD
  - Dual Mixer Time Difference
  - Digital implementation: linear, low cost, resource saving

Phase alignment

WR components

A White Rabbit network is composed of

Clock/Freq reference (optional)



GPS

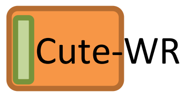
Ru/Cs

WR switch

Fiber links/cables

WR nodes

IP core



WR Switch

by Seven Solutions

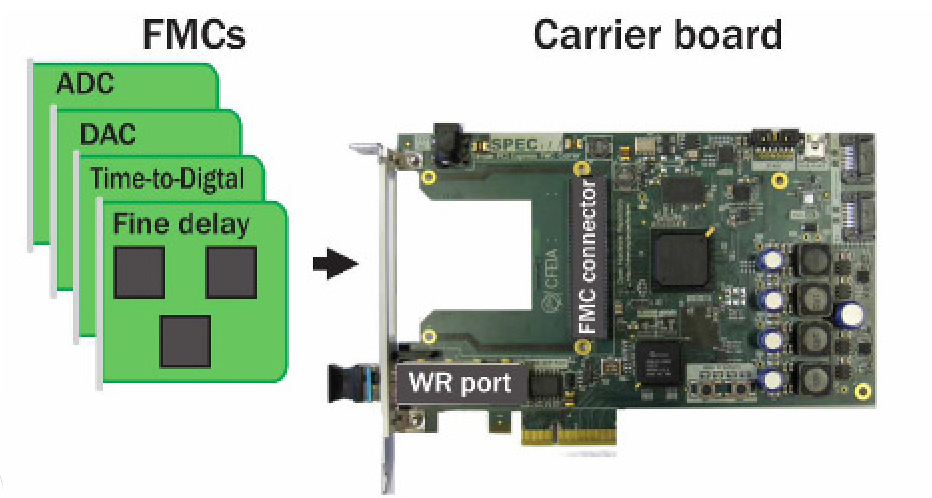
- Xilinx Virtex 6, Atmel AT91SAM9G45
- 18 cages for Gigabit SFPs, 10/100 Ethernet management port
- 5 SMC connectors (1-PPS in/out, CLK in/out)
- designed and produced by *Seven Solutions* in cooperation with CERN
- schematics, PCB design and mechanical drawings in the public OpenHardware repository

- Central element of WR network
- Original design optimized for timing, designed from scratch
- 18 1000BASE-BX10 ports
- Capable of driving 10 km of SM fiber
- Open design (H/W and S/W)

WR Node: carrier boards

- PCI-Express/VME/PXI/uTCA form carrier boards:
  - Logic/Memory/Process
  - WR circuit/SPF-Port/WRPC
  - FMC mezzanine connectors
- AD/DA/IO with FMC mezzanine cards

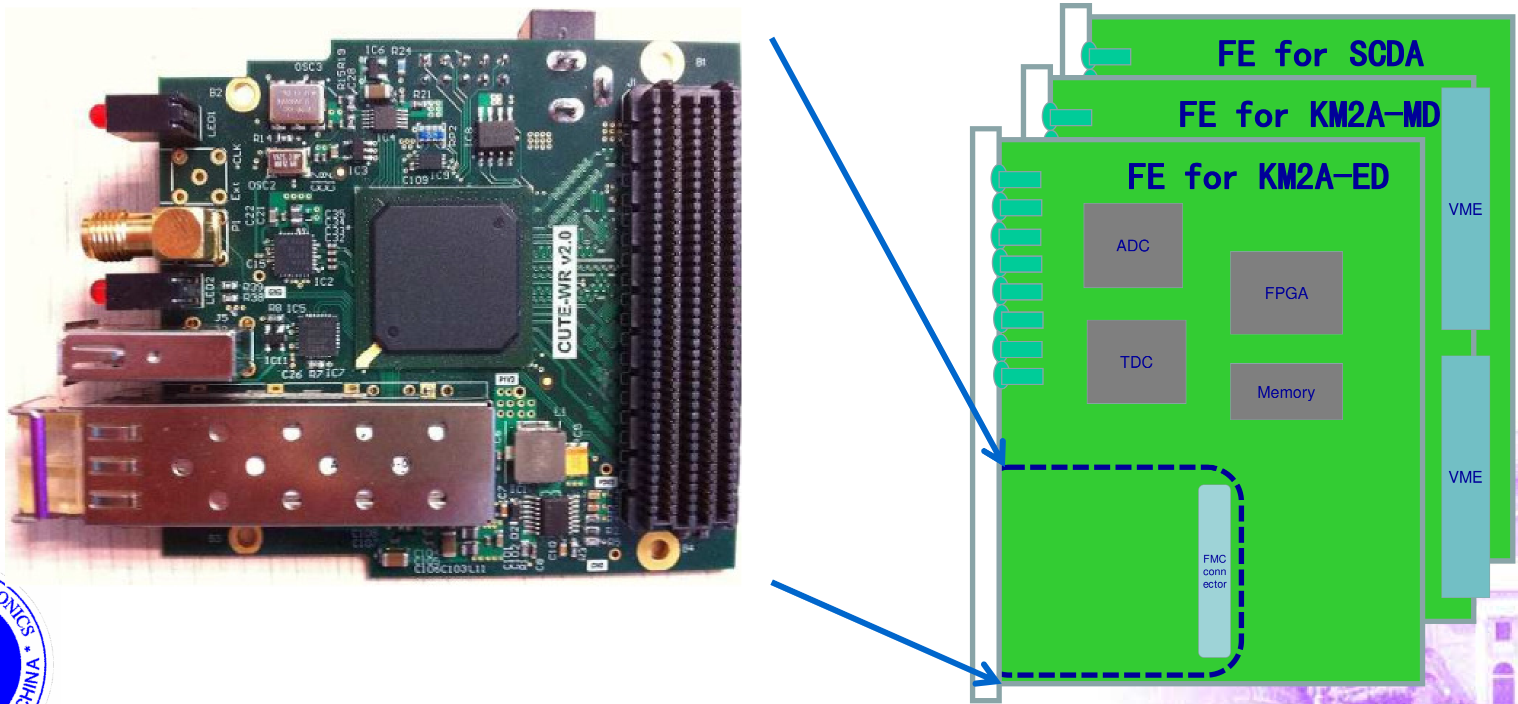
Application mode for CERN/GSI



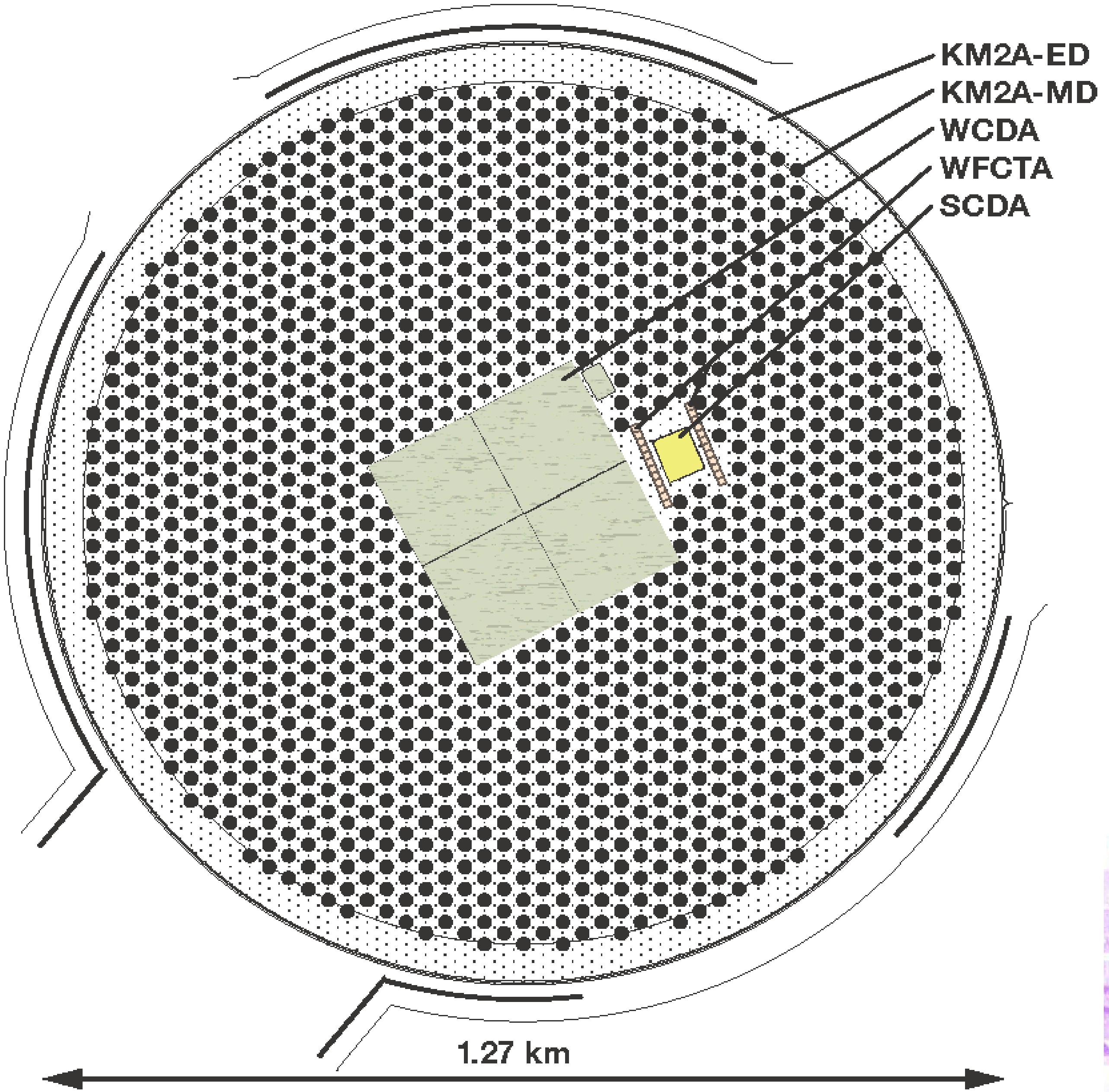
WR Nodes: Cute-WR

- FMC form WR mezzanine
  - WR circuit/SFP-Port/WRPC
  - FMC mezzanine connector

Application mode for LHAASO

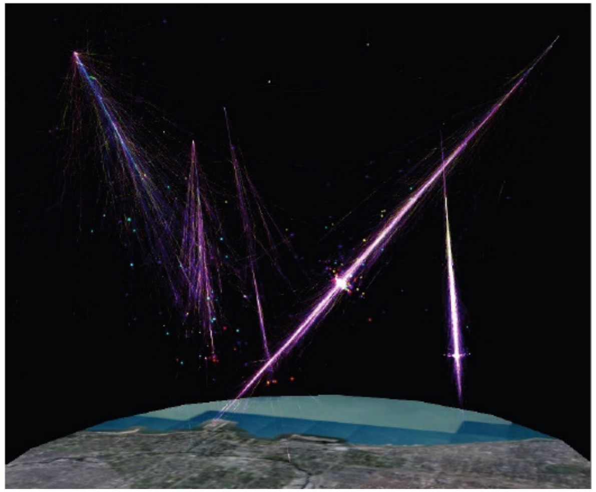


Large High Altitude Air Shower Observatory



LHAASO detector

- KM2A：
  - 5632 Electron detector, 15m spacing
  - 1221 μ detector, 30m spacing
- WCDA： ***W***ater ***C***herenkov ***D***etector ***A***rray
  - 4 x (150 × 150) m^2
  - 3600 detector units
- WFCTA： ***W***ide ***F***OV ***C***herenkov ***T***elescope ***A***rray
  - 24, 300m spacing
- SCDA： ***S***hower ***C***ore ***D***etector ***A***rray
  - 5000m^2, 452 core detectors



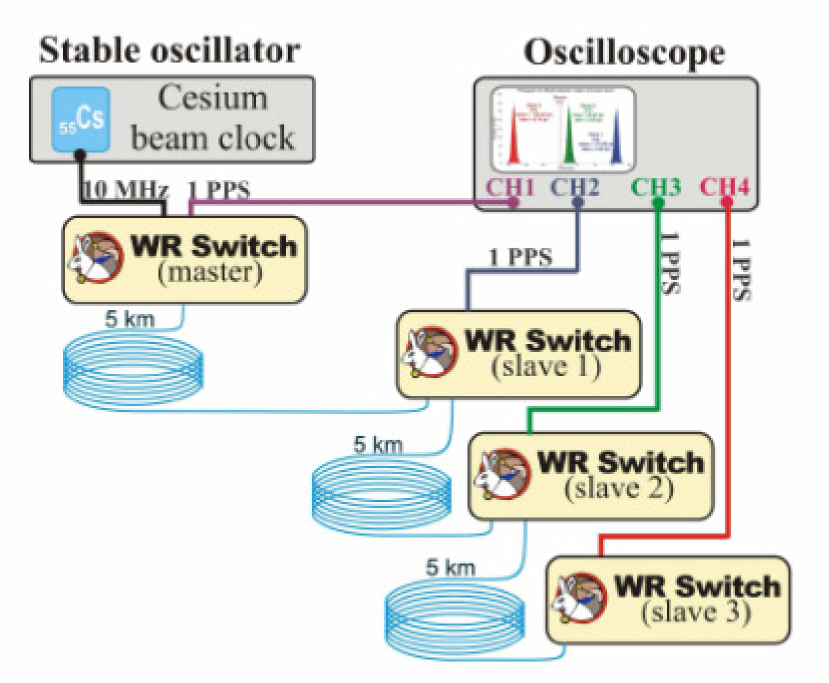
Over 6,000 detector units
Spread around 1km^2 area

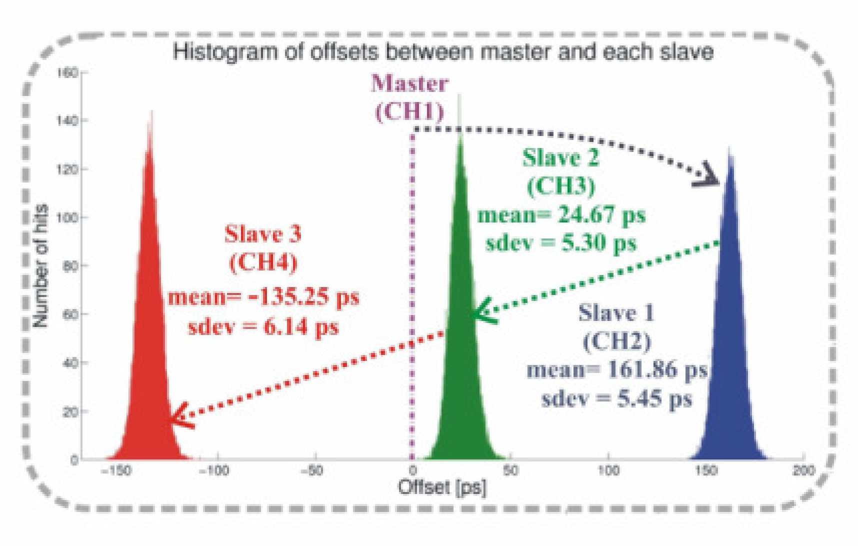
0.5° Angular resolution for shower reconstruct from *timing* of hits TOA

Synchronous timing among detectors

1000m coax cable in 30°C change, Δ delay = 15ns!

WR performance（@CERN）

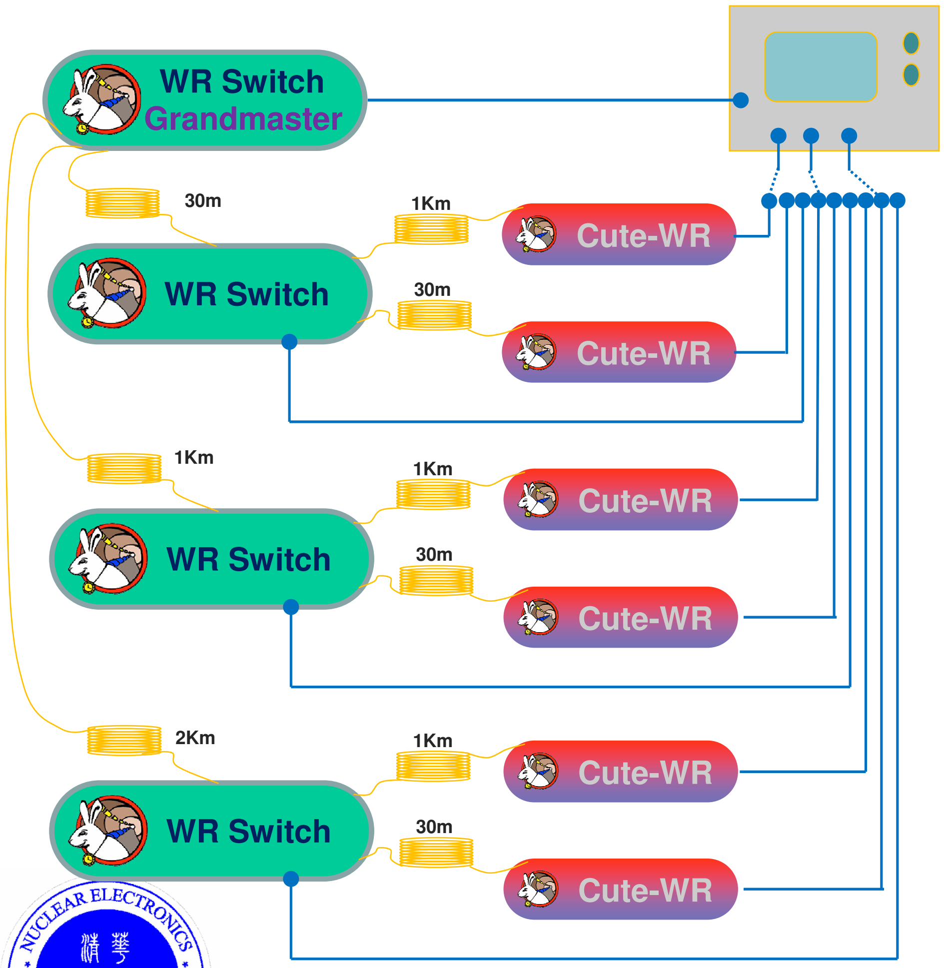


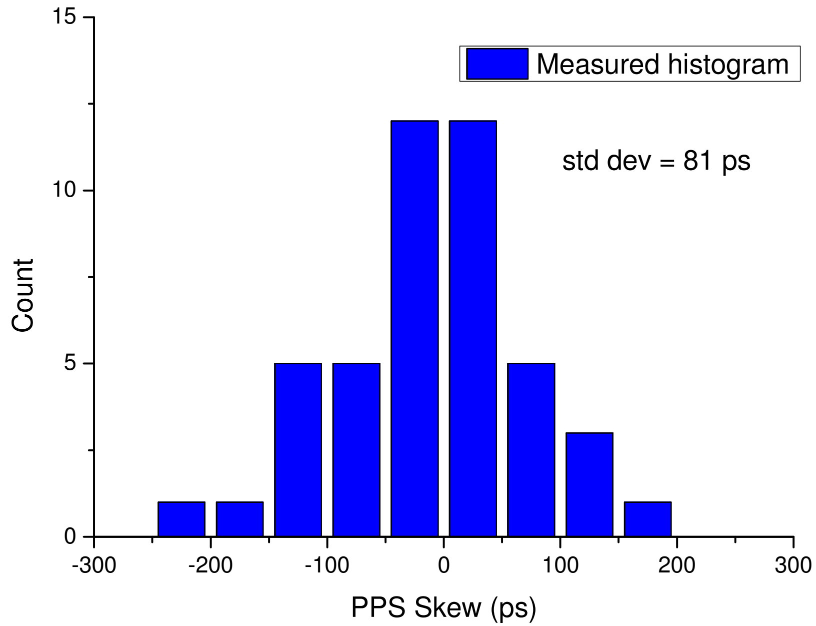


WR test（@Tsinghua）

- Test includes:
  - 4 WR switch v3.3
  - 8 Cute-WR nodes
  - Rolls of SM fiber (few km each)
- Performance test
  - Precision/accuracy test
  - Consistency test
  - Topology test
- measurement
  - Set the PPS from top-level WRS as reference.
  - Measure the offset between PPS signals from other WRS/Cute-WR
  - Results include different situations:
    - Fiber length, WR nodes, SFP modules, WRS ports, connections, power-cycle, link-up, components exchange,

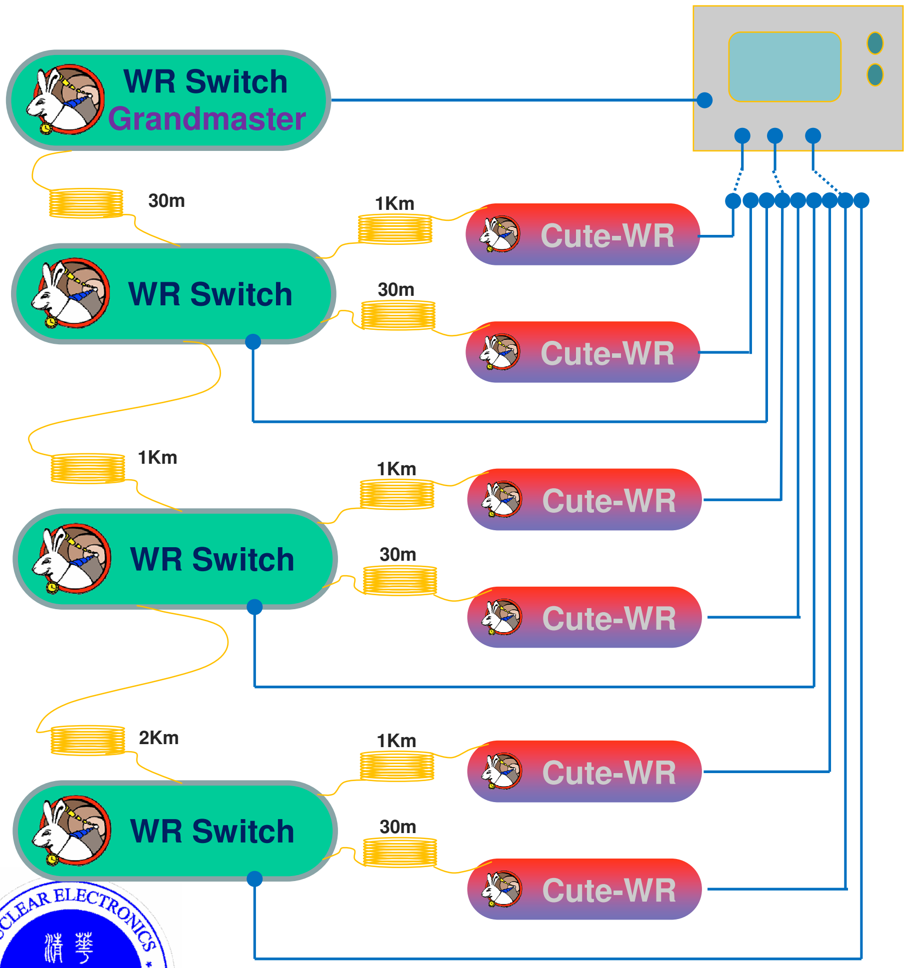
WR performance（@Tsinghua)

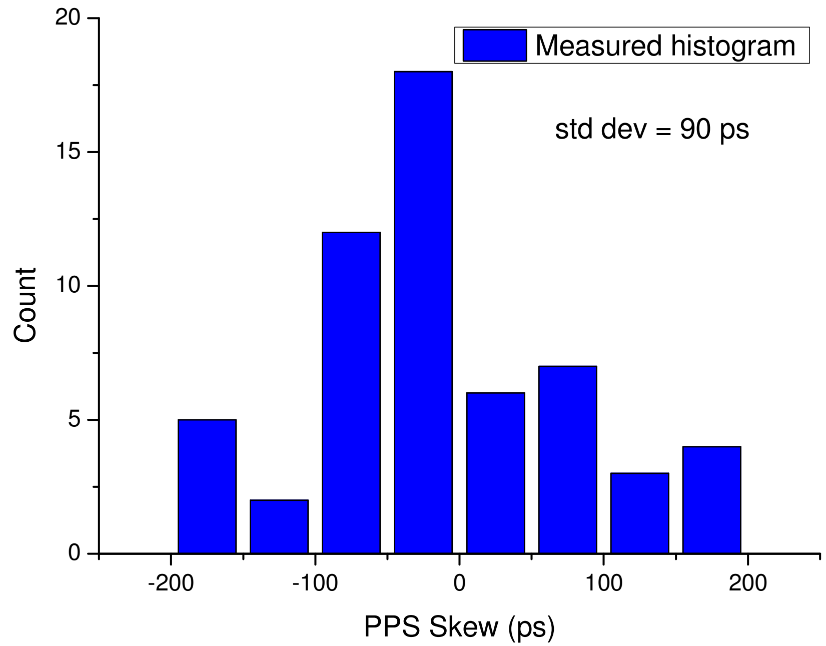




Parallel topoloty

WR performance（@Tsinghua)

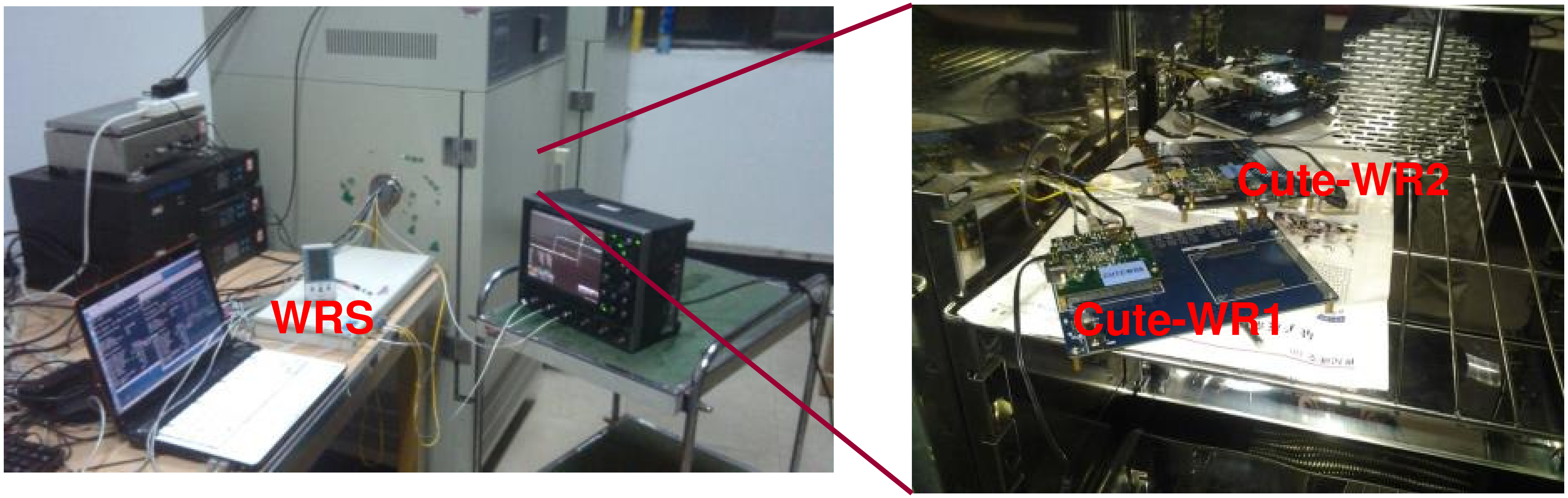




Cascade topoloty

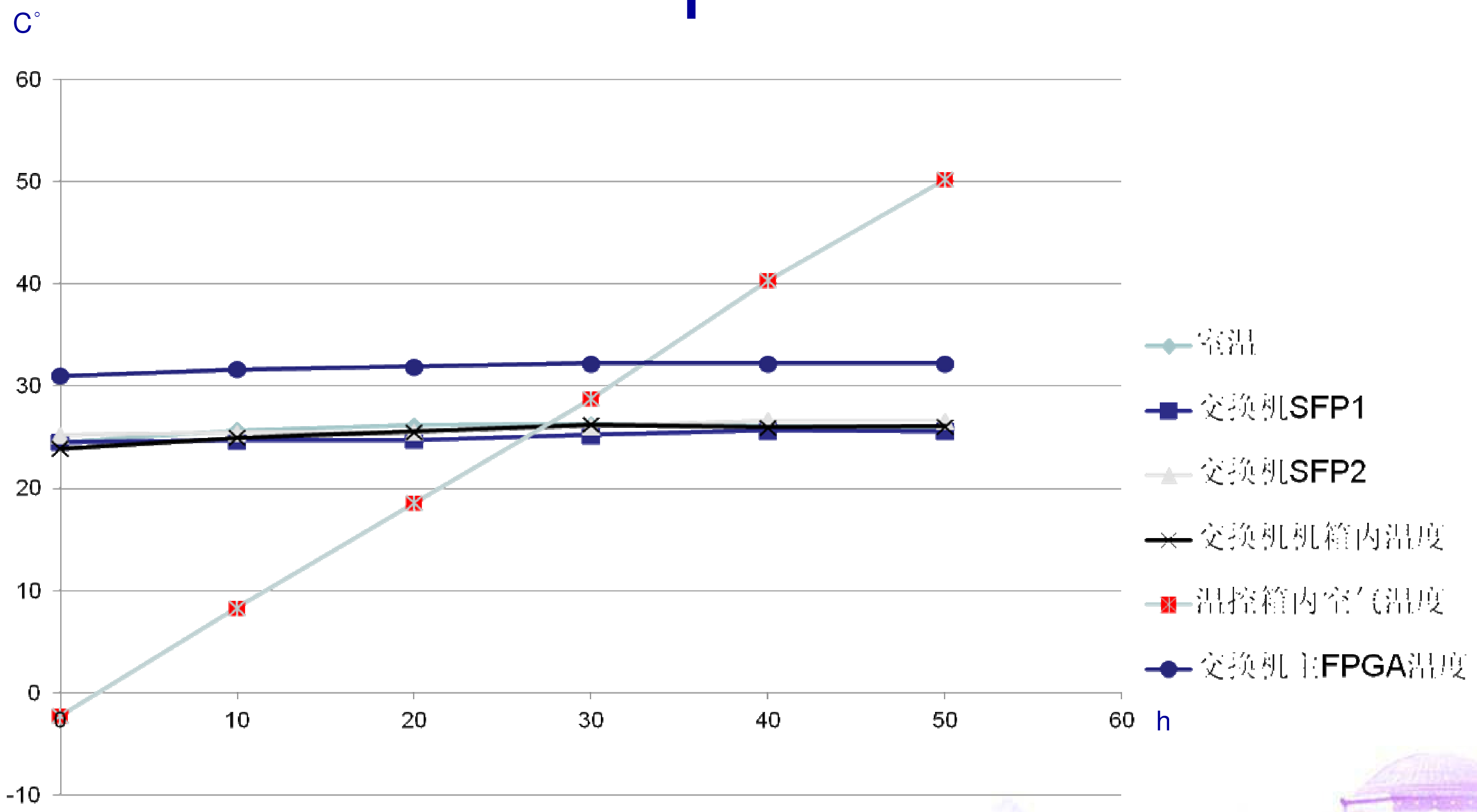
One layer less than KM2A deployment

WR temp. effect



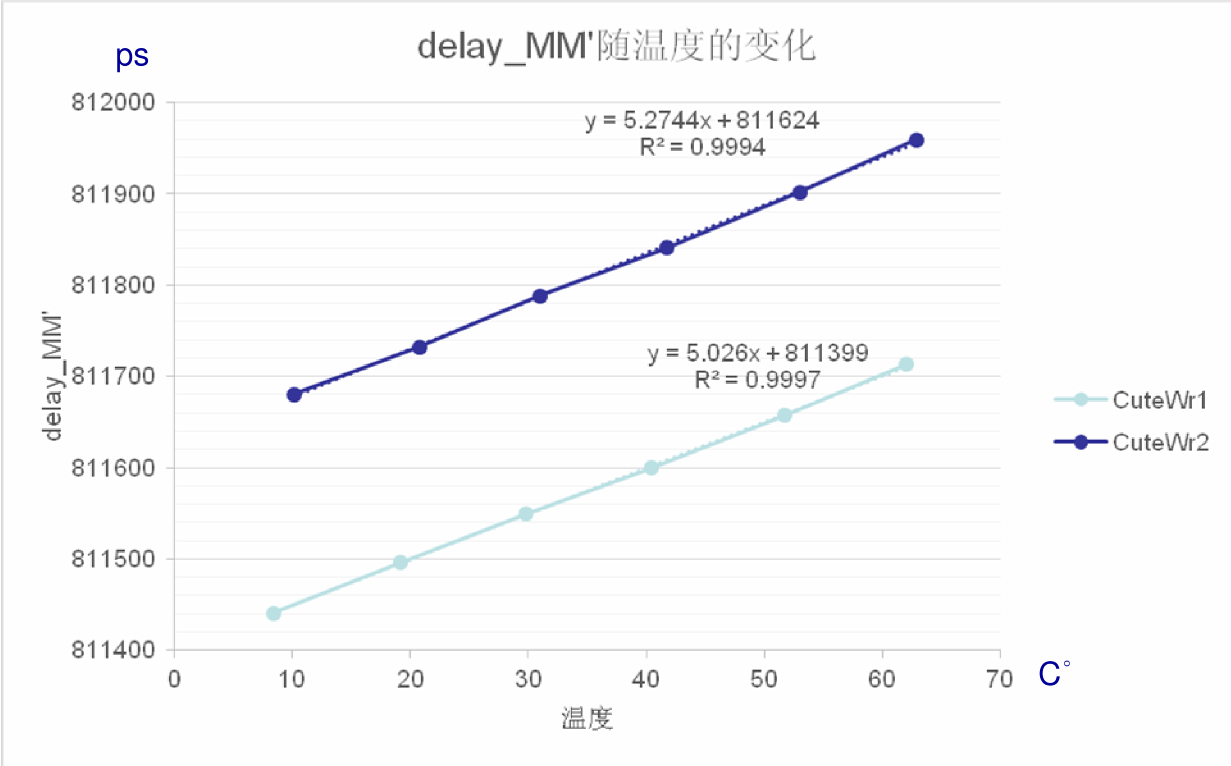
- Fiber temp. variation is compensated by DMTD&PTPv2
- Temp. effect of Cute-WR fixed delay can be problem
  - Put Cute-WR in incubator
  - Temp. range 0-50 degree
  - Environmental temp. are monitored.

Temp. record



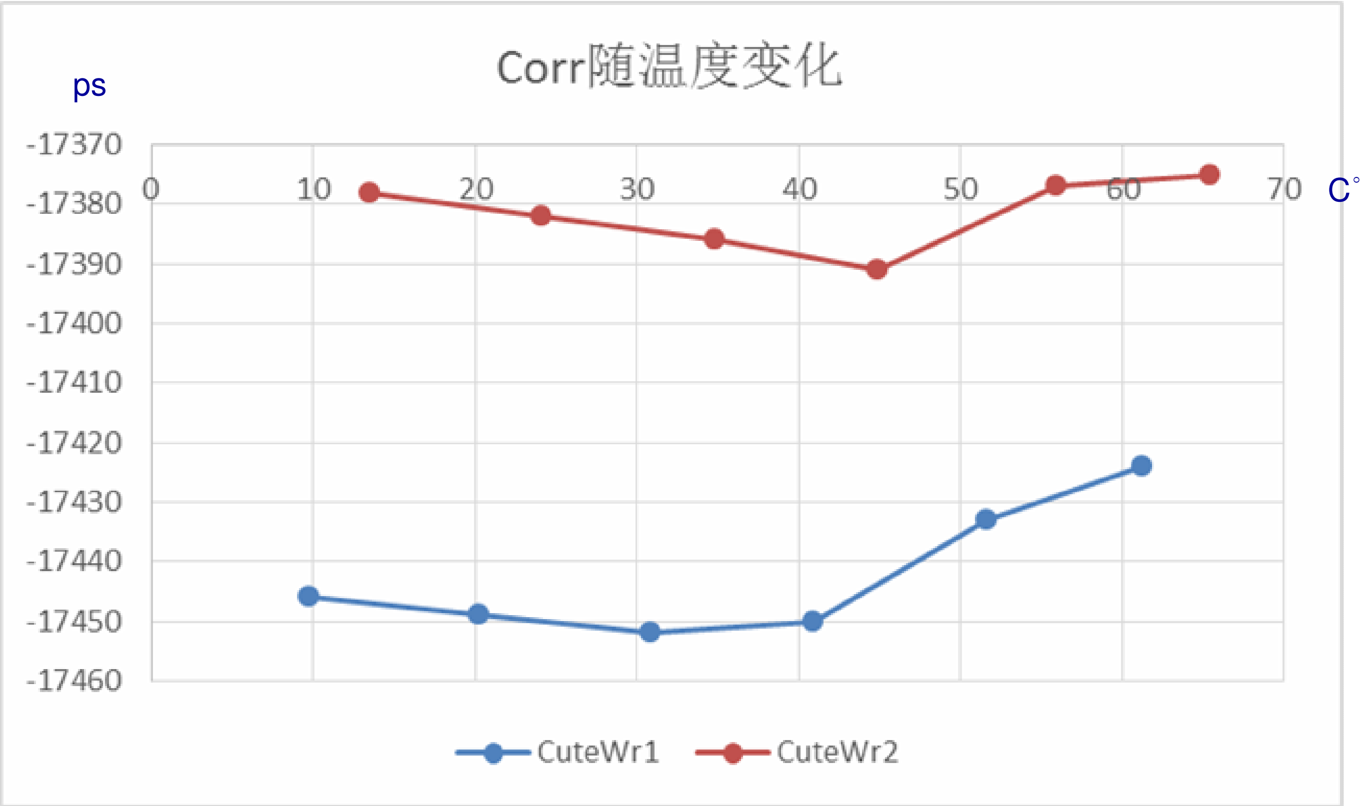
C°
60
50
40
30
20
10
0
-10
0
10
20
30
40
50
60
h
室温
交换机SFP1
交换机SFP2
交换机机箱内温度
温控箱内空气温度
交换机主FPGA温度

temp. dependency of Cute-WR fixed delay



- $(\delta_{txs} + \delta_{rxs})$ ~5ps/℃

After temp. compensation



- A temp. range of 50℃, 50ps accuracy can be achieved after temp. compensation