# FRONT-END ELECTRONICS BASED ON PARISROC ASIC FOR THE LHAASO EXPERIMENT

Yingtao CHEN, IPNO, France/YNU, China

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# Outline

- The requirements of WFCTA
- The PARISROC 2 ASIC
- Design of the new FEE
- Results
- Conclusions

# Collaboration (see talk of Tiina Suomijärvi)

- Physicists (IPN-Orsay)
  - Yingtao Chen (PhD student funded by CSC), Olivier Deligny, Isabelle Lhenry-Yvon, Tiina Suomijärvi, Francesco Salamida (post-doc), Diane Martraire (PhD student)
  - New PhD student, Zizhao Zong, applying funds from CSC
- Technical group
  - Valerie Chambert, Bengyun Ky, Emmanuel Rauly, Thi Nguyen Trung, Eric Wanlin (IPN-Orsay)
  - Gisele Martin-Chassard, Frederic Dulucq, Christophe de la Taille (OMEGA)
- Collaboration with the Chinese LHAASO groups, in particular with the group of Zhen Cao from IHEP.

# Wide Field of view Cherenkov/Fluorescence Telescope Array (WFCTA)

**Telescopes**

- The angular resolution: *< 0.4°*
- The energy resolution: *< 20%*
- The resolution of the location of shower maximum: *< 40 g/cm²*
- The Field of View (FOV) of a single telescope: *14° X 16°*
- Dynamic range: *3 orders of magnitude of the energy*
- Movable design for different purposes
- 24 identical telescopes divided into 3 groups with a distance of 100 m

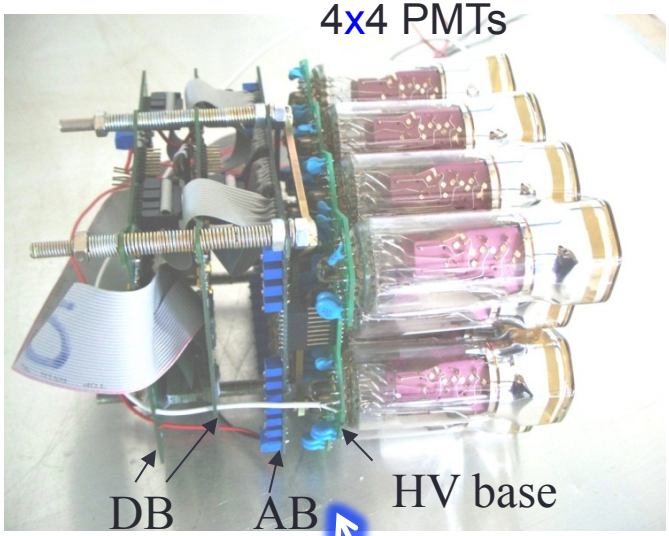
**Electronics**

- Signal polarity: *Negative or positive*
- Dynamic range: *160 fC to 240 pC*
- Nonlinearity: *< 2%*
- Charge resolution: *< 20% @160 fC and <5% @ 240 pC*
- Time resolution: *20 ns (RMS)*
- Single channel event rate: *10 kHz*
- Signal width: *6 ns to 50 ns (Cherenkov)*
- Pedestal monitoring: *Sky and electronics*
- Channels: *1024 per telescope*
- Power consumption: *260 W*

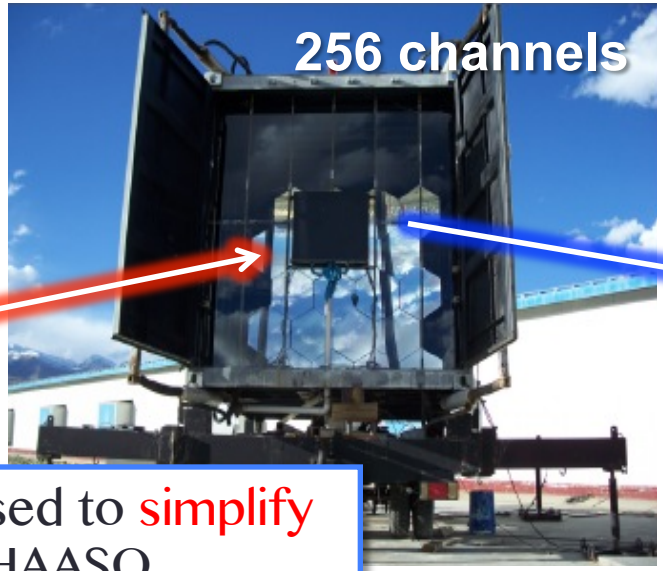
Prototypes in YBJ, Tibet

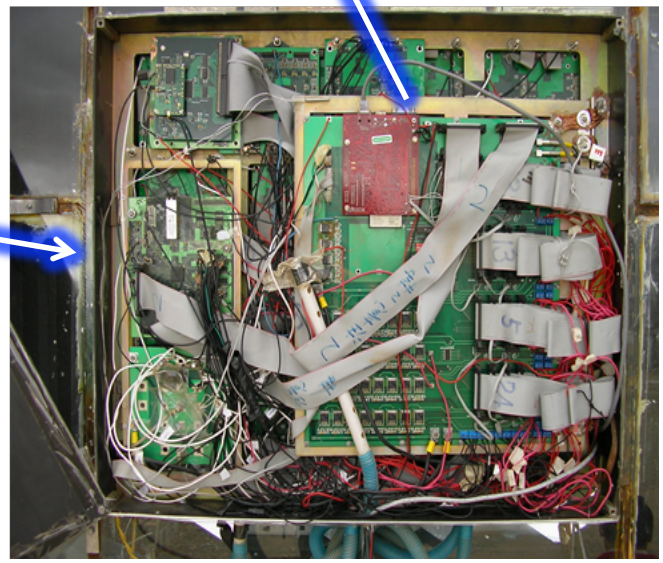
# Challenges for electronics

- High altitude and low air pressure ➔ *decreased heat dissipation*
- Large number of channels ➔ *increased density, complexity and power consumption*
- Harsh environment and remote location ➔ *require stability, reliability and maintainability*
- Design based on IC ➔ *simplified design, decreased power consumption, increased reliability*




- Compact design
- High stability
- High reliability
- Easy to maintain



Prototypes in YBJ, Tibet

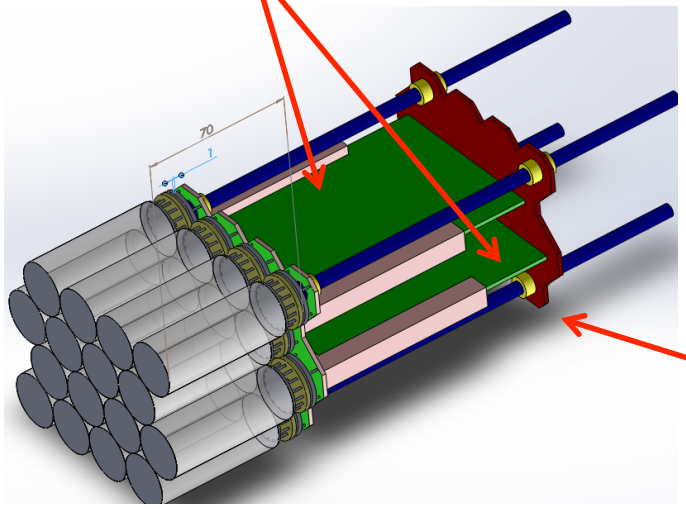
We focused on WFCTA at first.

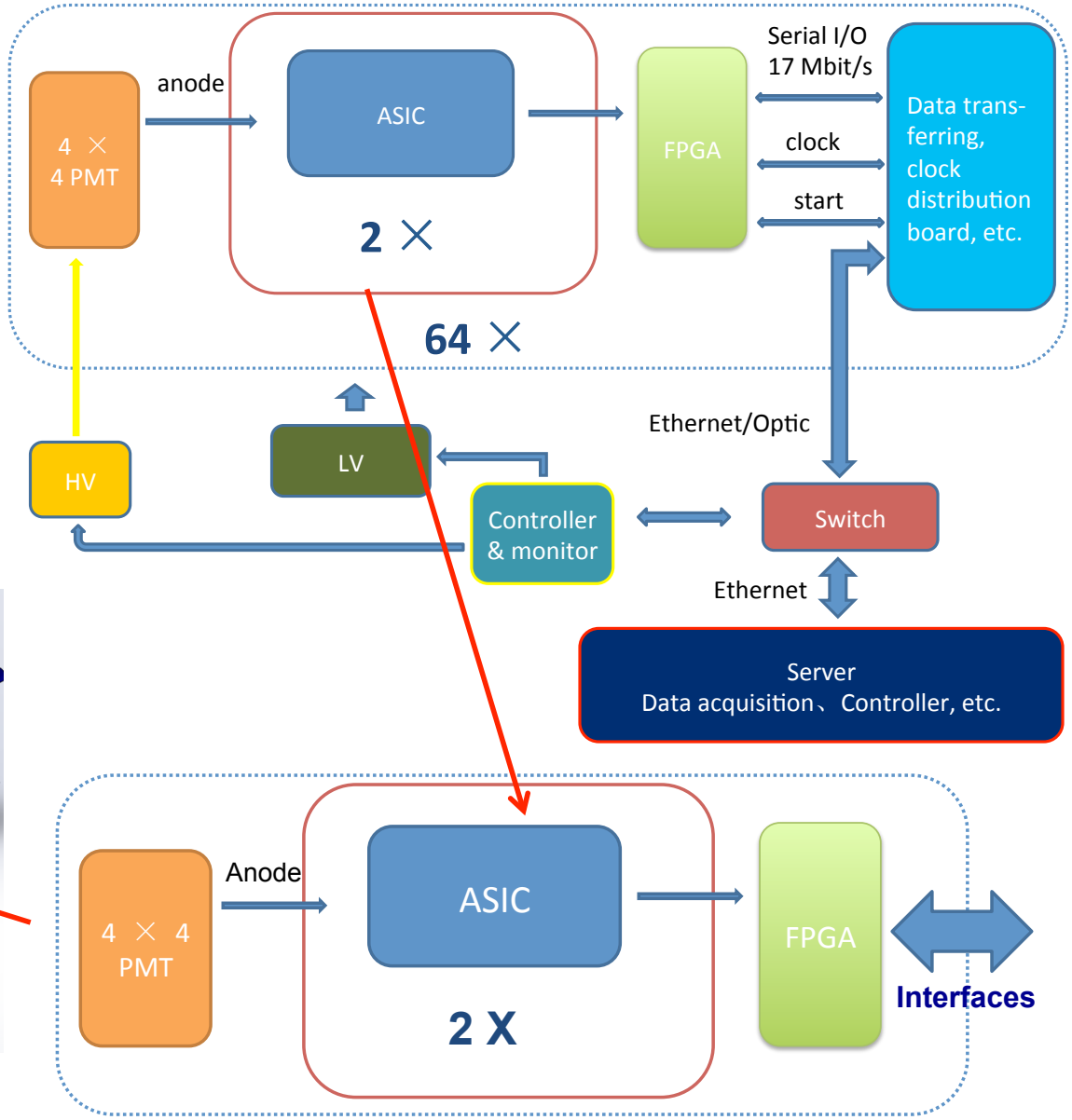
The ASICs can be used to simplify the electronics of LHAASO.

# The schema of electronics of WFCTA

- **Large number of channels**
  - WFCTA: 1024 channels each
- **Heat dissipation at 4300m**
  - Air density: 60%
  - Active heat dissipation system
- **Reliability & Maintainability**
  - "SoC + FPGA" Design

FEE boards

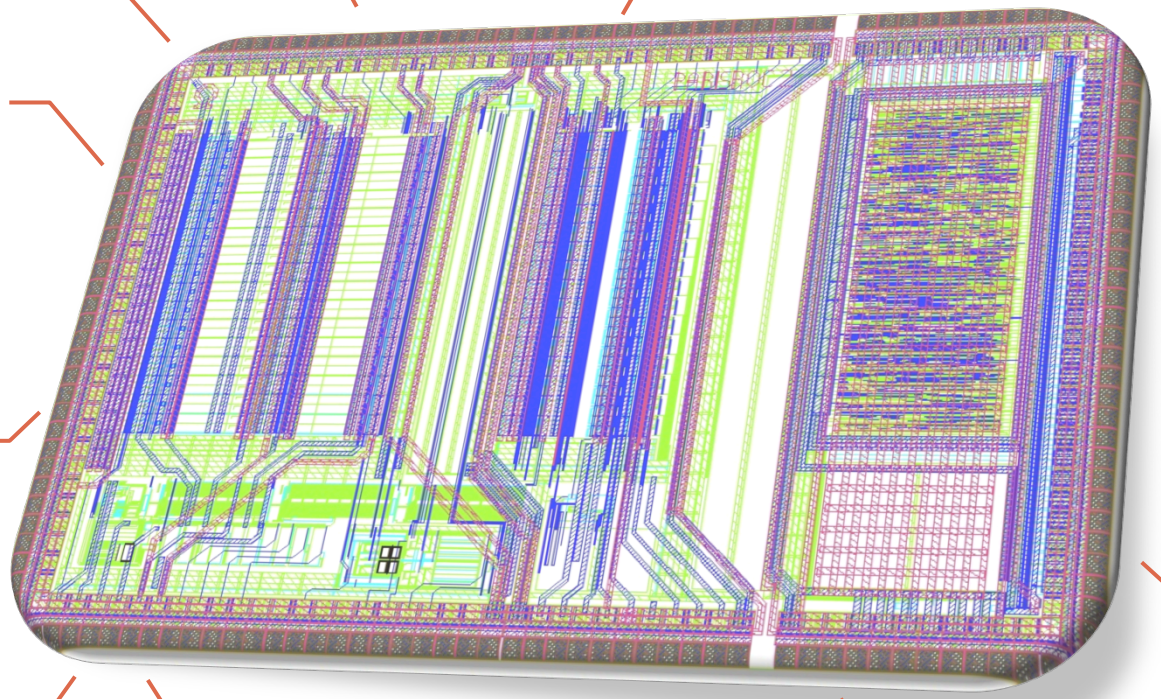




*Technology: 0.35μm SiGe AMS*

# Photomultiplier ARray Integrated in SiGe ReadOut Chip

PARISROC 2 is designed by OMEGA Group



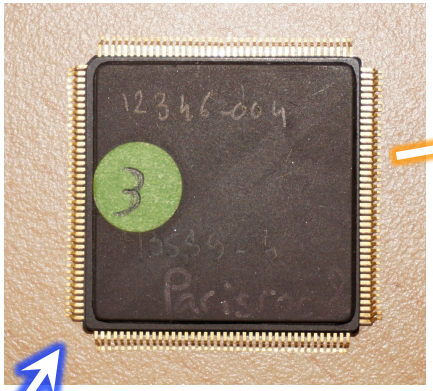
- Dual-gain Preamplifiers
- Time measurement: tagging < 1 ns
- 16 Channels (neg.)
- 10 bit ADC internal conversion
- TQFP160 5 mm X 3.4 mm
- A very complex SoC designed for multiple purposes and experiments
- Input range -0.8 V to 4.1 V
- 278 slow control parameters
- Auto-trigger design
- Charge measurement: 50 fC ~ 100 pC
- 15 mW / channel

S. Conforti Di Lorenzo et al., NIM A 2009.05.135, arXiv:0811.2681.

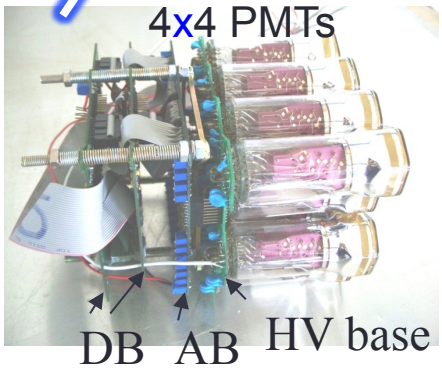
# Simplified block diagram

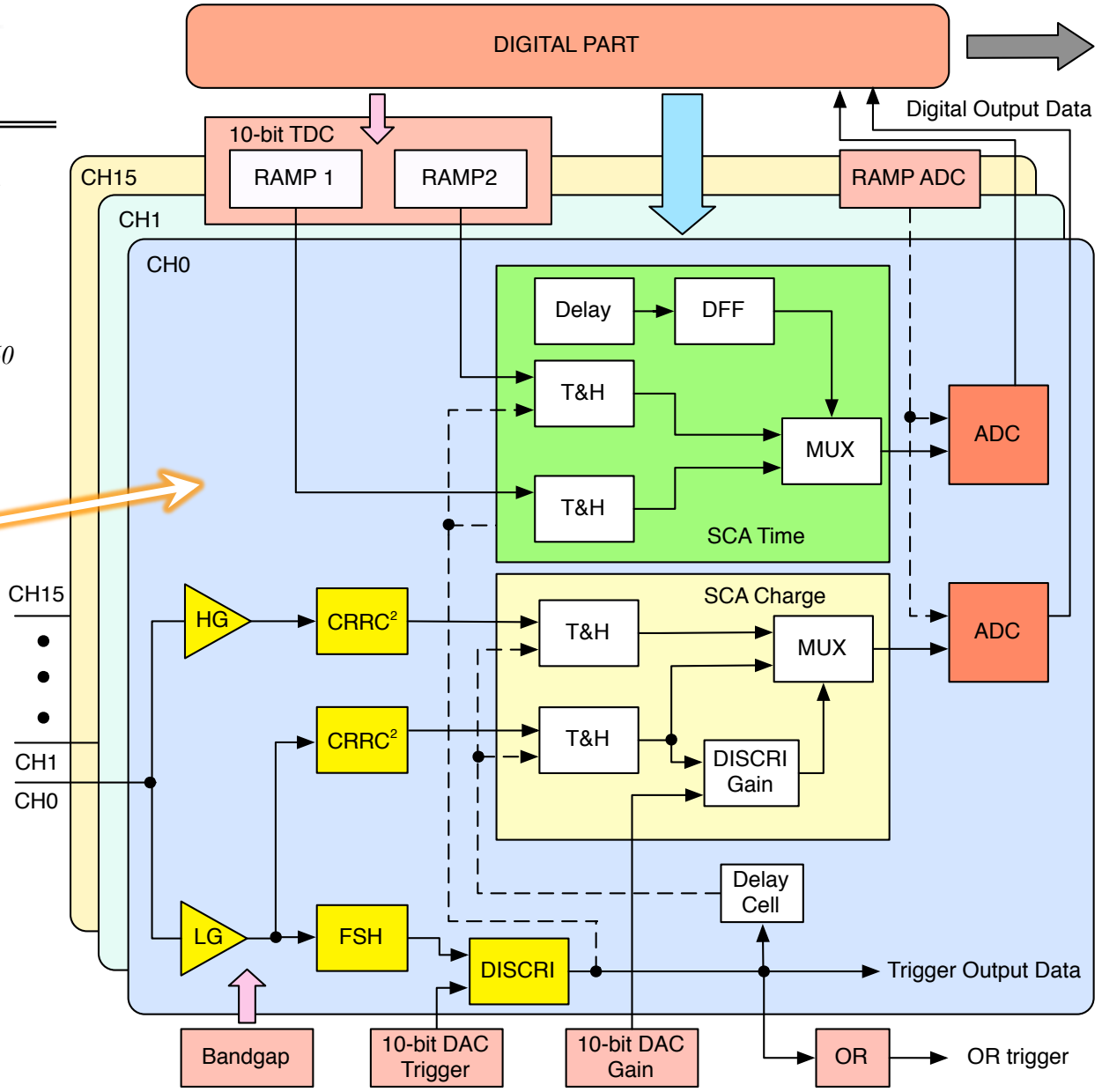
## PARISROC 2

| Property | Specification |
|---|---|
| **Technology** | *AMS 0.35µm SiGe* |
| **Die dimensions** | *5.034 mm × 3.42 mm* |
| **Area** | *17.21 mm²* |
| **Channels** | *16* |
| **Power Supply** | *3.3 V* |
| **Power Consumption** | *15 mW/channel* |
| **Package** | *CQFP-160/TQFP-160* |

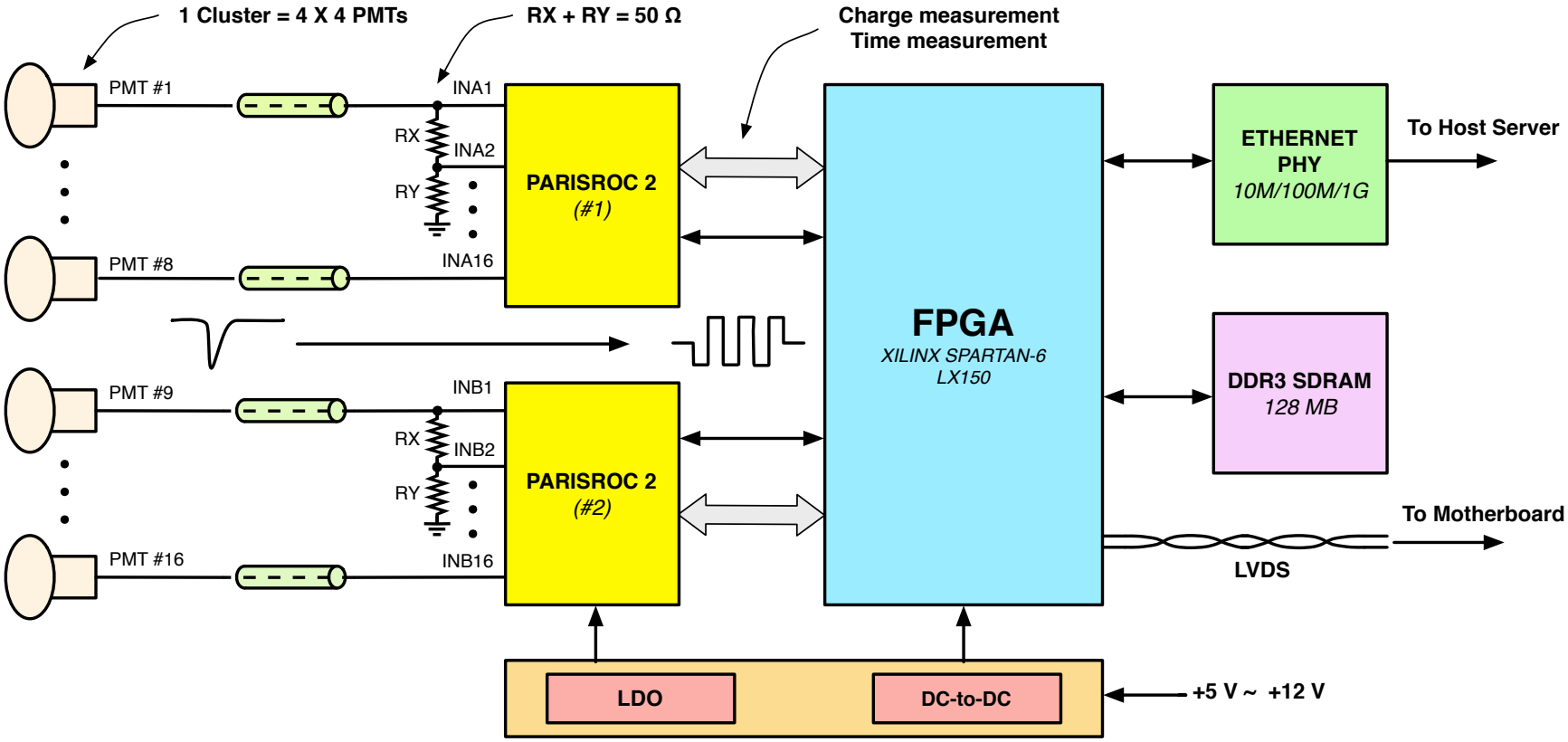


Die: 5 mm X 3.4 mm



# System block of the new FEE



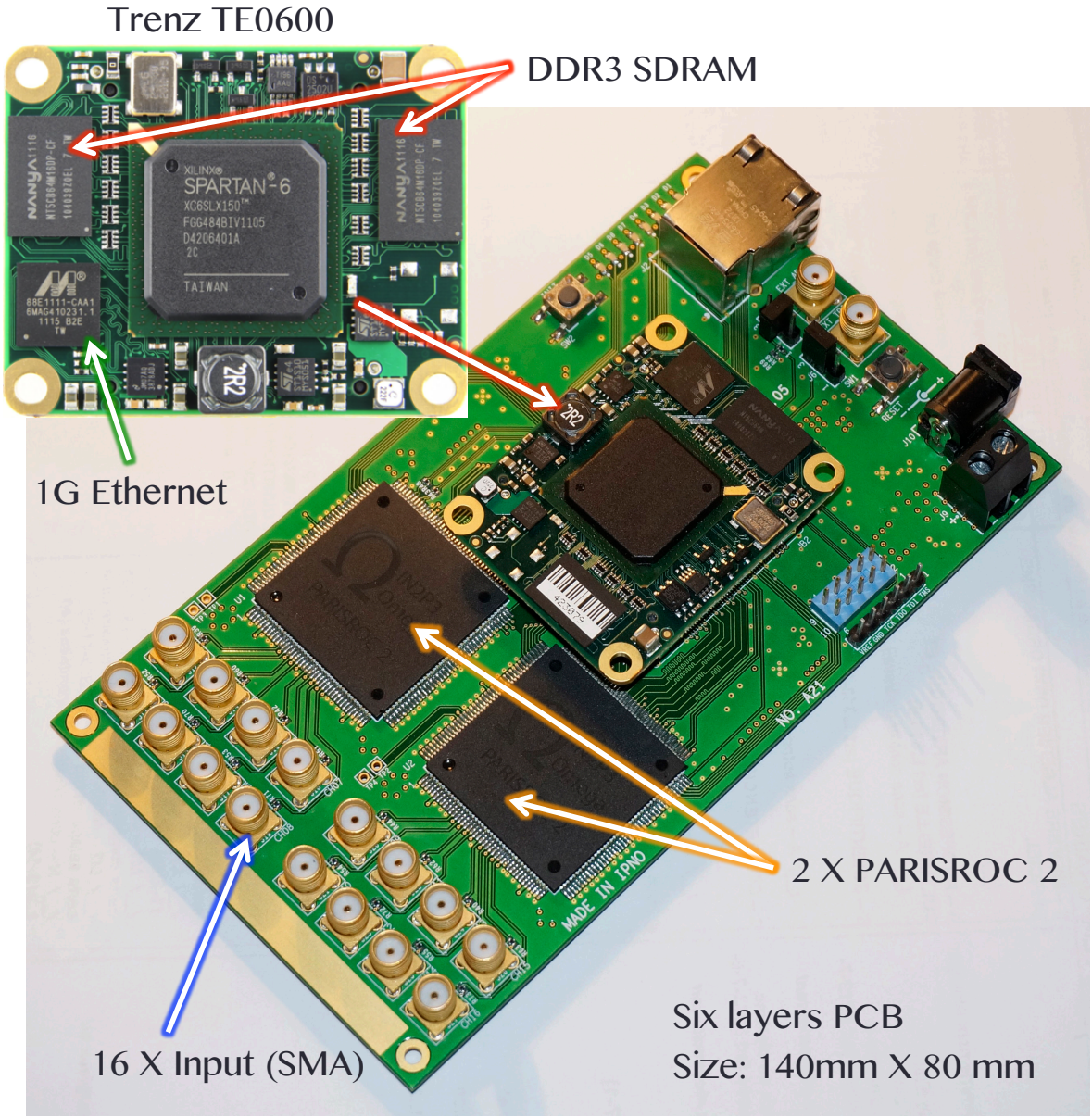

- Two PARISROC 2 chips with 2 groups of 16 inputs
- Voltage dividers at input to extend the dynamic range and keep nonlinearity low
- New powerful FPGA (Xilinx Spartan-6 LX150) as the central controller
- Multiple transferring protocols, such as 1G Ethernet, LVDS
- Power supply: +5 V to +12 V
- Can be easily adapted to any other experiment with similar requirements

Y.T. Chen et al., Front-end electronics based on an autonomous, trigger-less ASIC for LHAASO, 33rd ICRC, Rio de Janeiro, 2013

# Picture of the FEE

## Trenz TE0600-01

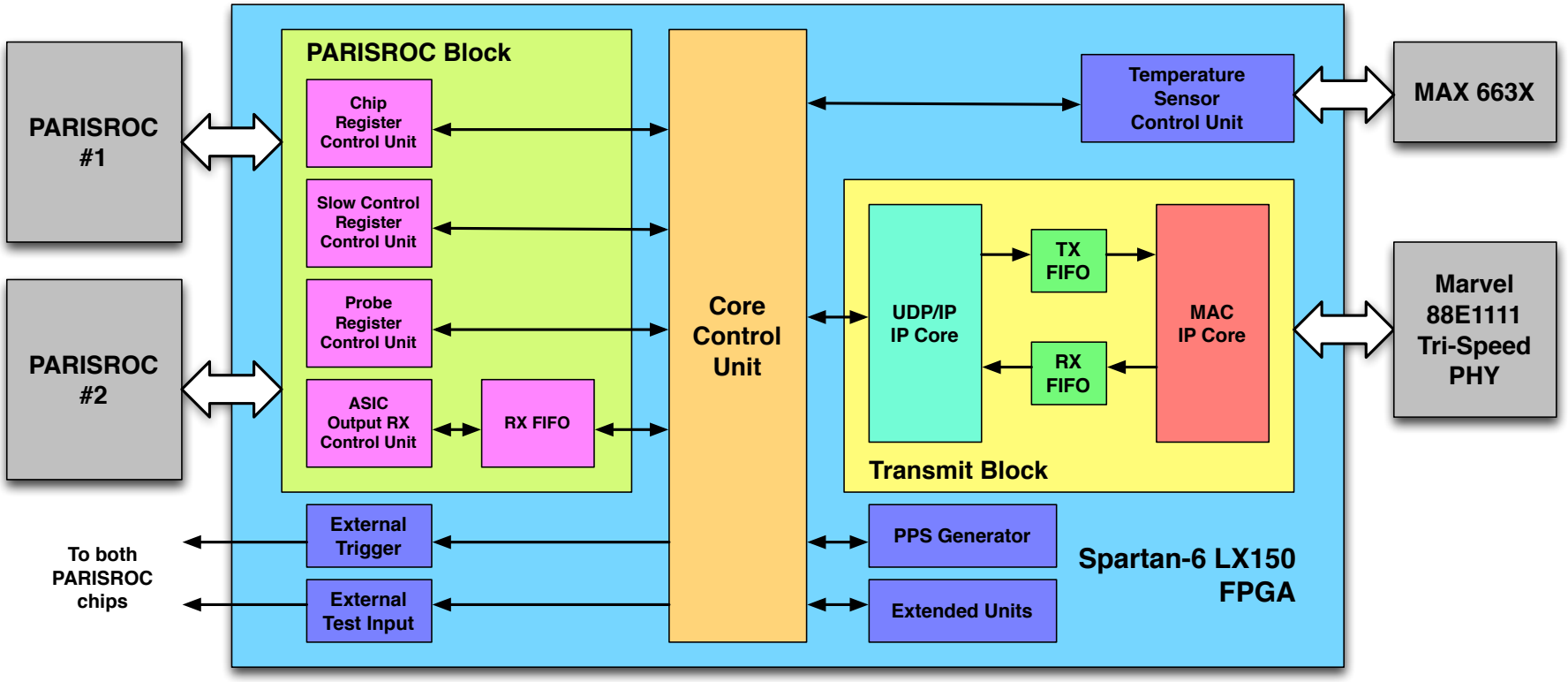
- Spartan-6 LX150: 147K
- Size: **50 mm × 40 mm**
- **10M/100M/1000M Ethernet**
- 2 x 16-bit 256MB DDR3 SDRAM
- 128Mb (16 MB) SPI Flash
- Robust board-to-board connectors (B2B) LSHM up to 10 GHz / 20 Gbps
- Up to 52 differential I/O
- Up to 109 single-ended I/O



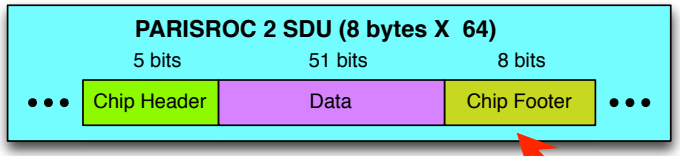
# Software block & power consumption

| Unit | Power Consumption |
|---|---|
| PARISROC 2 X 2 | ~ 1.0W |
| Ethernet Interface | ~ 1.1W |
| FPGA & Peripherals | ~ 0.9W |
| | ~ 3.0W (2.98W meas.) |

- Fully described in VHDL and FSM structure
- Resource occupation: < 10% (XS6LX150)
- Power consumption: ~ 128 W for 64 clusters without Ethernet Interface (260W budget)

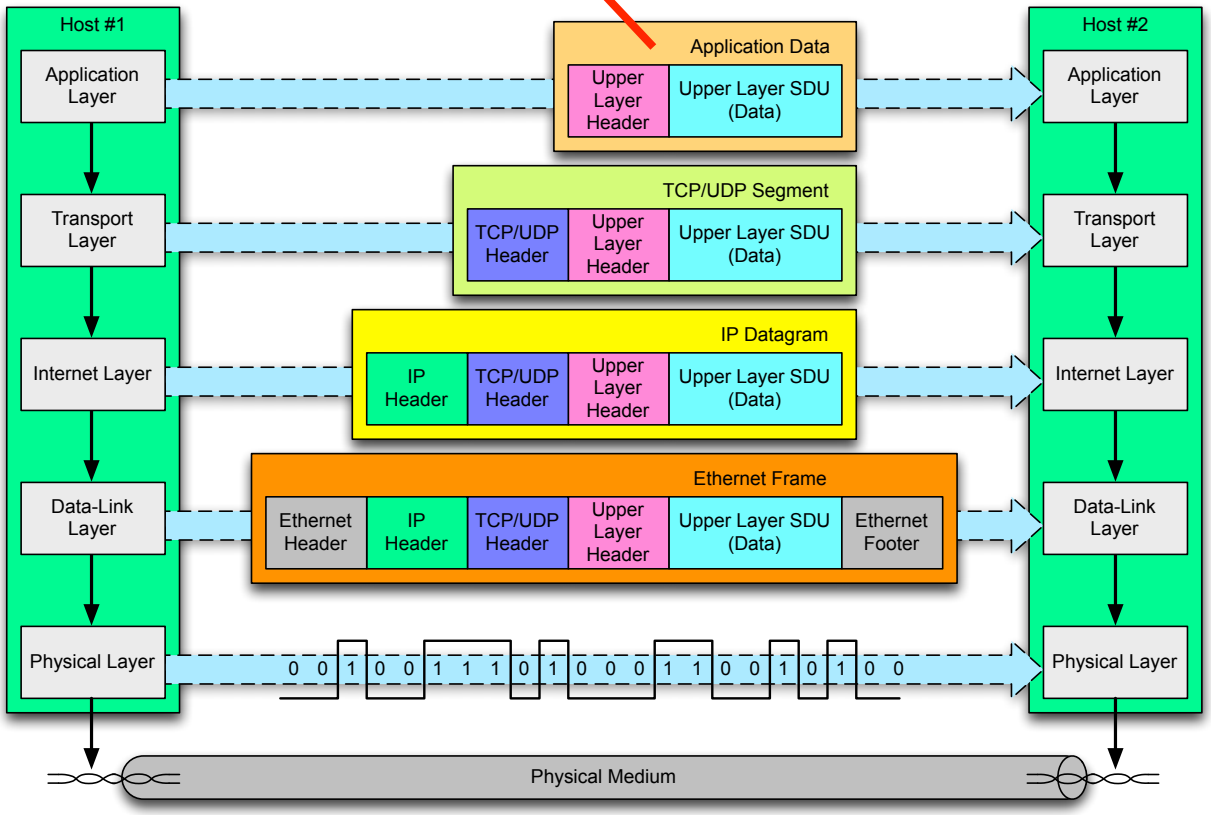


# Communication system

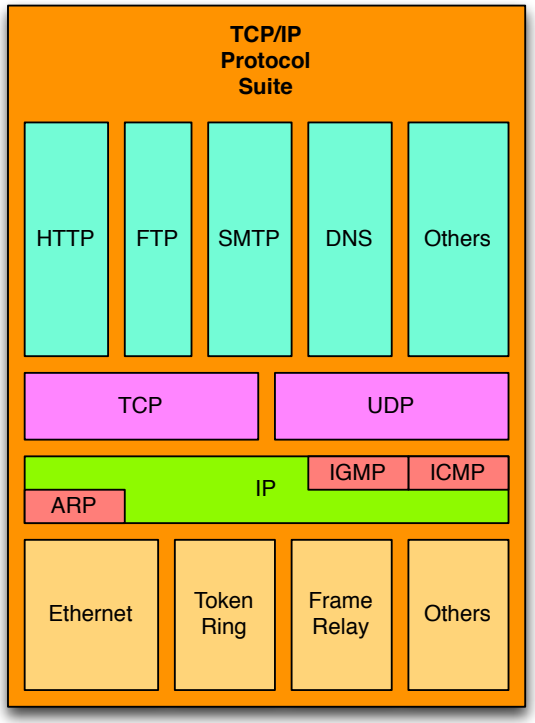



Chip header: Chip No.
Chip Footer: Time stamp or et al.

Length of a full frame: 555 bytes




Support standard UDP/IP Protocol

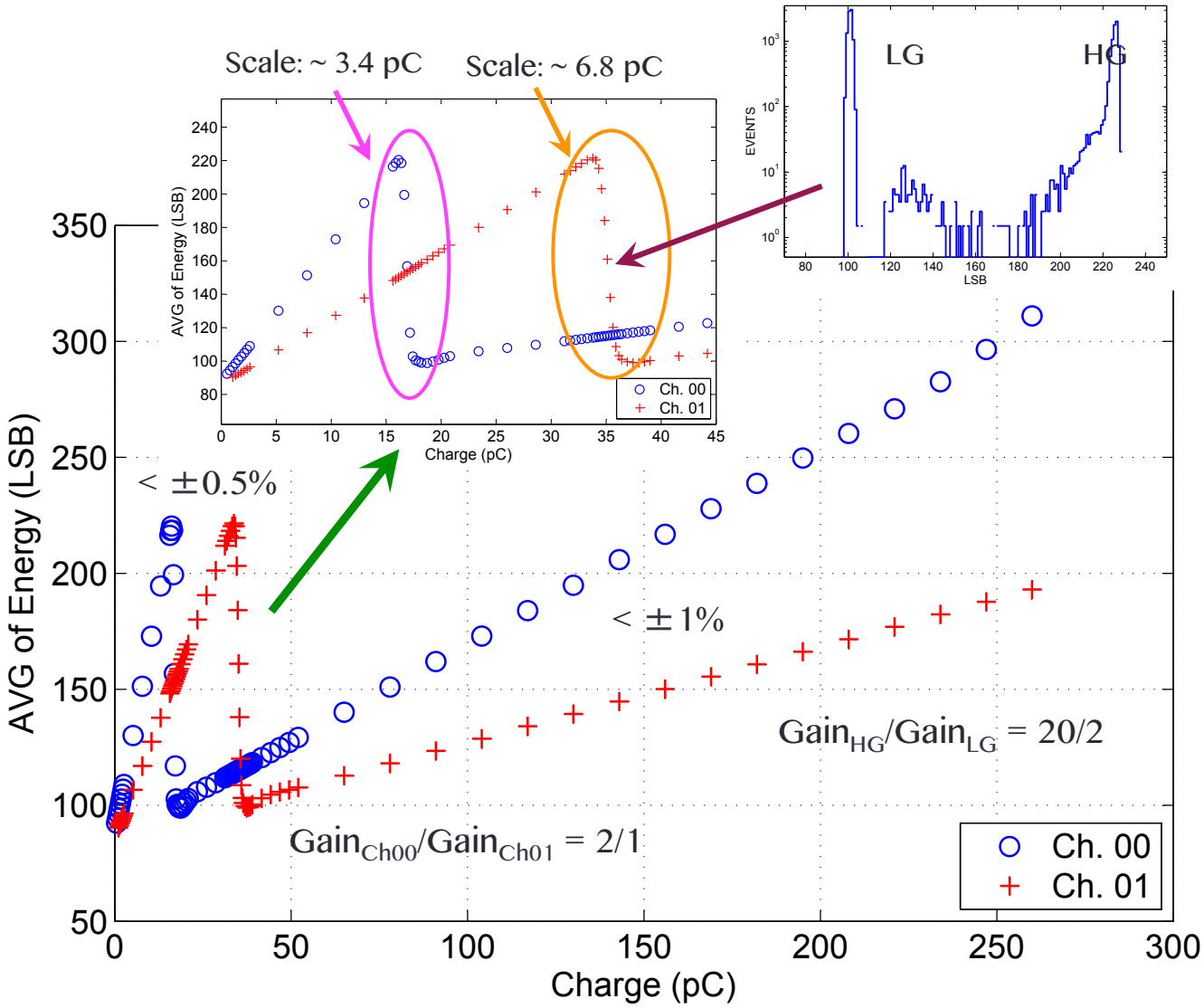



Bandwidth test
FEE ➔Ethernet data logger
Highest bandwidth: 972 Mbit/s

Data output rate of ASIC

- 56 bits/frame each channel
- Serial output (40 MHz)
- 5 kHz: 4.48 Mbit/s
- 20 kHz: 17.92 Mbit/s

# Results: General electronics tests




Voltage divider as input extends the dynamic range and keeps nonlinearity low

- DR: 0.16 pC to 240 pC
- NL: < ±1%

Event rate (16 channels)

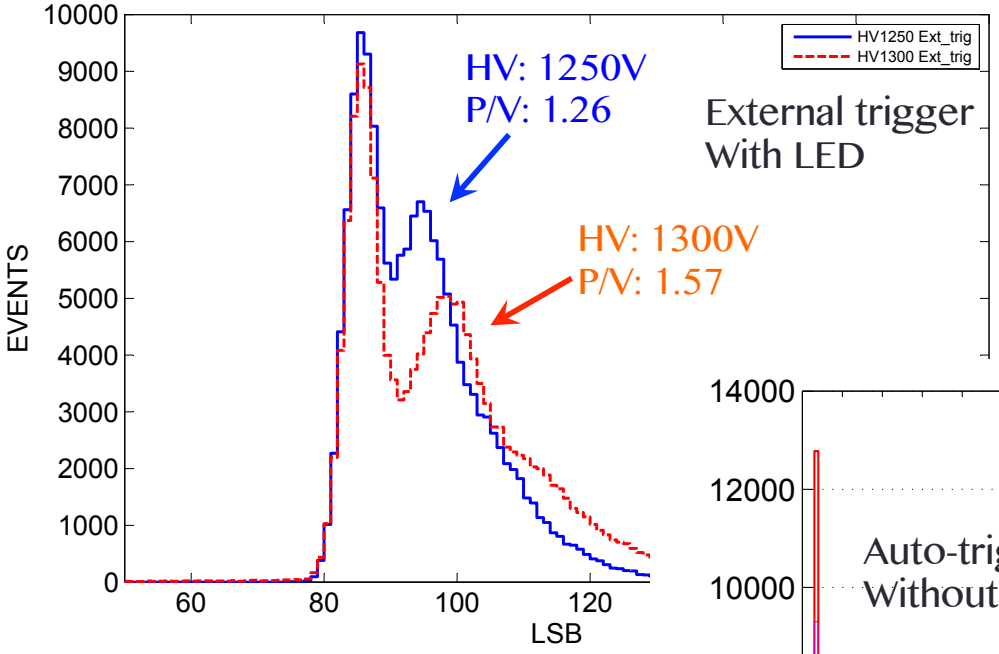
- TDC on: ~ 24 kHz (53.24 Mbit/s)
- TDC off: ~ 37 kHz (82.14 Mbit/s)

Pedestal monitoring

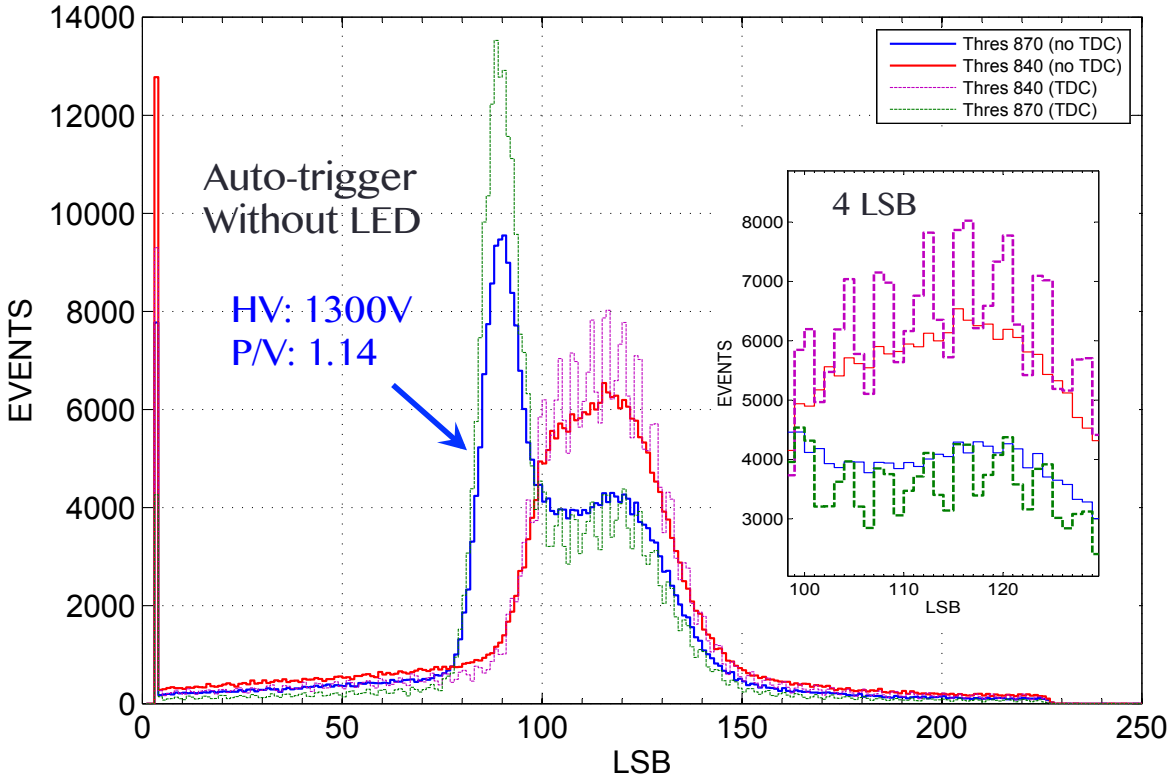
- Electronics: external trigger
- Sky: counting rate

ASIC Conf. : Time constant =100ns; Gain = 16K **1 mV ≈ 260 fC; 0.6 mV ≈ 160 fC ≈ 1pe @ PMT Gain = $10^6$**

# Results: PMT tests



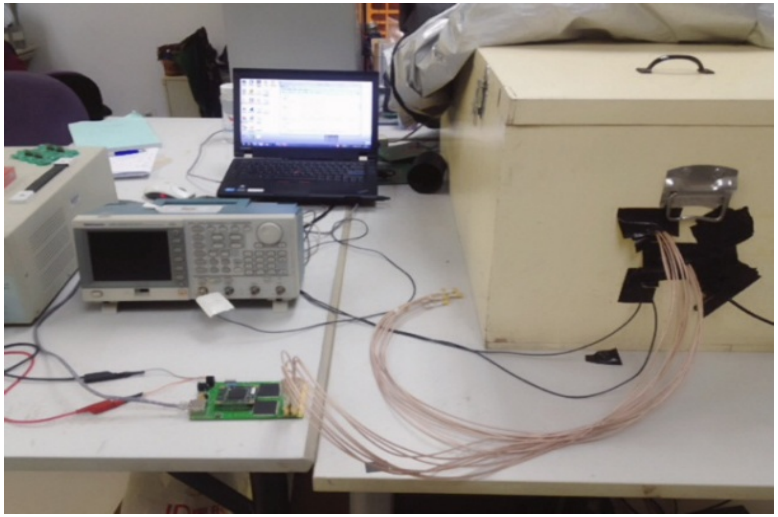

By using external trigger, the SPE spectrum can be easily extracted with good P/V ratio.



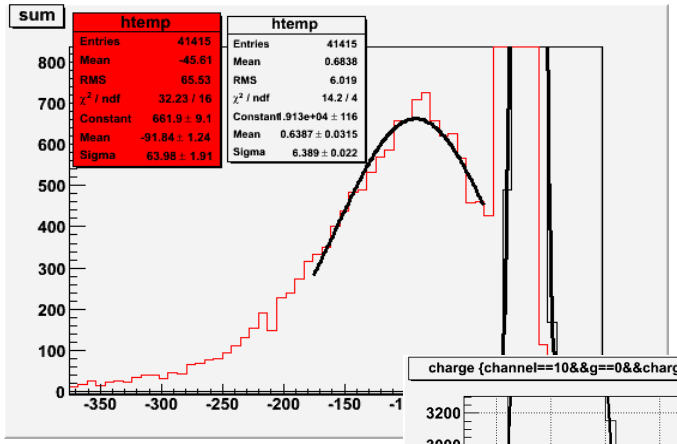

The periodical crosstalk from TDC unit will affect the accuracy of charge measurement when the internal trigger is used.

However, the threshold will not affect the location of the pedestal and the SPE peak.

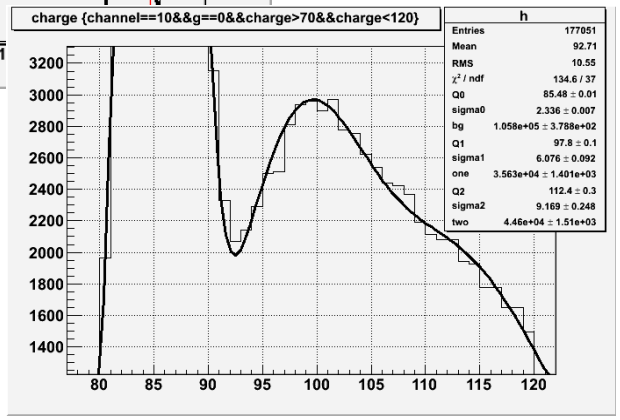
# Results from IHEP



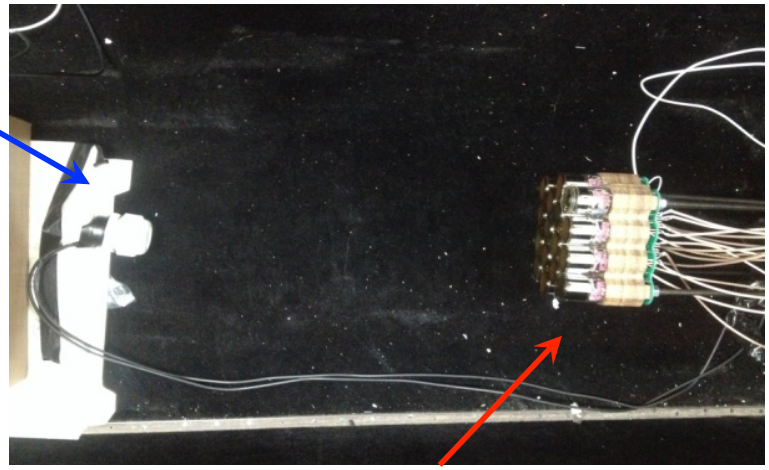
Test bench in IHEP




Oscilloscope




FEE based on PARISROC 2




Tests in progress with a 16 PMT array:

- Dynamic range and nonlinearity
- Trigger efficiency
- Event rate
- Signal duration

# Current Plan

- FEE tests for WFCTA
  - Tests with 16 PMTs continue
  - Tests with scintillators
  - Field test in Tibet with scintillator detectors
  - Prototype telescope test
- Adapting PARISROC to other detectors
  - Water tank test for WCDA
  - Scintillator test for KM2A

- **OMEGA plans to upgrade the ASIC in the fall 2014**
  - The requirements and improvements will be proposed before May 2014.
  - The new **PARISROC** version is coming up early 2015.

# Conclusions

- The ASICs are adapted for experiments like LHAASO at high altitude.
- The performances of the PARISROC 2 has been studied for WFCTA in Cherenkov mode.
  - Signal duration
  - Dynamic range
  - Nonlinearity
  - Event rate
  - Pedestal monitoring
- New FEE based on PARISROC 2 has been designed and tested.
- OMEGA plans to upgrade PARISROC this year.
  - Tests of the current FEE should be completed before May 2014.

# Thank you
for your attention!