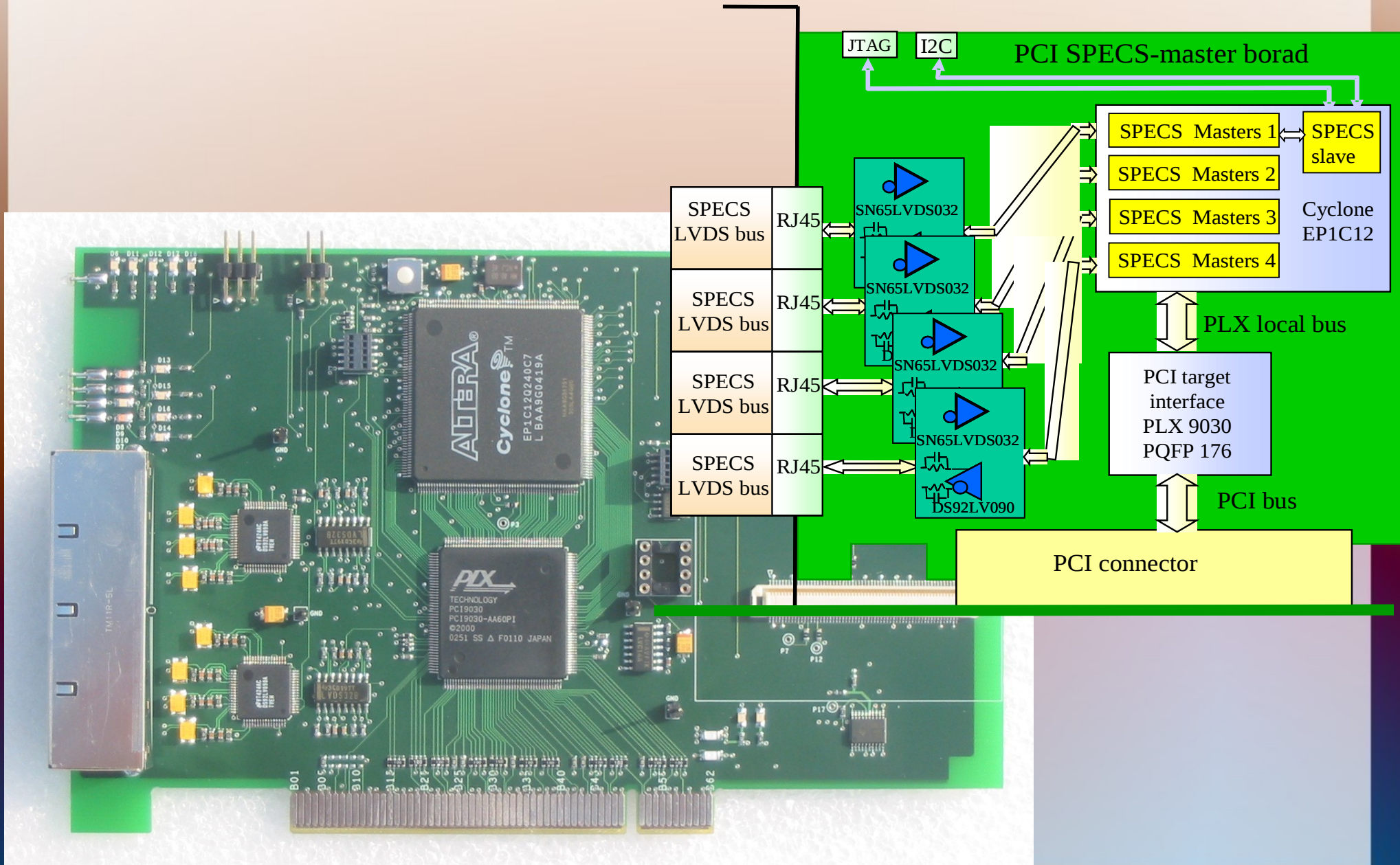




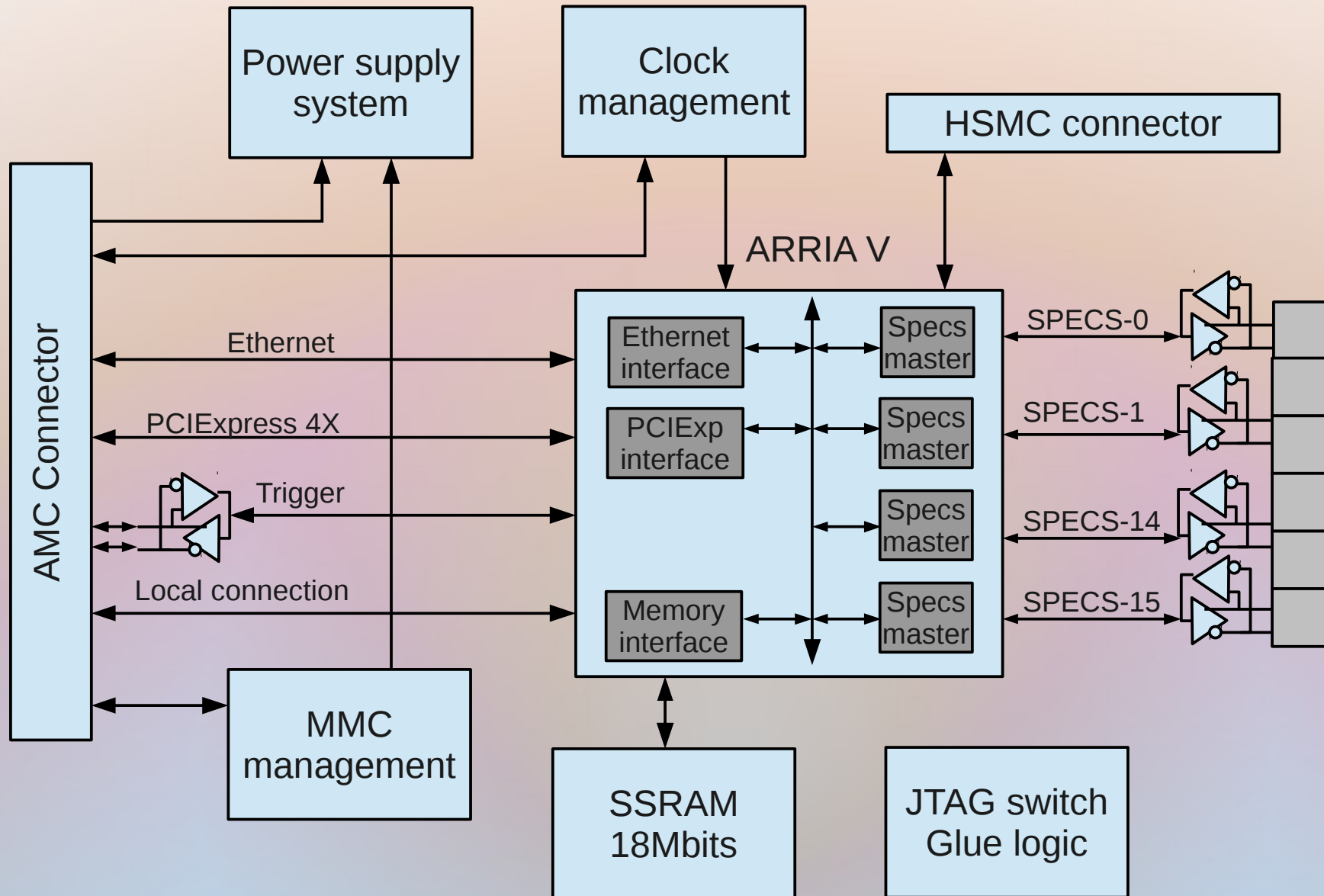


# SPECS master version 1





# SPECS master version 2





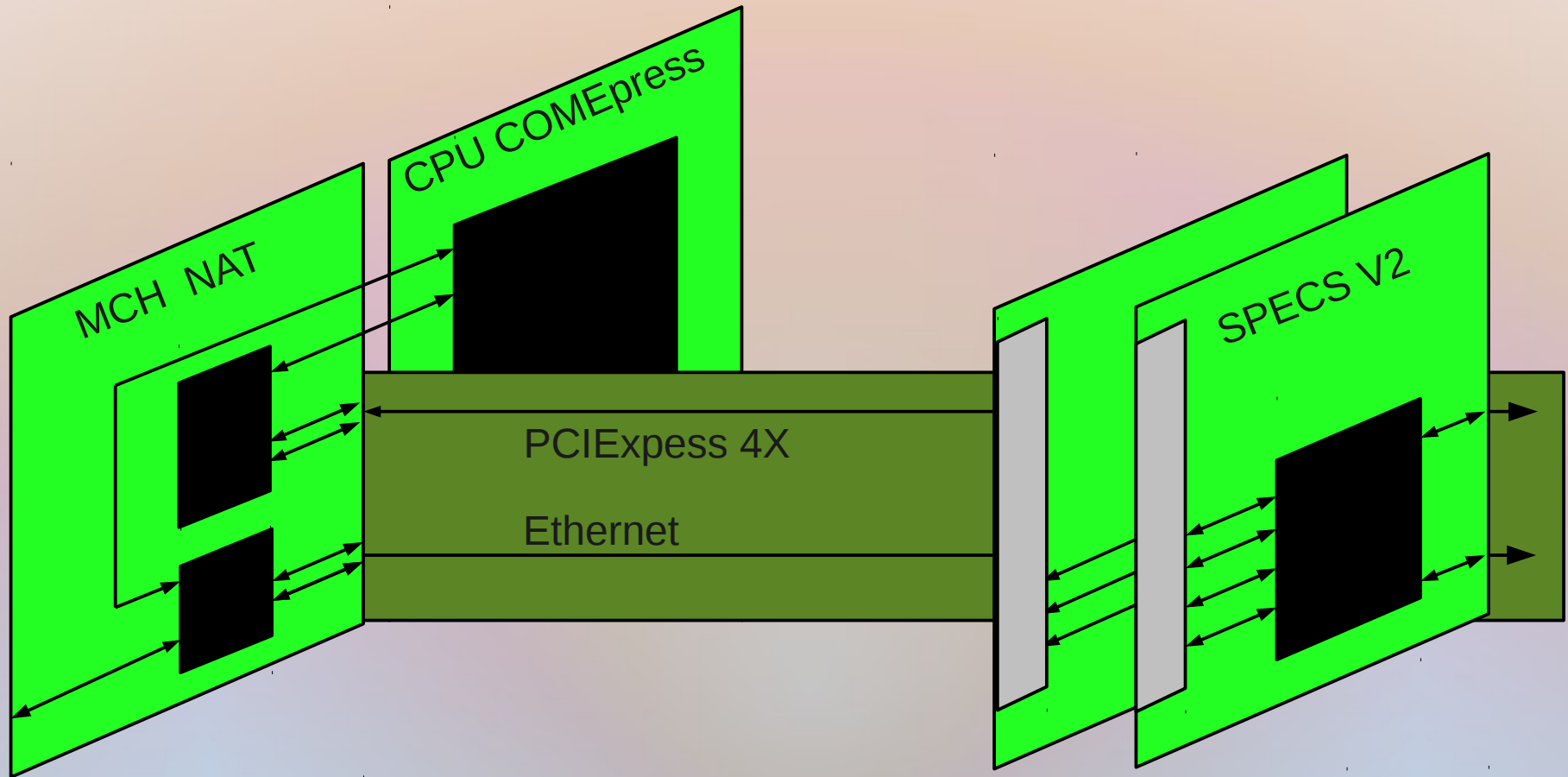
# Caractéristique principale

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- MicroTCA 4.x double-width full size
- Interface
  - PCIExpress Gen 2 4x (hard IP)
  - Ethernet (custom made)
- FPGA ARRIA V GX (5AGXMA1D4F31C5N)
- Configuration
  - Active serial (Quad SPI 128 Mbits)
  - CvP
- SSRAM 18Mbits
- HSMC connector



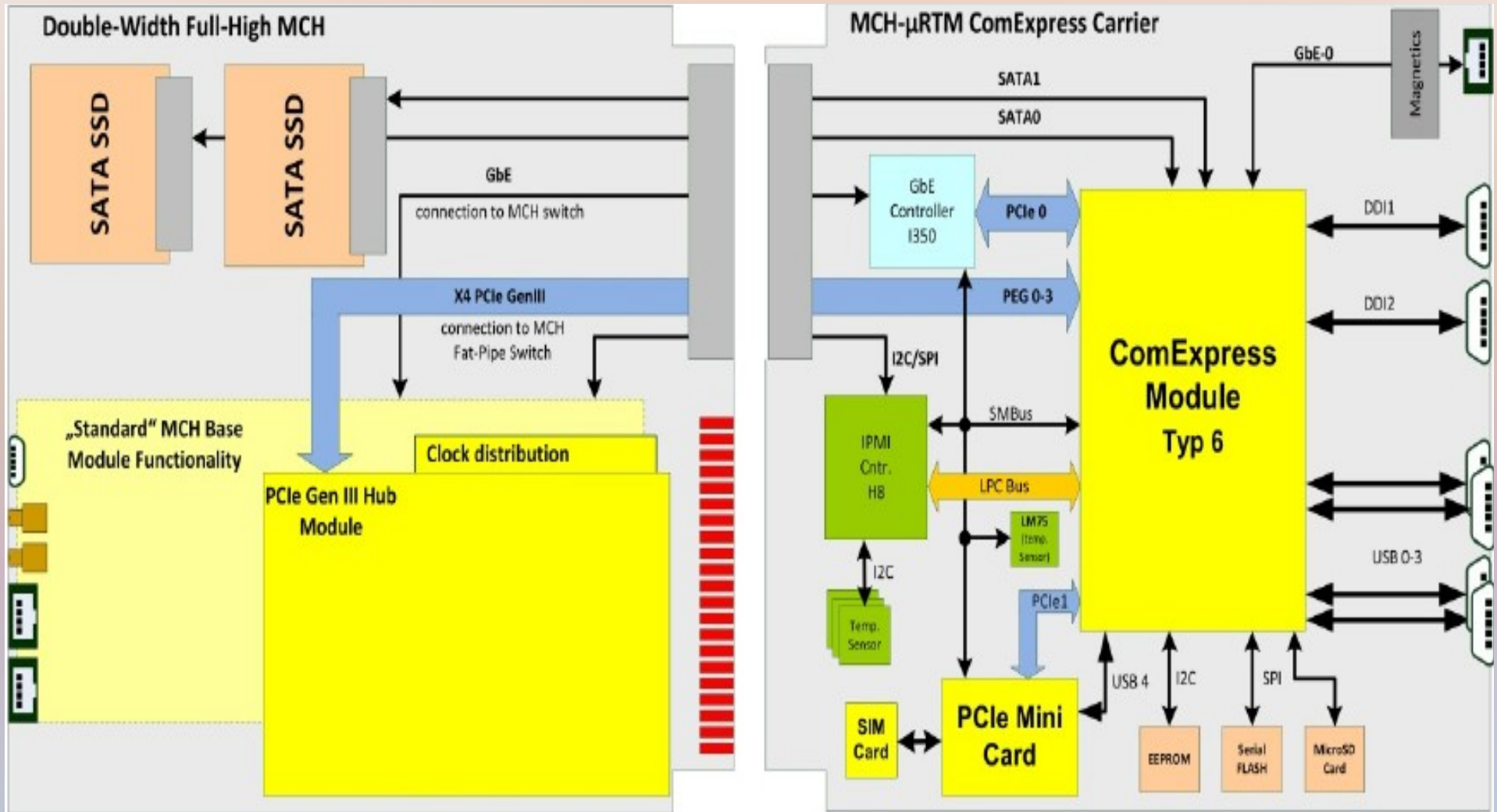
# SPECS V2 Crate







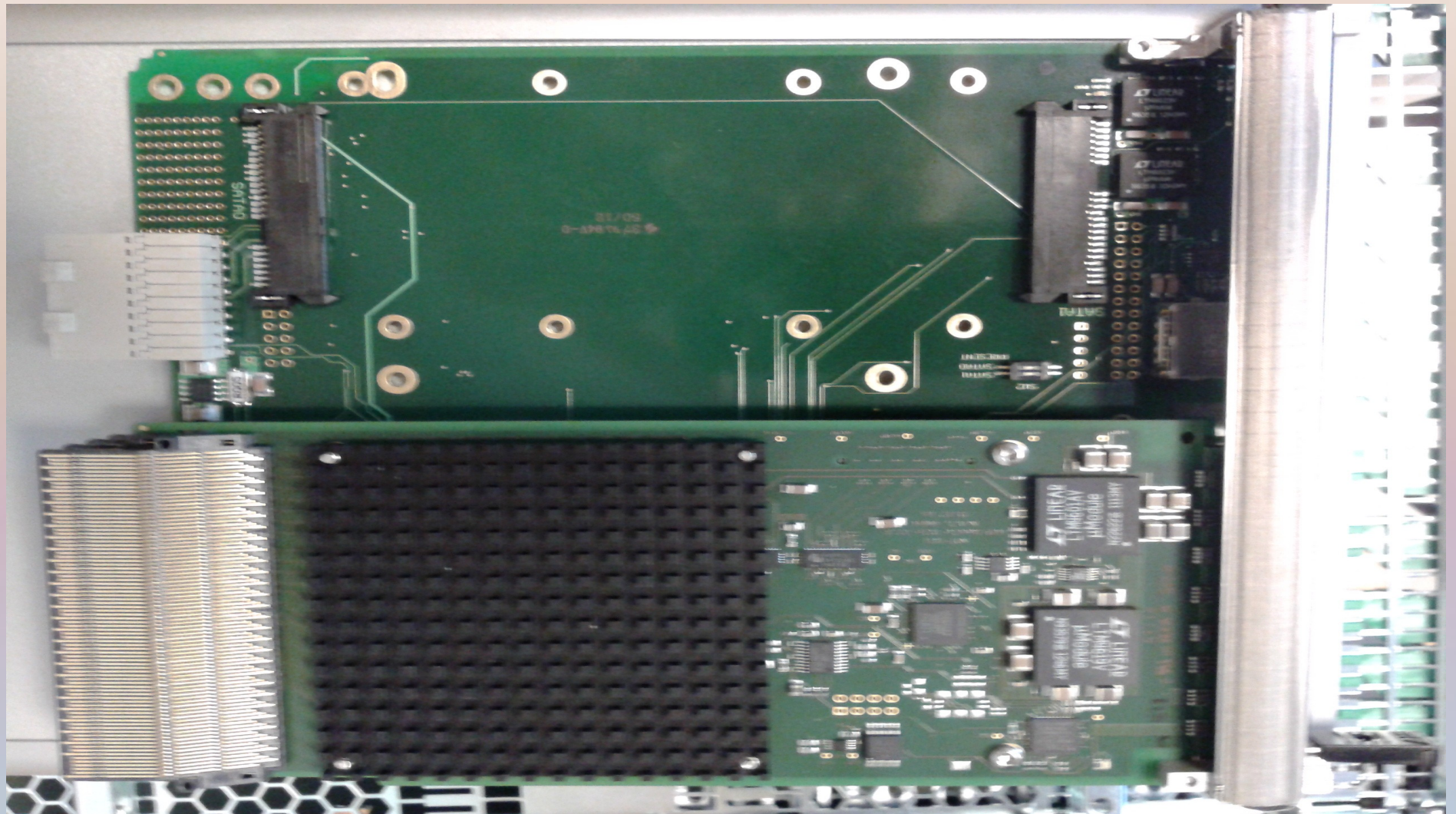
# MCH-CPU





# NAT MCH

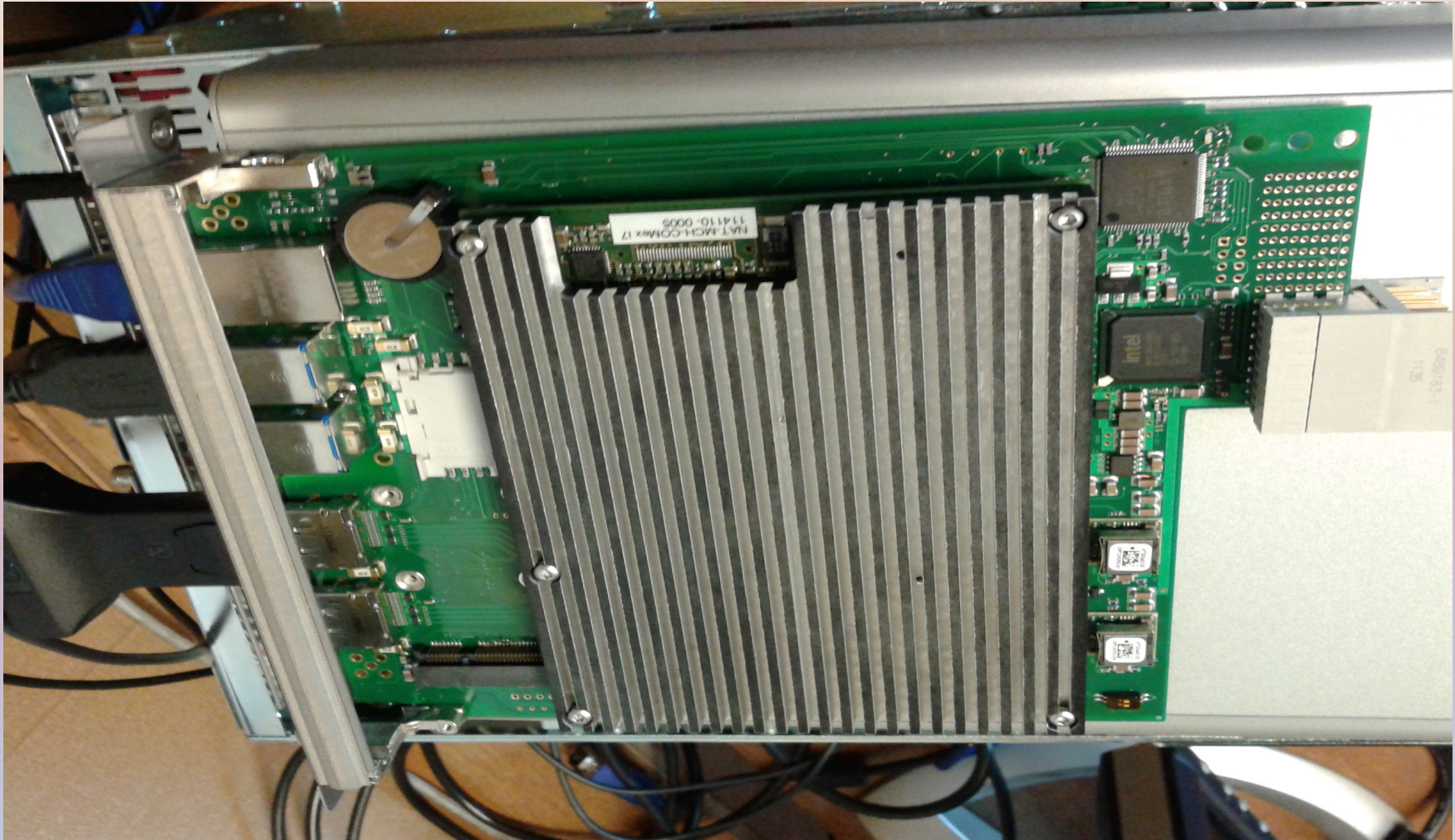
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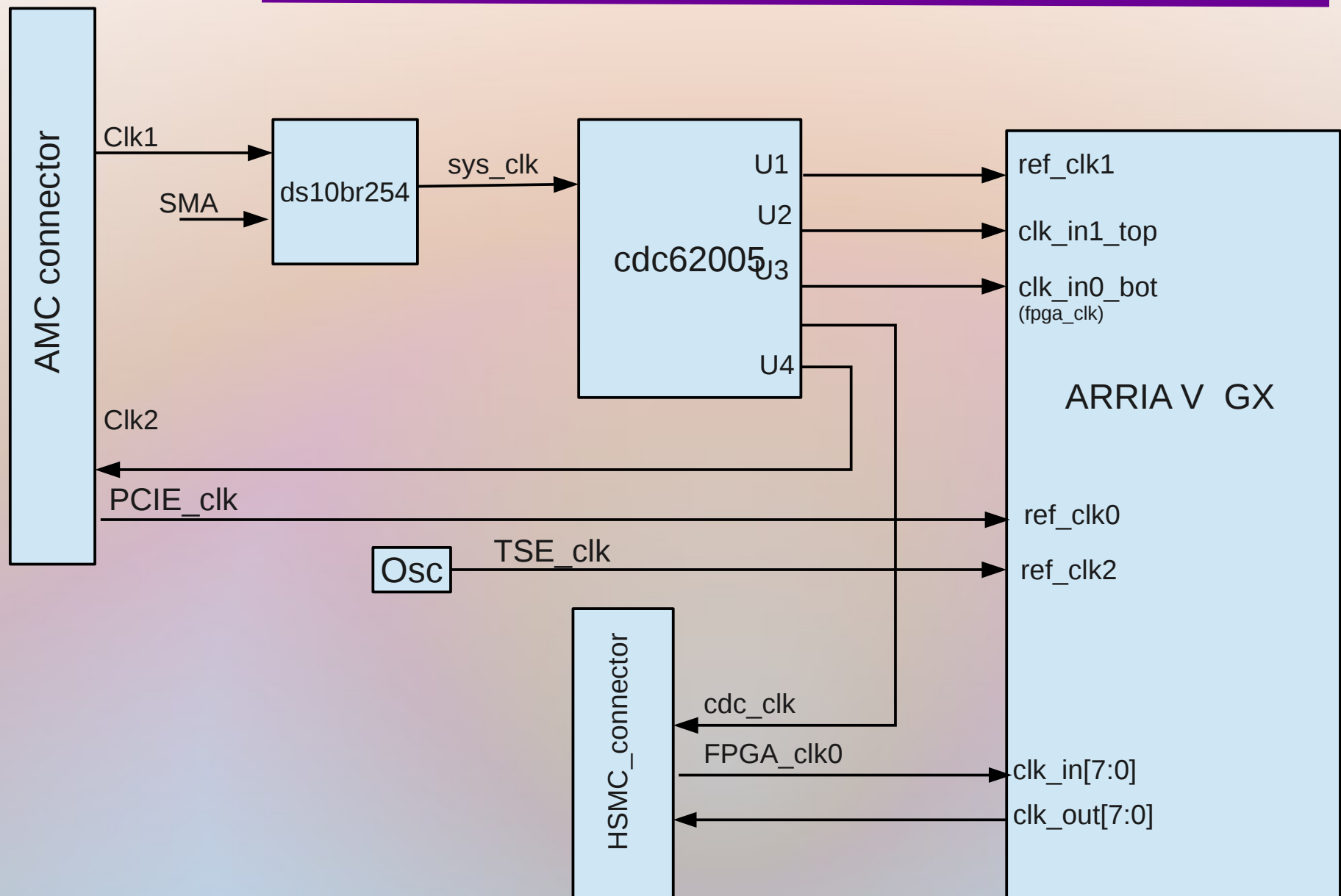


# NAT CPU



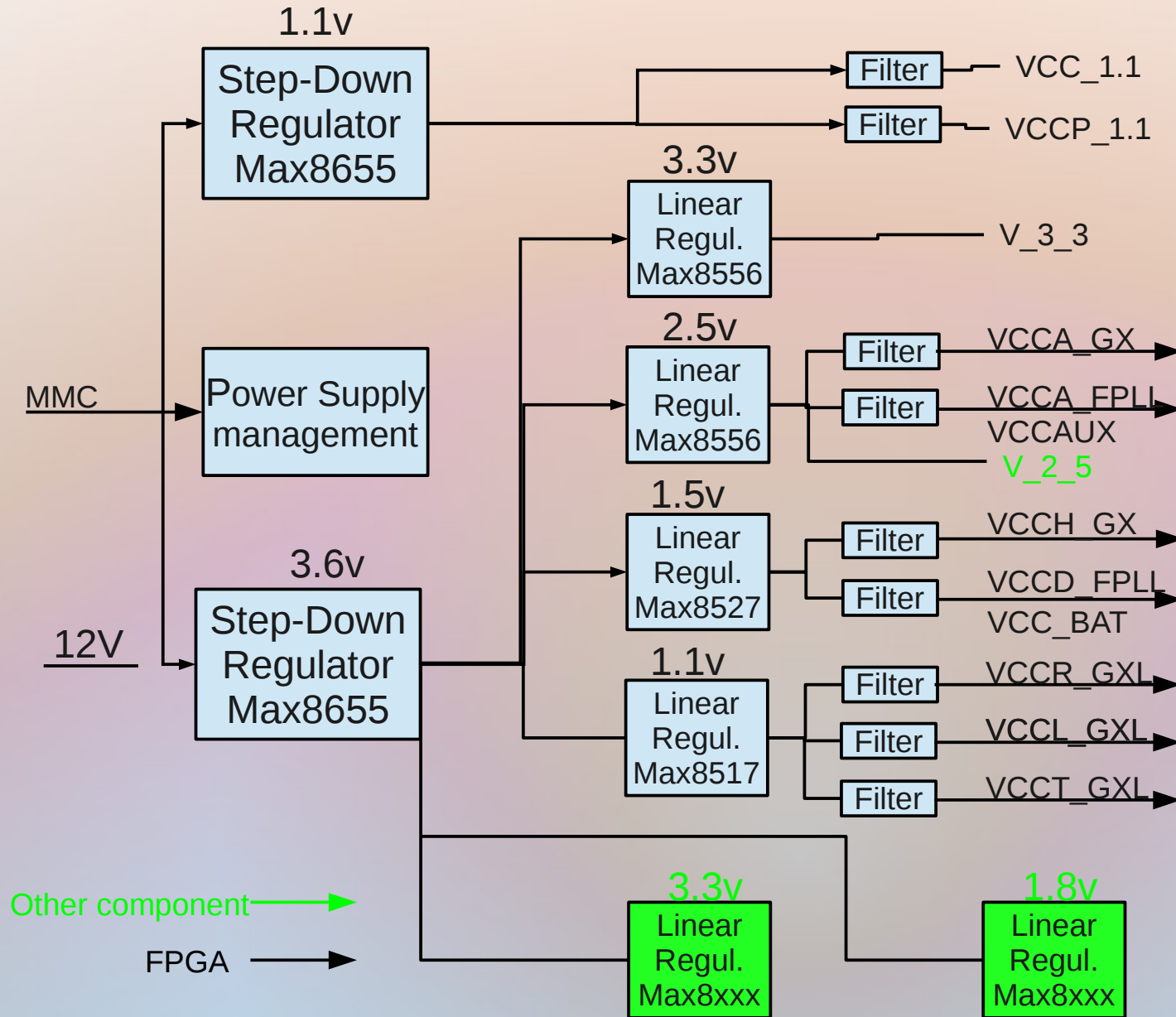


# Clock tree





# Power supply







# FPGASYSPLANNER 2

ns Raccourcis Système

Power Mapping Editor (sur iao.lal.in2p3.fr)

Collapse Sort Ascending Sort Descending Filter Find Cut Copy Paste Show/Hide Columns Reset Width Clear Highlight Refresh Update From CSV Export To CSV Define Regulators Auto Map Regulators Map Regulators Check Connection Reset All Import Reg.

Pin Number	Signal Name	Voltage Level	Regulator Voltage	Regulator Name	Power Filter	External Port	External Net Name
V18	VCC	1.1	1.1	VCC_1_1		<input type="checkbox"/>	
V20	VCC	1.1	1.1	VCC_1_1		<input type="checkbox"/>	
M16	VCCA_FPLL	2.5	2.5	VCCA_FPLL_2_5		<input type="checkbox"/>	
P9	VCCA_FPLL	2.5	2.5	VCCA_FPLL_2_5		<input type="checkbox"/>	
P22	VCCA_FPLL	2.5	2.5	VCCA_FPLL_2_5		<input type="checkbox"/>	
T9	VCCA_FPLL	2.5	2.5	VCCA_FPLL_2_5		<input type="checkbox"/>	
T22	VCCA_FPLL	2.5	2.5	VCCA_FPLL_2_5		<input type="checkbox"/>	
W16	VCCA_FPLL	2.5	2.5	VCCA_FPLL_2_5		<input type="checkbox"/>	
V24	VCCA_GXBL0	2.5	2.5	VCCA_GX_2_5		<input type="checkbox"/>	
P24	VCCA_GXBL1	2.5	2.5	VCCA_GX_2_5		<input type="checkbox"/>	
K26	VCCBAT	1.5	1.5	VCCD_FPLL_BAT_1_5		<input type="checkbox"/>	
M8	VCCD_FPLL	1.5	1.5	VCCD_FPLL_BAT_1_5		<input type="checkbox"/>	
M15	VCCD_FPLL	1.5	1.5	VCCD_FPLL_BAT_1_5		<input type="checkbox"/>	
N22	VCCD_FPLL	1.5	1.5	VCCD_FPLL_BAT_1_5		<input type="checkbox"/>	
V9	VCCD_FPLL	1.5	1.5	VCCD_FPLL_BAT_1_5		<input type="checkbox"/>	
V22	VCCD_FPLL	1.5	1.5	VCCD_FPLL_BAT_1_5		<input type="checkbox"/>	
W15	VCCD_FPLL	1.5	1.5	VCCD_FPLL_BAT_1_5		<input type="checkbox"/>	
T24	VCCD_GXBL0	1.5	1.5	VCCD_GX_1_5		<input type="checkbox"/>	
N25	VCCD_GXBL1	1.5	1.5	VCCD_GX_1_5		<input type="checkbox"/>	
T25	VCCD_GXBL0	1.1	1.1	VCCD_GX_1_1		<input type="checkbox"/>	
T26	VCCD_GXBL0	1.1	1.1	VCCD_GX_1_1		<input type="checkbox"/>	
M25	VCCD_GXBL1	1.1	1.1	VCCD_GX_1_1		<input type="checkbox"/>	
L9	VCCP	1.1	1.1	VCCP_1_1		<input type="checkbox"/>	
L11	VCCP	1.1	1.1	VCCP_1_1		<input type="checkbox"/>	
L15	VCCP	1.1	1.1	VCCP_1_1		<input type="checkbox"/>	
L19	VCCP	1.1	1.1	VCCP_1_1		<input type="checkbox"/>	

OK Cancel Apply

M17

Error

```
successfully.  
: path set to /exp/elec/charlet/LHcb/SpecsPCIE/sfp/specsv2a5.  
/exp/elec/charlet/LHcb/SpecsPCIE/sfp/specsv2a5/specsv2a5.fsp for editing.  
connections...  
: v_2_5(2.5) voltage does not match required voltage 3.3 for pin VCCPD3 ( V21 ) in instance M1.  
: connections check.  
: HSMS_LVCMOS ( part_hsms_lvcmos ) at x=53.07912 mm, y=92.61553 mm.  
: CLOCK_LVDS ( part_clock_lvds ) at x=53.75519 mm, y=104.29509 mm.  
: HSMS_DIFF ( part_hsms_diff ) at x=55.27595 mm, y=115.45114 mm.  
: M1_TRANCEIVER ( part_m1_transceiver ) at x=56.29156 mm, y=131.32166 mm.
```

charlet] [Allegro Design Entry HDL XL : Allegro... [Allegro Design Entry HDL XL : Allegro... [dialcprt.dat (sur iao.lal.in2p3.fr)] (su





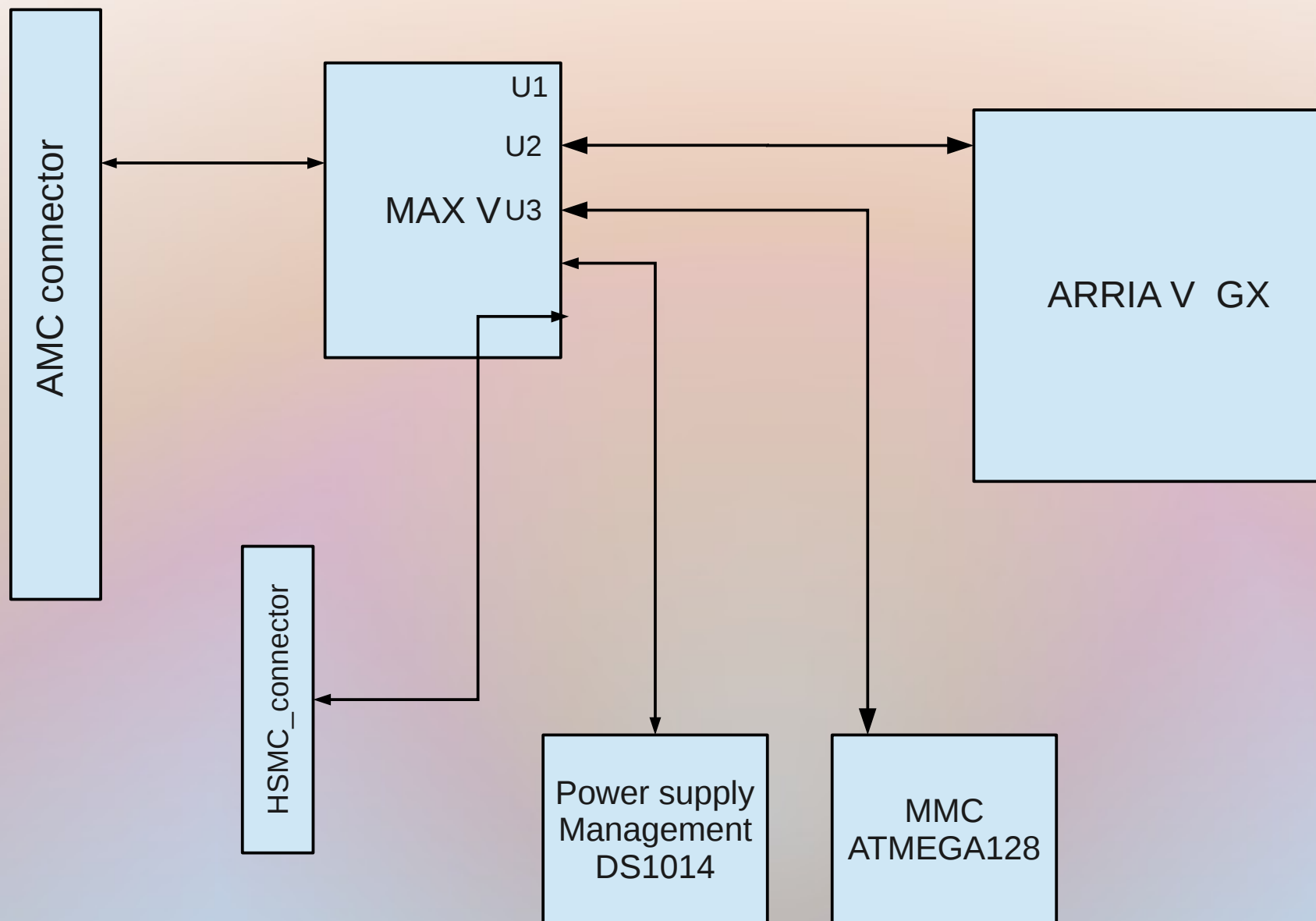
# Conclusion

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- Carte en cour de rootage
- Test courant septembre
- 17 cartes à produire
- Fond de carte double largeur disponible en bibliothèque



# JTAG tree





Completer par:  
Jtag tree  
MMC  
Interface fpgasyplanner  
Architecture FPGA actuelle  
Futur