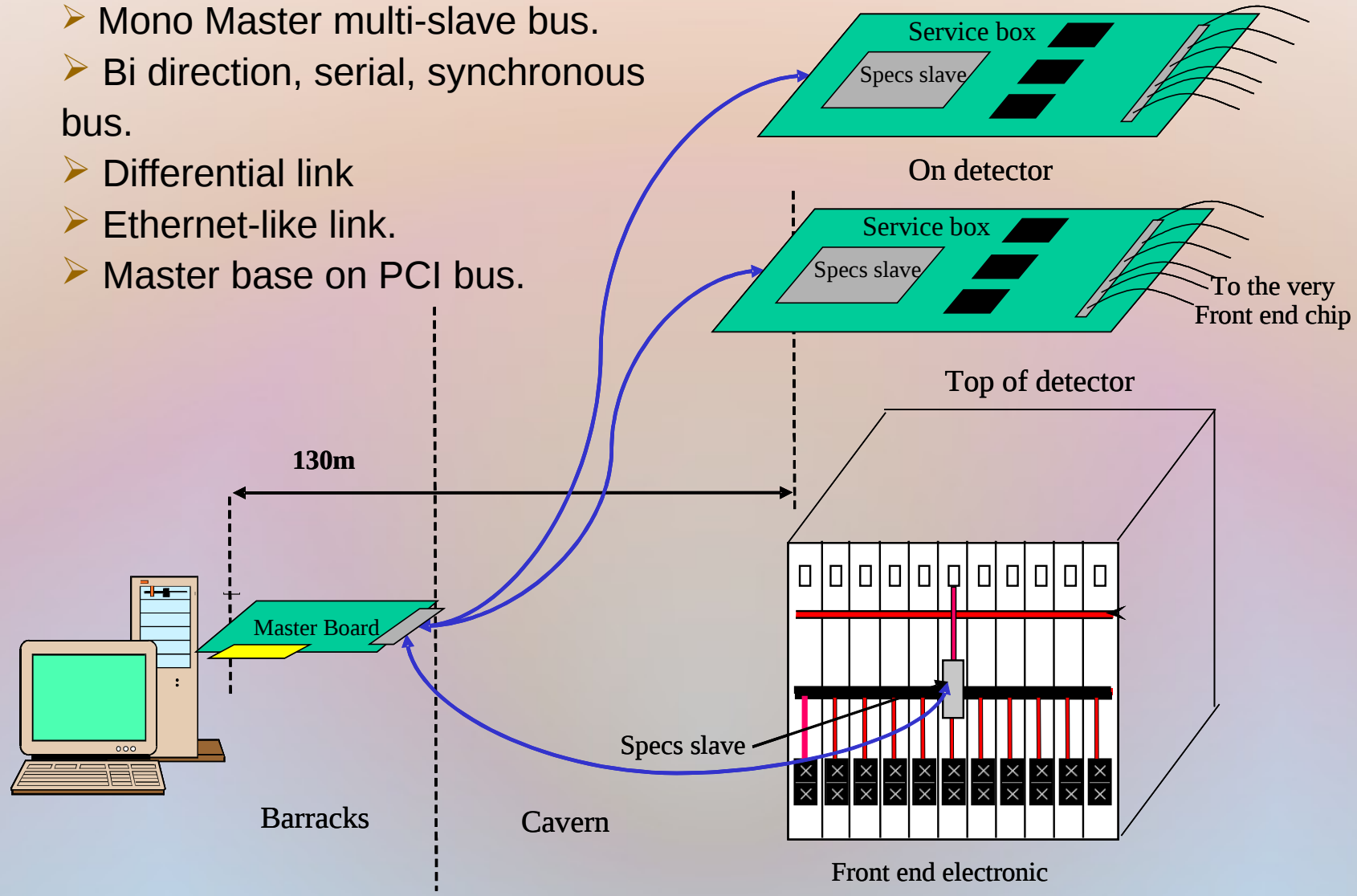
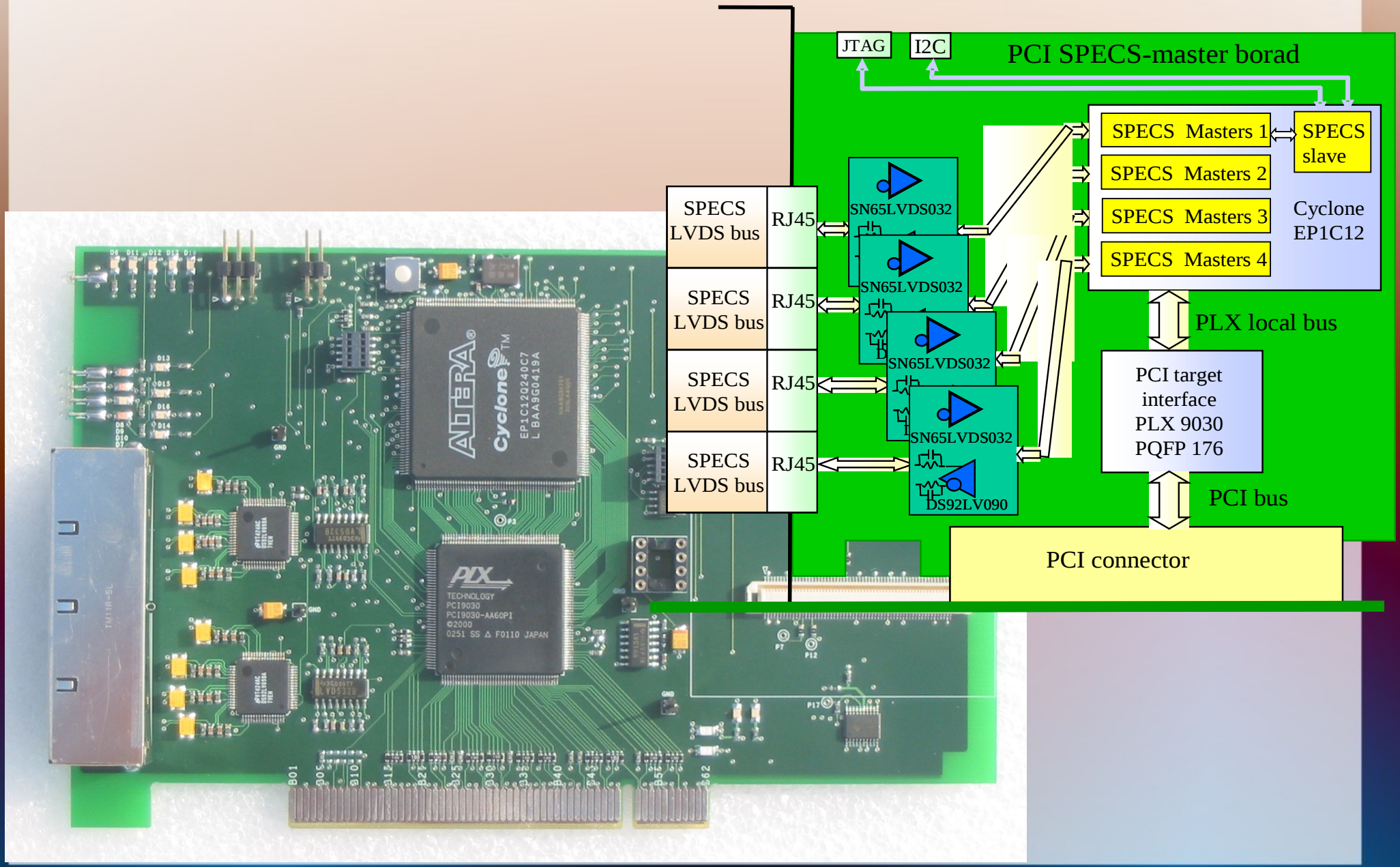
SPECS System

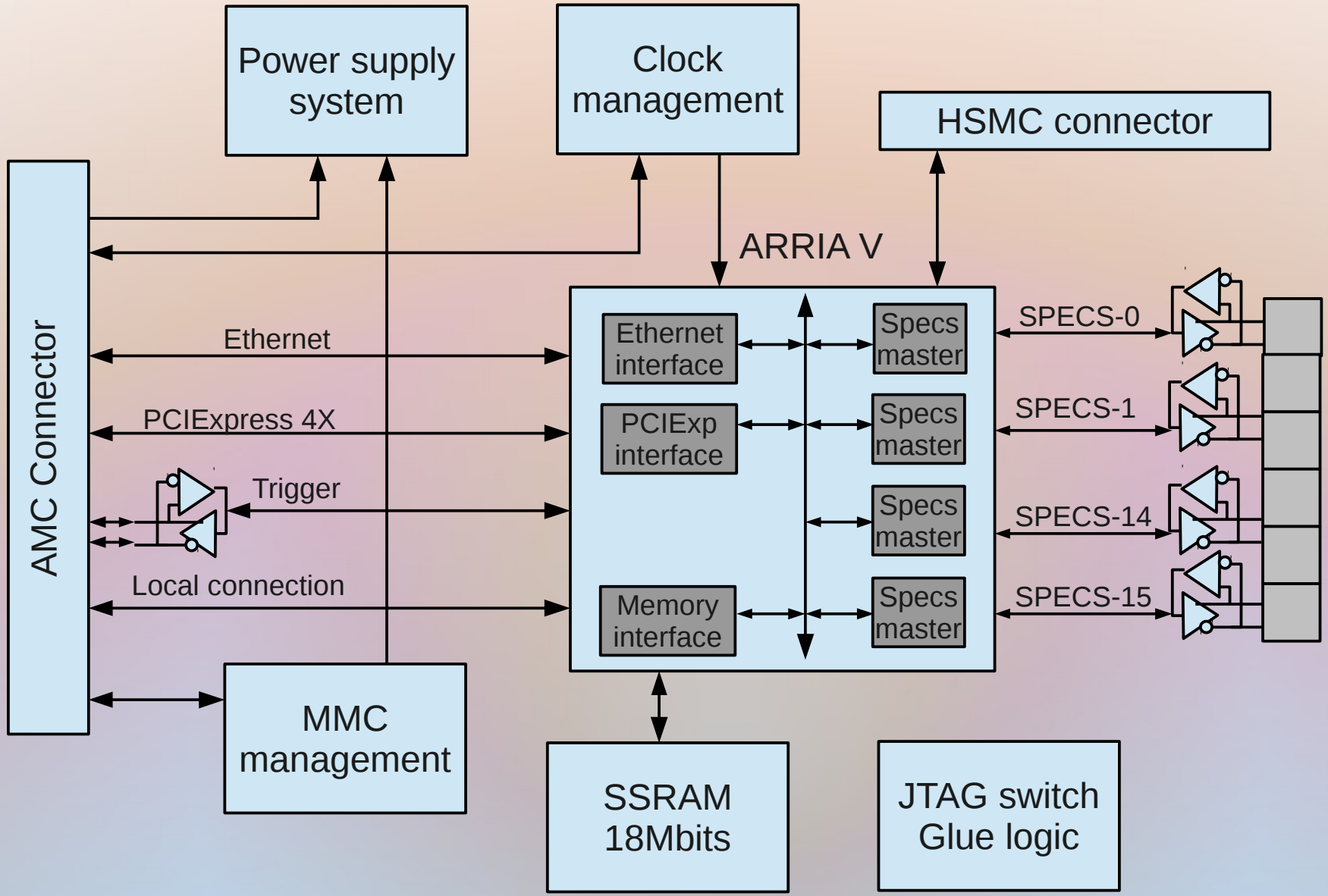
- Mono Master multi-slave bus.
- Bi direction, serial, synchronous bus.
- Differential link
- Ethernet-like link.
- Master base on PCI bus.



SPECS master version 1



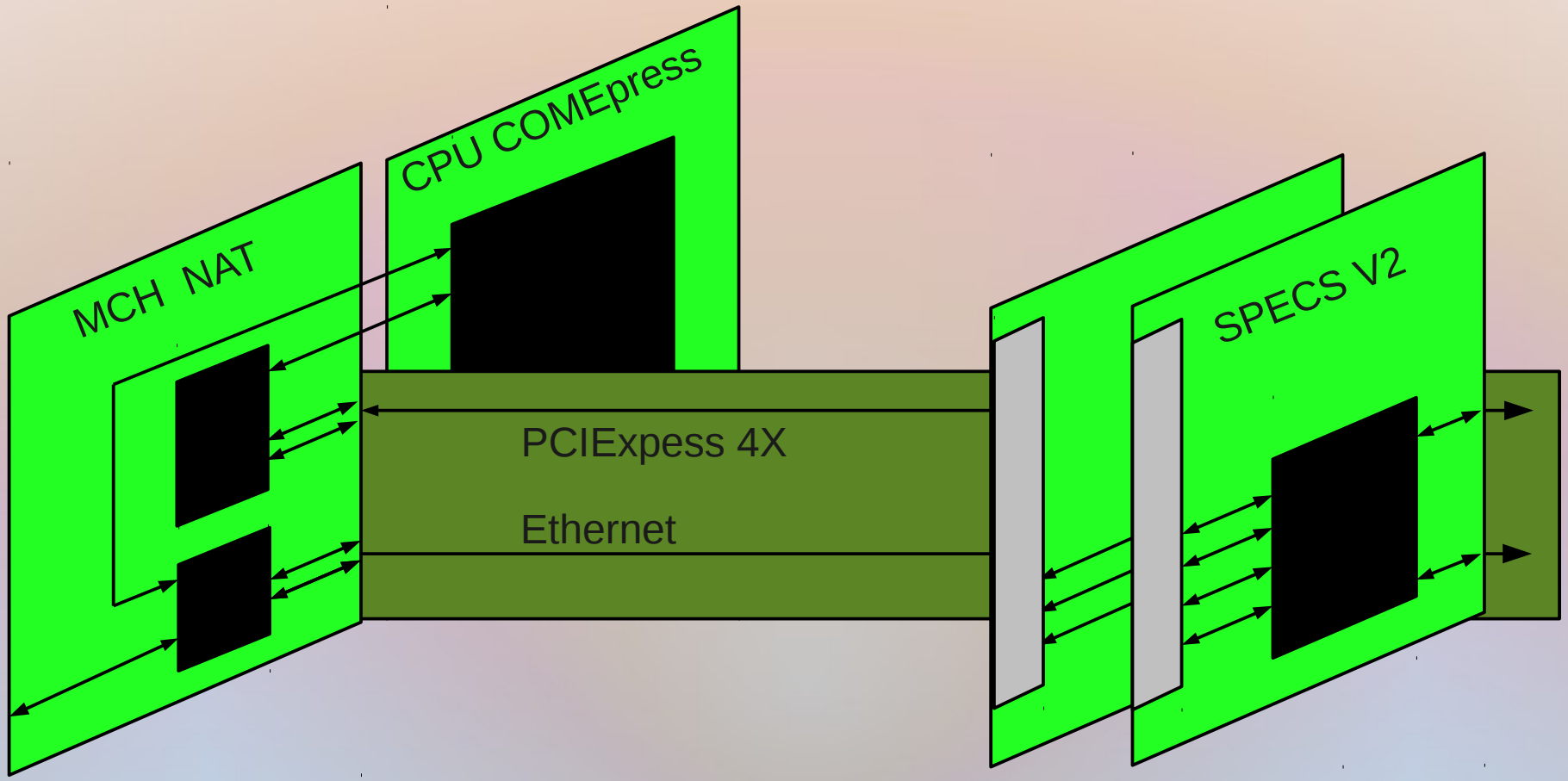
SPECS master version 2

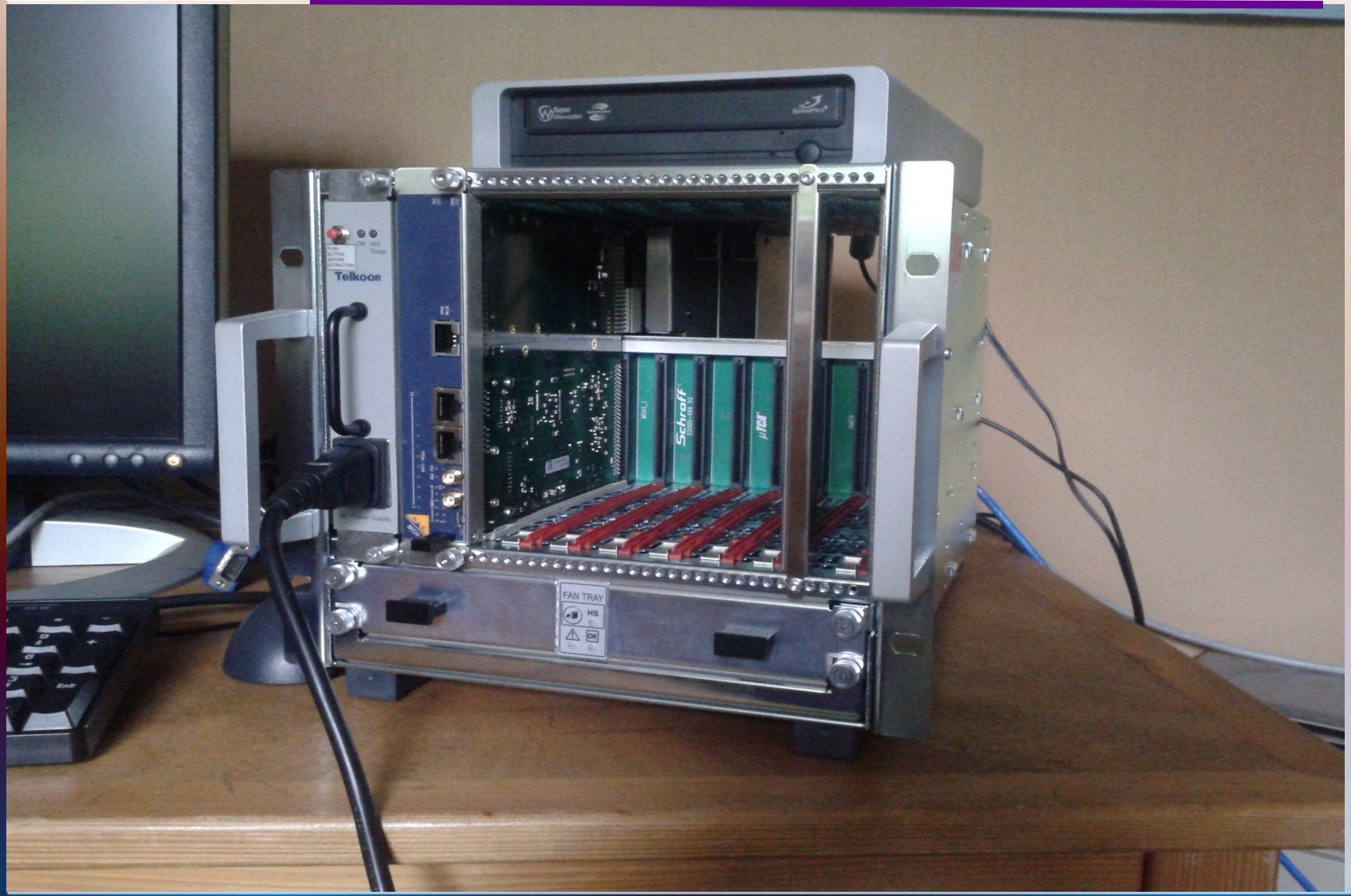


Caractéristique principale

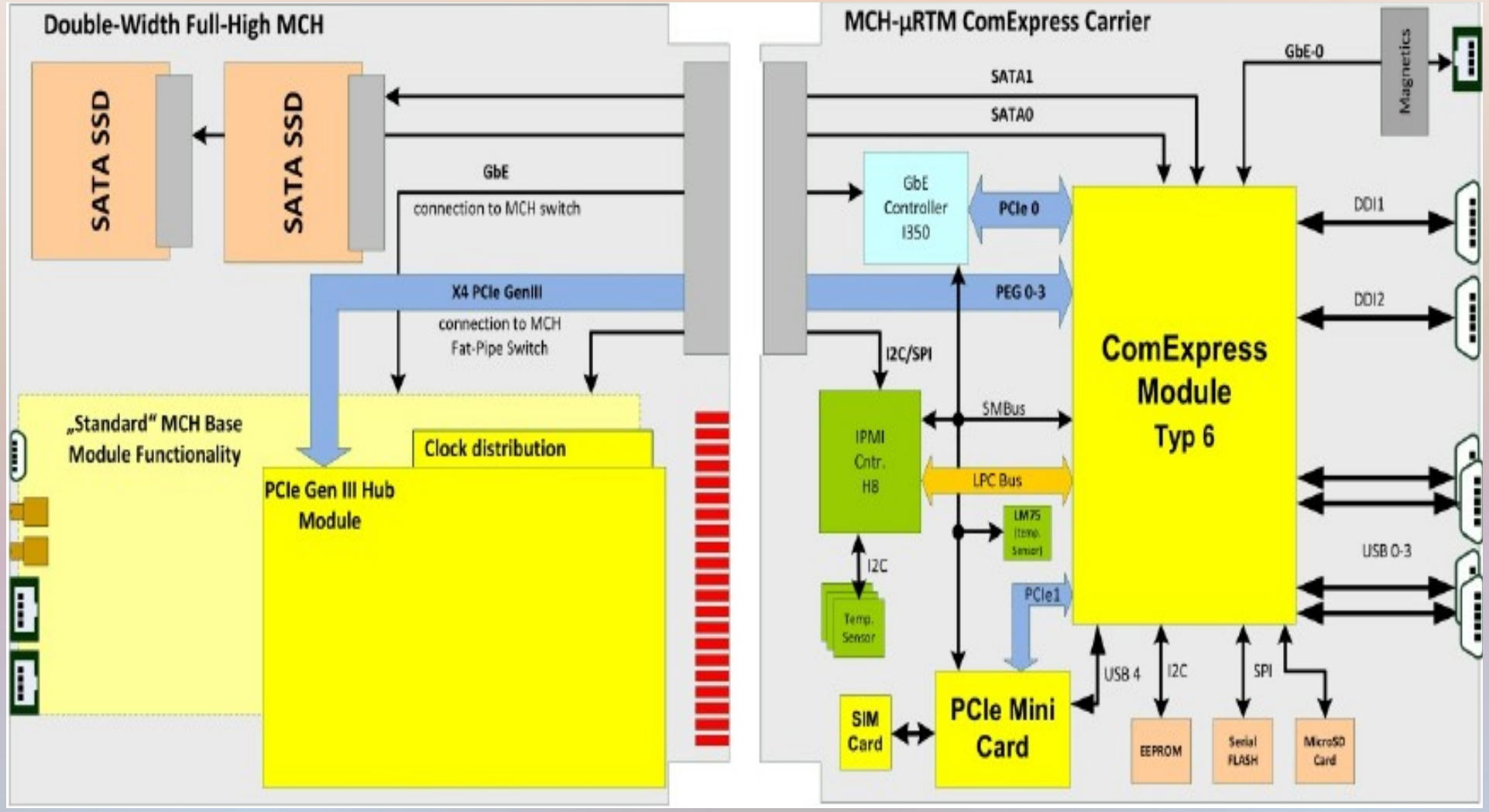
- MicroTCA 4.x double-with full size
- Interface
  - PCIExpress Gen 2 4x (hard IP)
  - Ethernet (custom made)
- FPGA ARRIA V GX (5AGXMA1D4F31C5N)
- Configuration
  - Active serial (Quad SPI 128 Mbits)
  - CvP
- SSRAM 18Mbits
- HSMC connector

SPECS V2 Crate

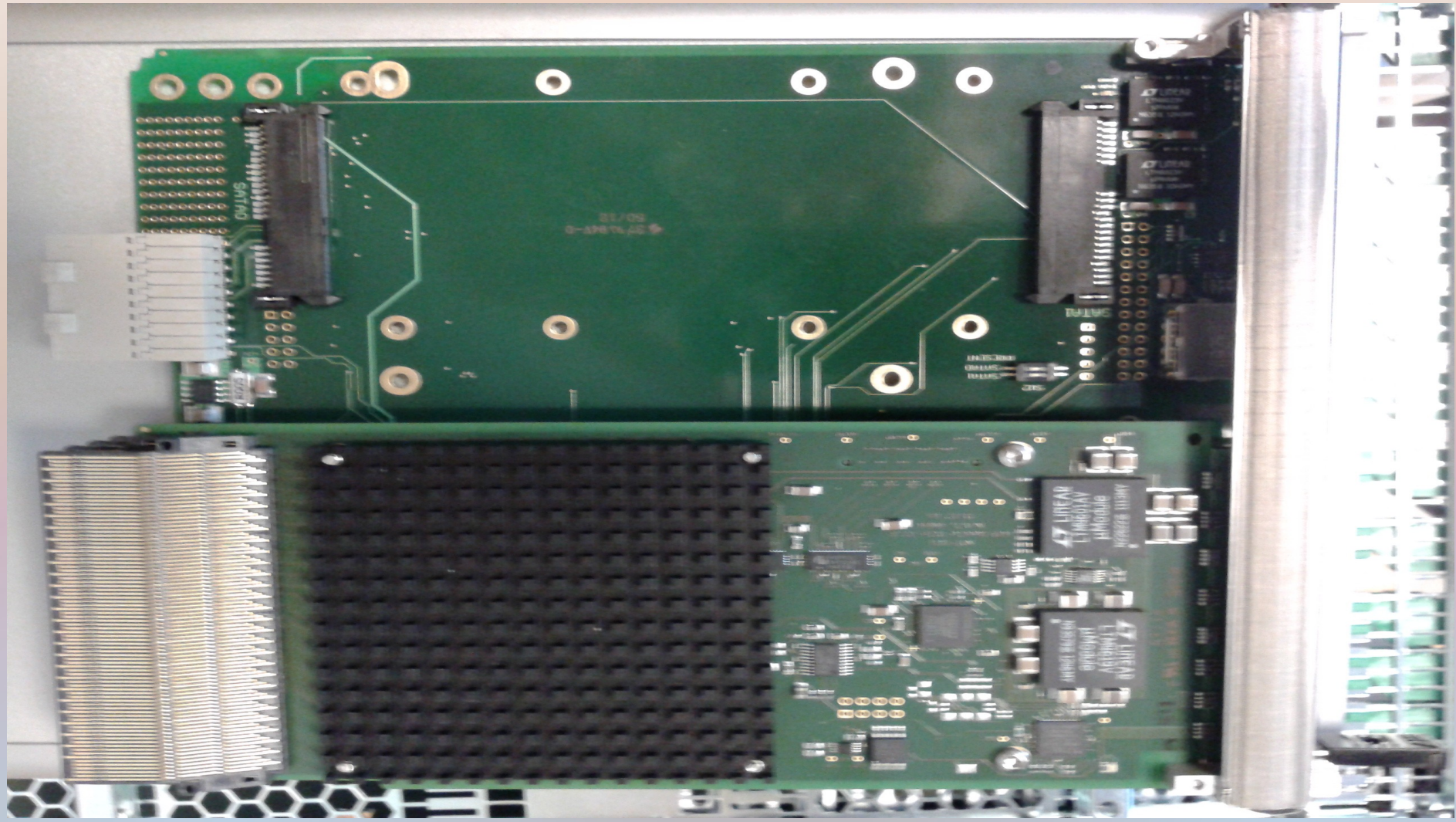



Telkoor
Schroff
µTCA
FAN TRAY
HS
OK

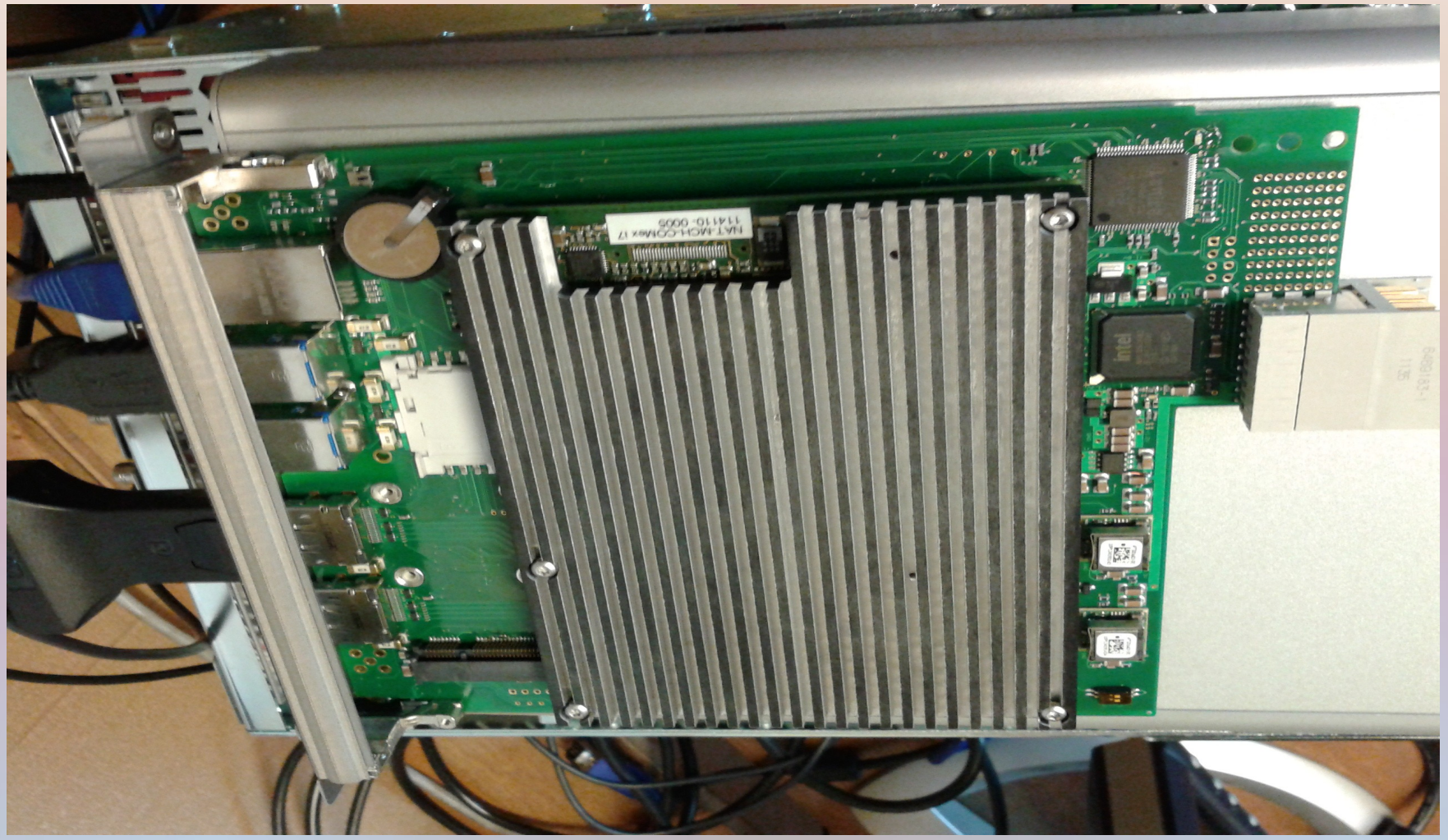
MCH-CPU


Double-Width Full-High MCH
SATA SSD
SATA SSD
GbE
connection to MCH switch
X4 PCIe GenIII
connection to MCH
Fat-Pipe Switch
„Standard" MCH Base
Module Functionality
Clock distribution
PCIe Gen III Hub
Module
MCH-µRTM ComExpress Carrier
SATA1
SATA0
GbE-0
Magnetics
GbE
Controller
I350
PCIe 0
PEG 0-3
I2C/SPI
SMBus
IPMI
Cntr.
H8
LPC Bus
LM75
(temp.
Sensor)
I2C
Temp.
Sensor
PCIe1
ComExpress
Module
Typ 6
DDI1
DDI2
USB 0-3
USB 4
I2C
SPI
SIM
Card
PCIe Mini
Card
EEPROM
Serial
FLASH
MicroSD
Card

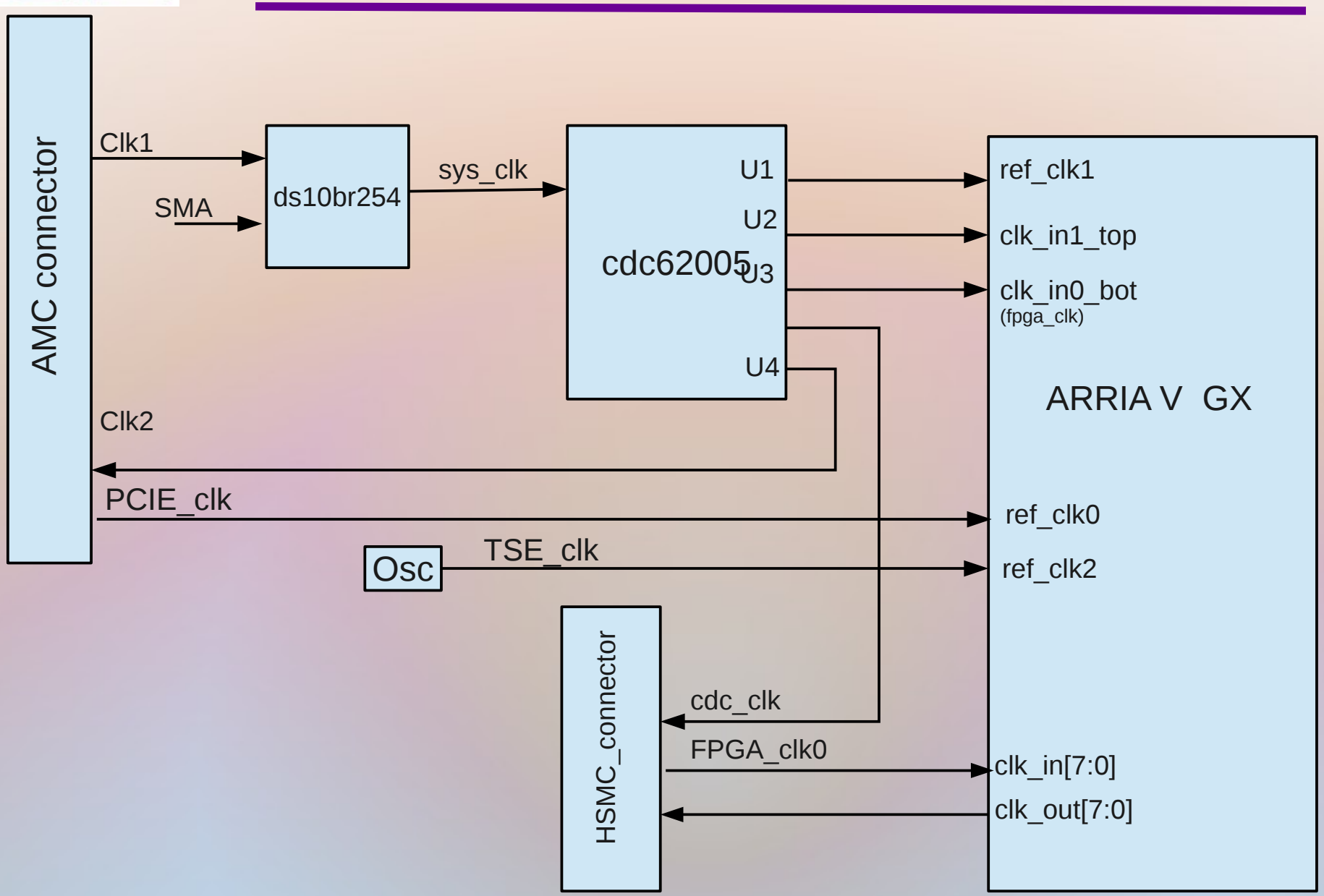
NAT MCH



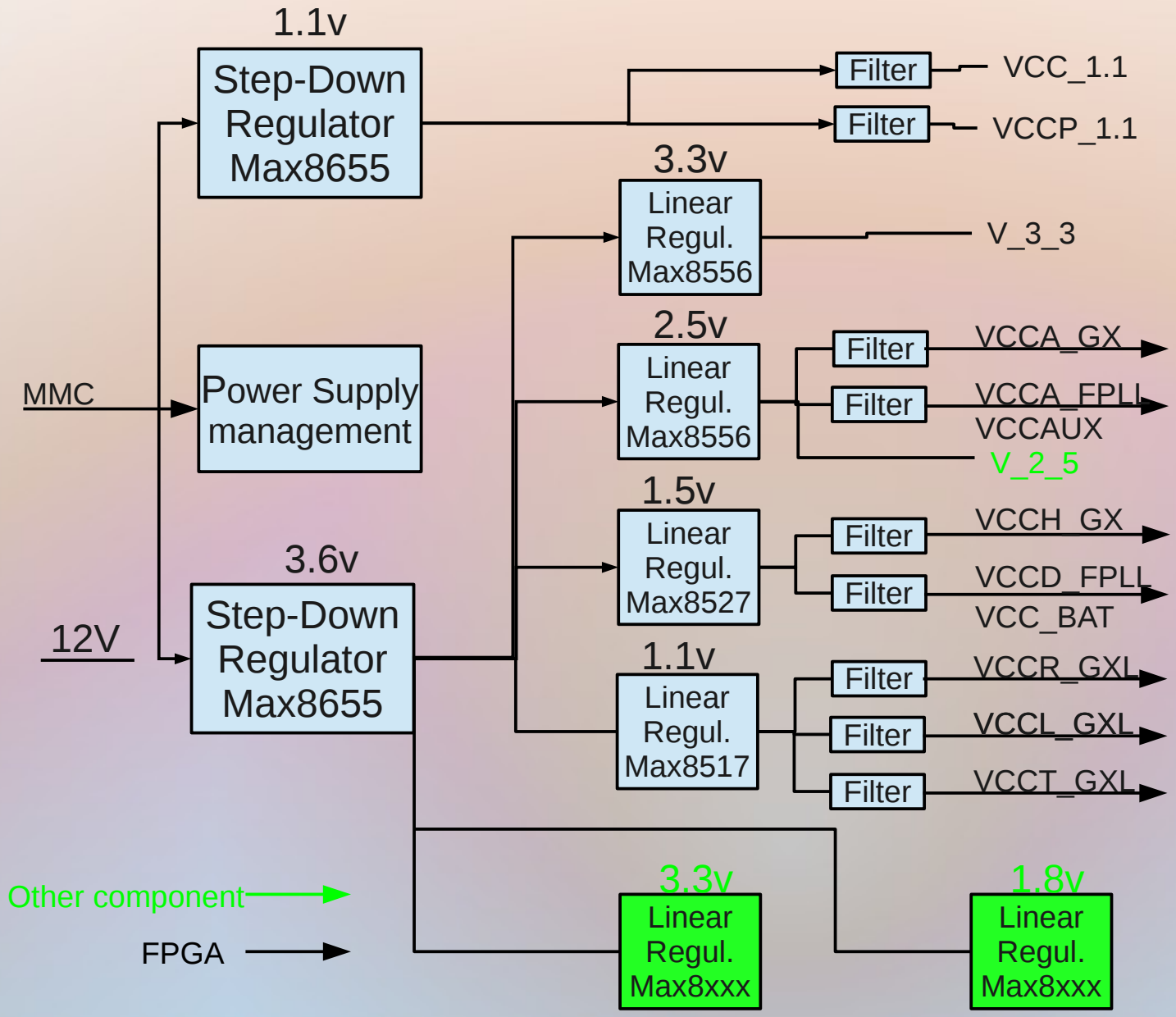
NAT CPU



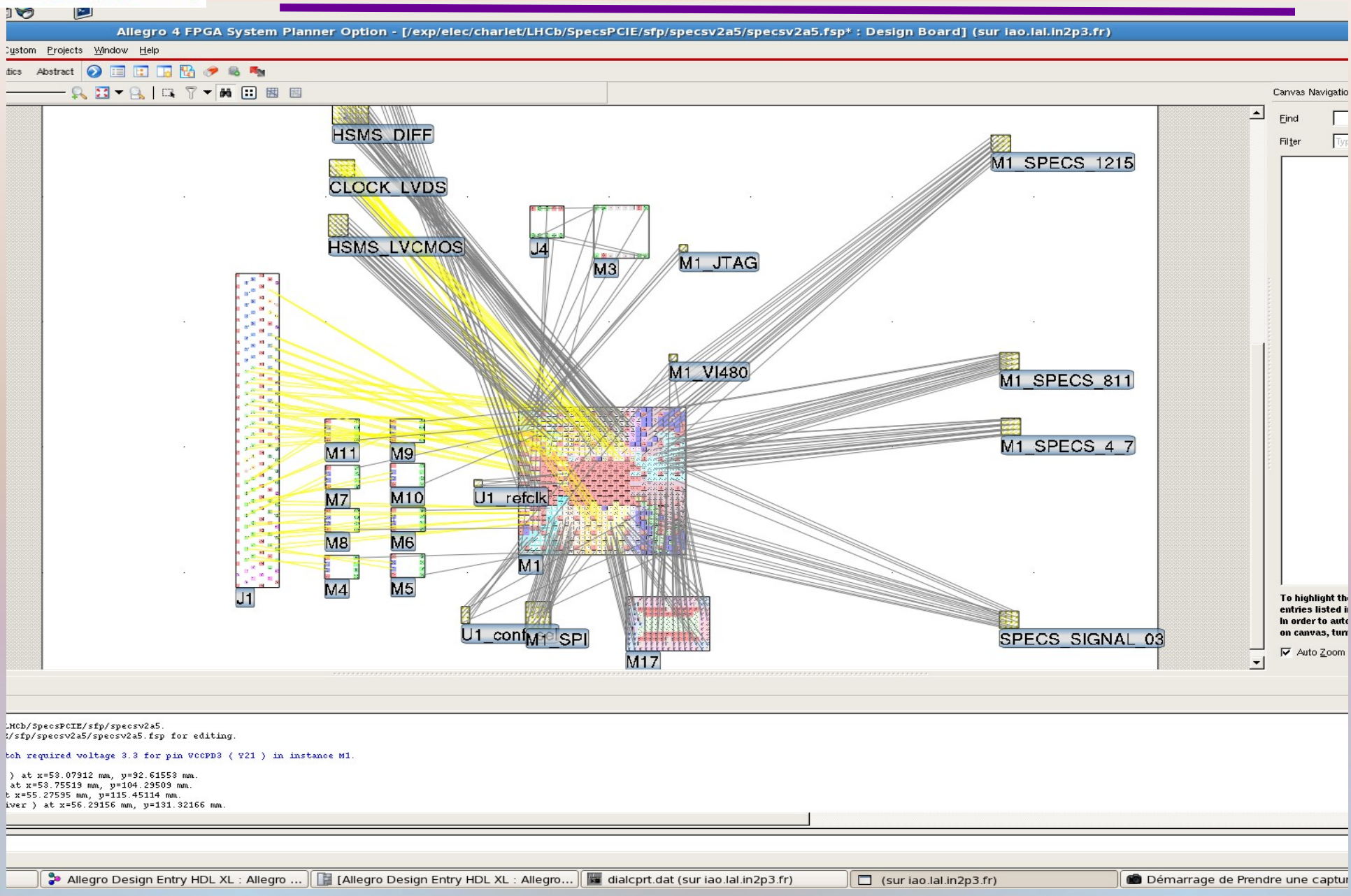
Clock tree


AMC connector
Clk1
SMA
ds10br254
sys_clk
cdc62005
U1
U2
U3
U4
ref_clk1
clk_in1_top
clk_in0_bot
(fpga_clk)
ARRIA V GX
Clk2
PCIE_clk
ref_clk0
Osc
TSE_clk
ref_clk2
HSMC_connector
cdc_clk
FPGA_clk0
clk_in[7:0]
clk_out[7:0]

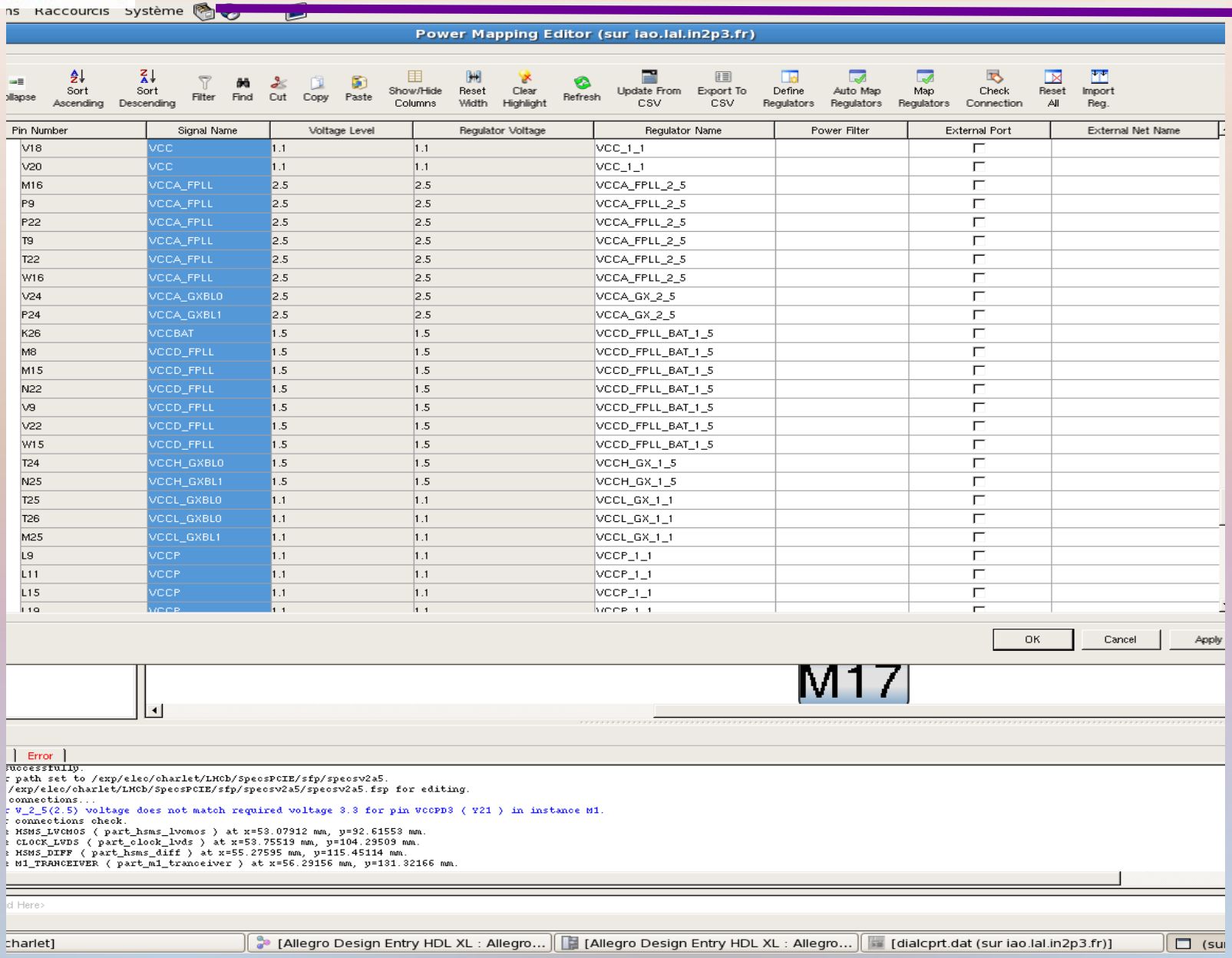
Power supply



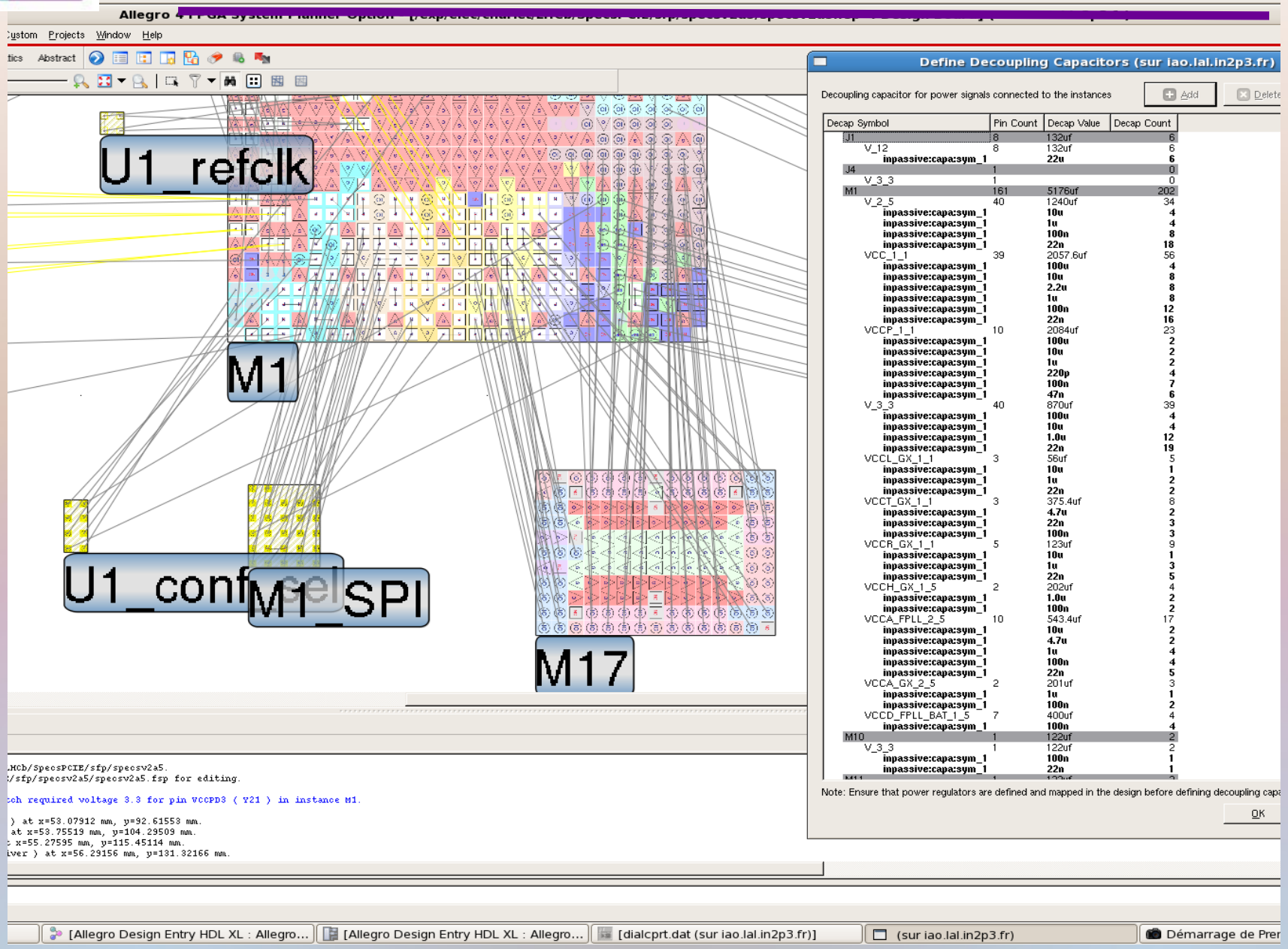
FPGASYSPLANNER 1



FPGASYSPLANNER 2



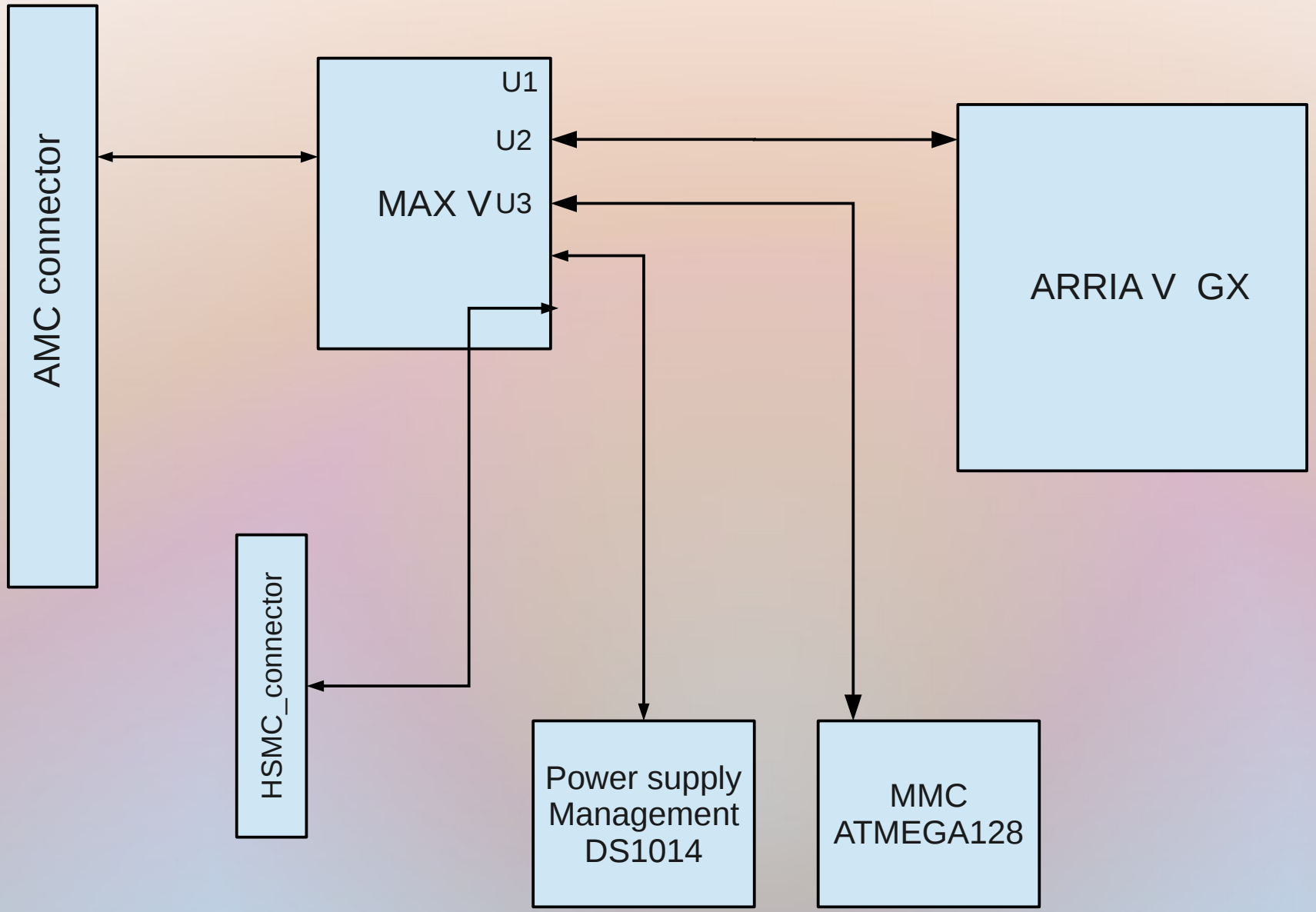
FPGASYSPLANNER 3



Conclusion

- Carte en cour de rootage
- Test courant septembre
- 17 cartes à produire
- Fond de carte double largeur disponible en bibliothèque

JTAG tree


AMC connector
U1
U2
MAX V U3
ARRIA V GX
HSMC_connector
Power supply
Management
DS1014
MMC
ATMEGA128

Completer par:

- Jtag tree
- MMC
- Interface fpgasyplanner
- Architecture FPGA actuelle
- Futur