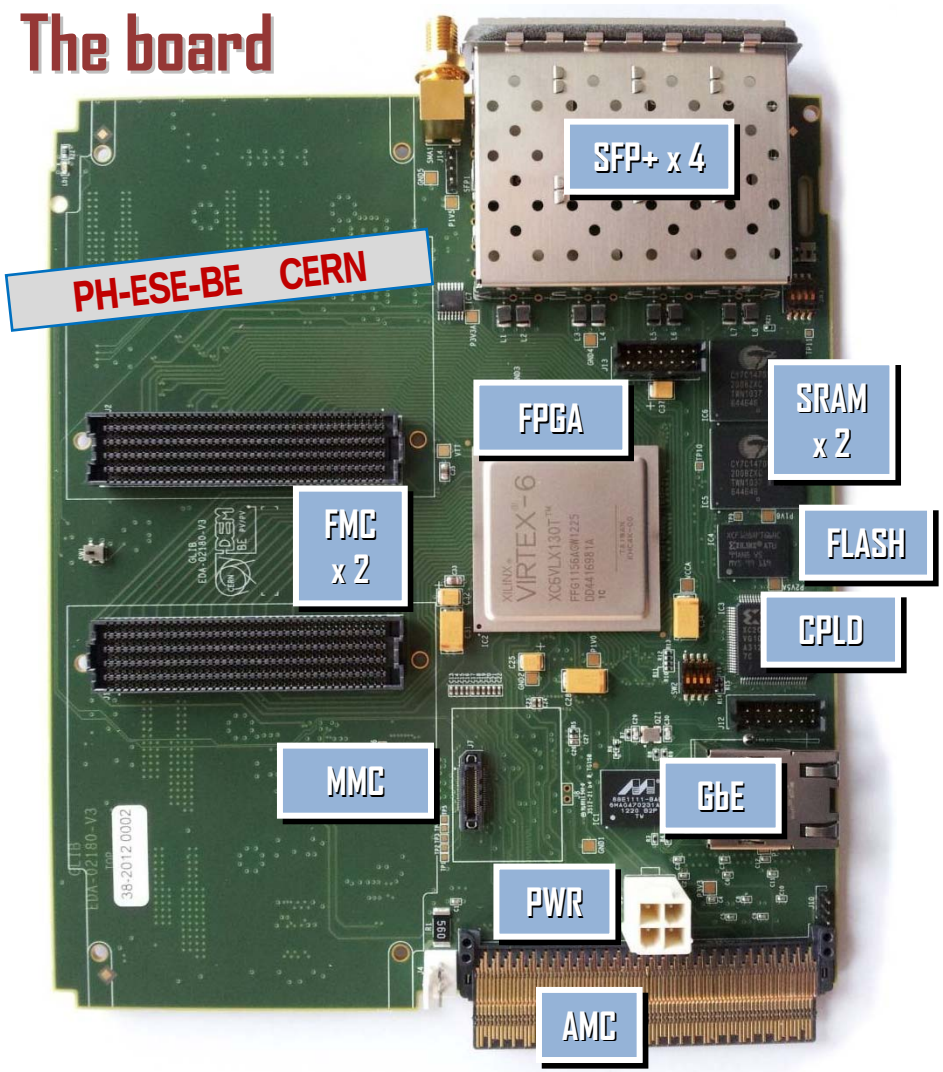
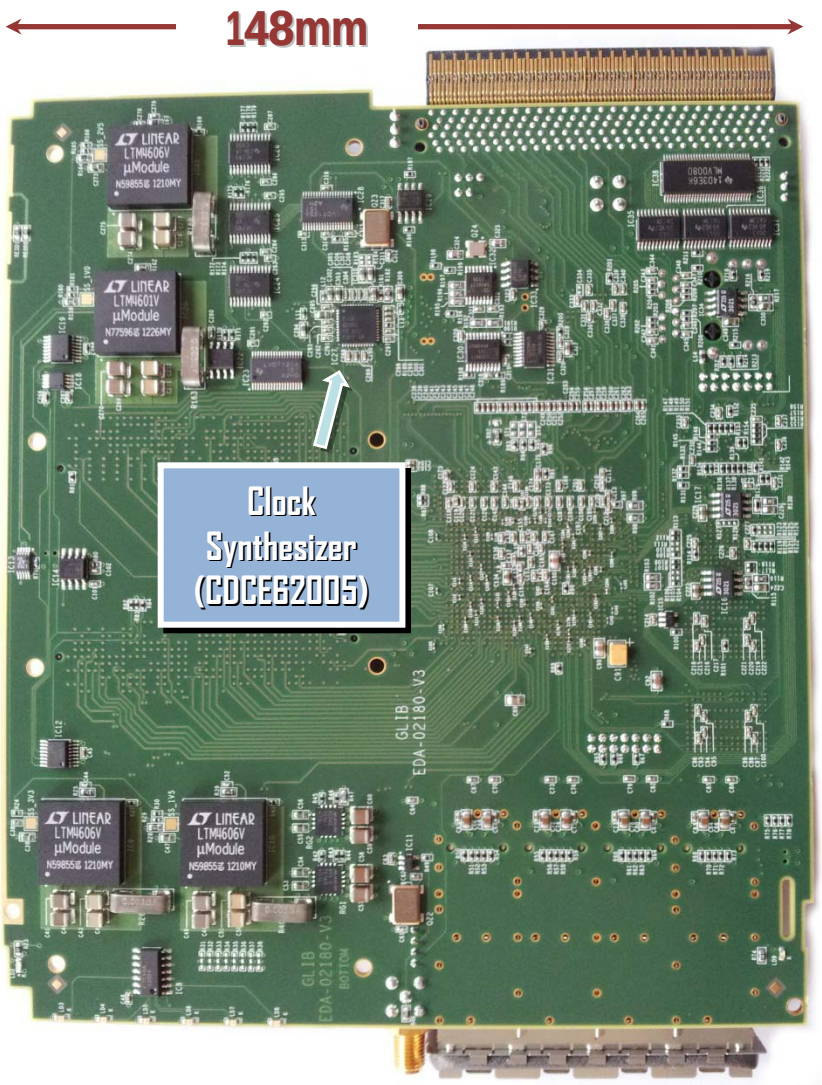

Un aperçu du µTCA à l'IPHC
projet CMS Tracker Upgrade

Glib : Gigabit Link Interface Board

PH-ESE-BE

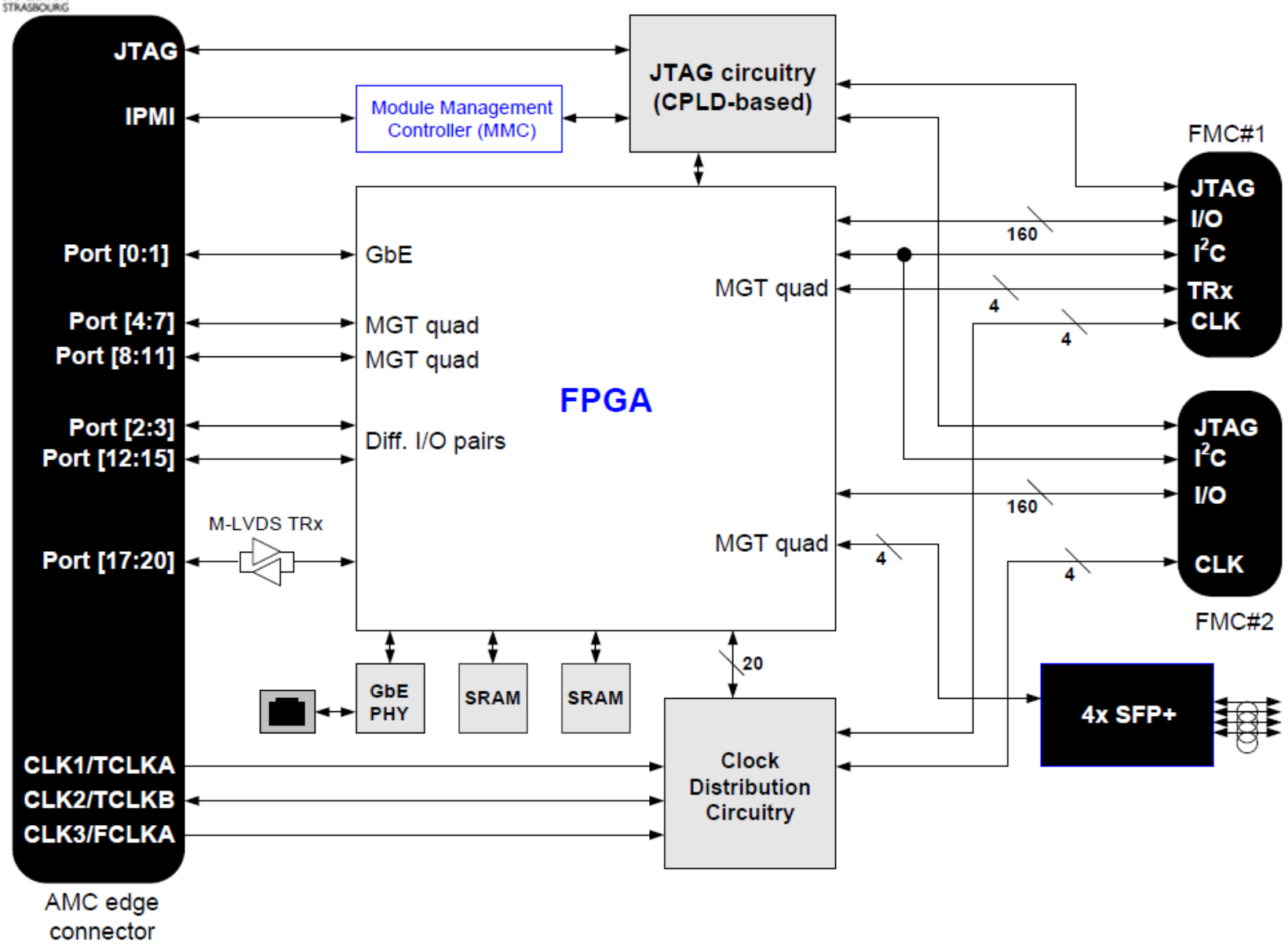
The board





Courtesy of P.Vichoudis

ARCHITECTURE



INTERFACES

Optical

- Four SFP+ cages

AMC

- Port [0-1]: GbE.
- Port [4-7] (Fat Pipe): PCIe x4 GEN2. Possibility to implement other protocols.
- Port [8-11] (Extended Fat Pipe): PCIe x4 GEN2. Possibility to implement other protocols.
- Port [2:3]: LVDS I/O pairs. Possibility to implement other differential I/O standards.
- Port [12-15]: LVDS I/O pairs. Possibility to implement other differential I/O standards.
- Port [17-20]: M-LVDS.
- CLK1/TCLKA: M-LVDS clock input.
- CLK2/TCLKB: M-LVDS clock input/output.
- CLK3/FCLKA: HCSL/M-LVDS clock input.

INTERFACES

FMC

- 2 High-pin count (HPC) sockets
- 160 user-specific I/Os (single-ended or differential pairs)
- 2 differential clock inputs and 2 differential clock outputs.
- The primary FMC is accessible from the front panel
- The primary FMC also provides four optional 6.5Gbps transceiver lines.

PC (only in bench-top operation)

- GbE RJ45 socket (1000BASE-T).
- PCIe 4x GEN2 adapter board.
- Possibility to implement additional PC interfaces on the FMC mezzanines.

FPGA – RAM & MMC

XILINX Virtex-6 LXT FPGA (VLX130T-1FF1156C)

- 600 I/O that can be configured to various differential or single-ended standards.
- Single-ended I/O data rates of up to 800Mbps.

On-board memory

- Two 72Mb (2M x 36bit) SRAM devices (CY7C1470 by Cypress)
- Operating frequency at up to 250MHz.
- Upgradeable up to 1.125Gb (once available)

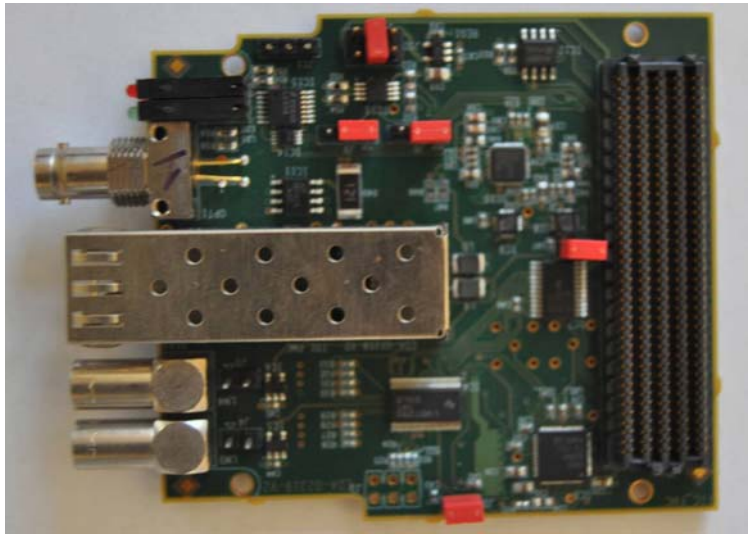
Module Management Controller (MMC)

- Implements the Intelligent Platform Management Interface (IPMI) for the AMC initialization and monitoring in μTCA environment.
- Mezzanine card based on an ATMEL microcontroller.
- Developed by CPPM, IN2P3-CNRS & Univ. Aix-Marseille II for LHCb.
- Dimensions: 39mm x 20mm x 10mm.

FMC standard strength : choice of mezzanines

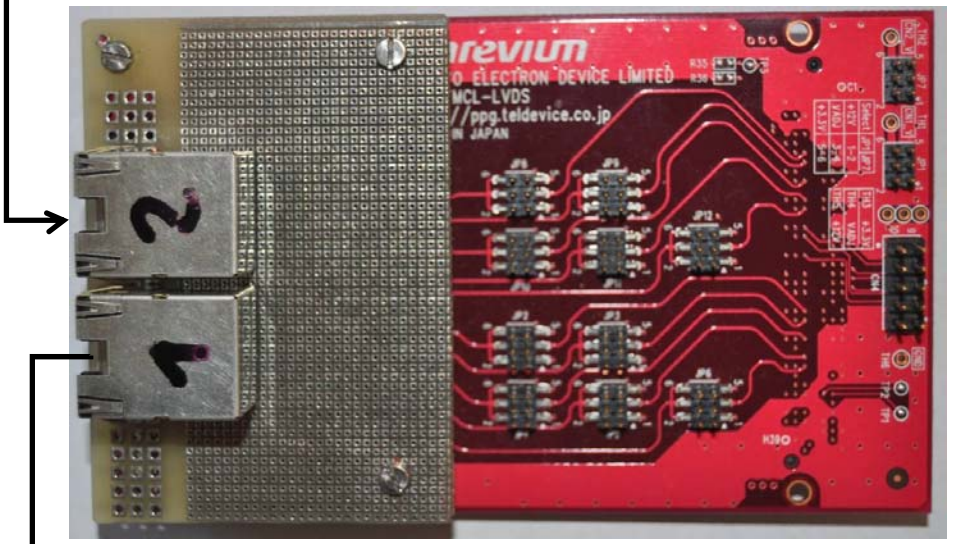
- As an example, for a CMS-compatible test bench design two different FMC mezzanines have been used. One home made mezzanine for TTC handling, and one commercial mezzanine for data readout and trigger throttling

- FMC mezzanine
- Designed by CERN
- Optical input for TTC signal
- 1 extra SFP+ cage
- Channels A/B electrical inputs
- CMS compatible



- FMC mezzanine
- Commercial product : **TB-FMCL-LVDS** from Inrevium – 250 €
- 2x16 LVDS I/O lines
- RJ45 plugs are a mezzanine on top of a mezzanine added to be compatible with CMS standard connections

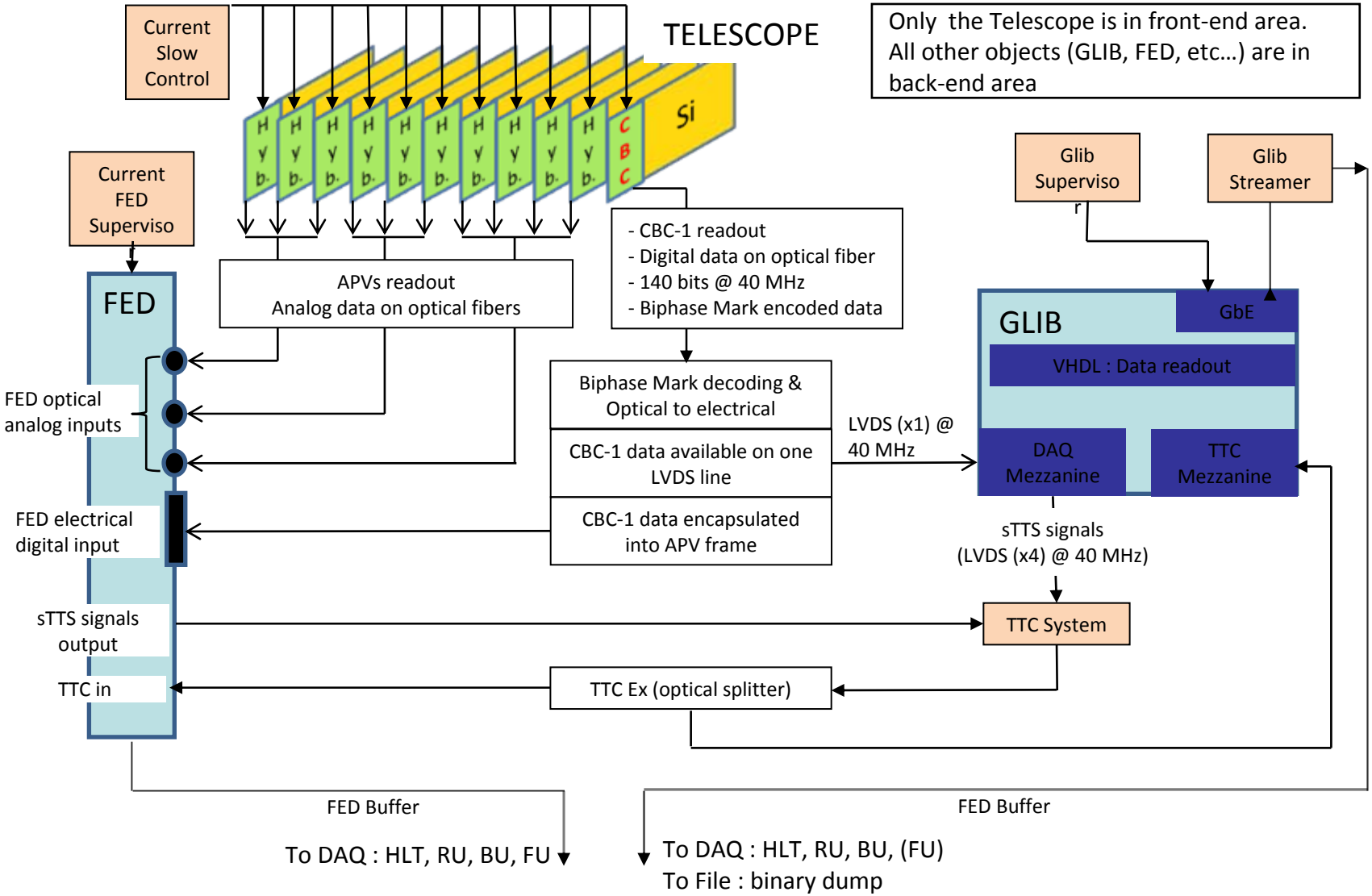
Sensor Data



Trigger Throttle command

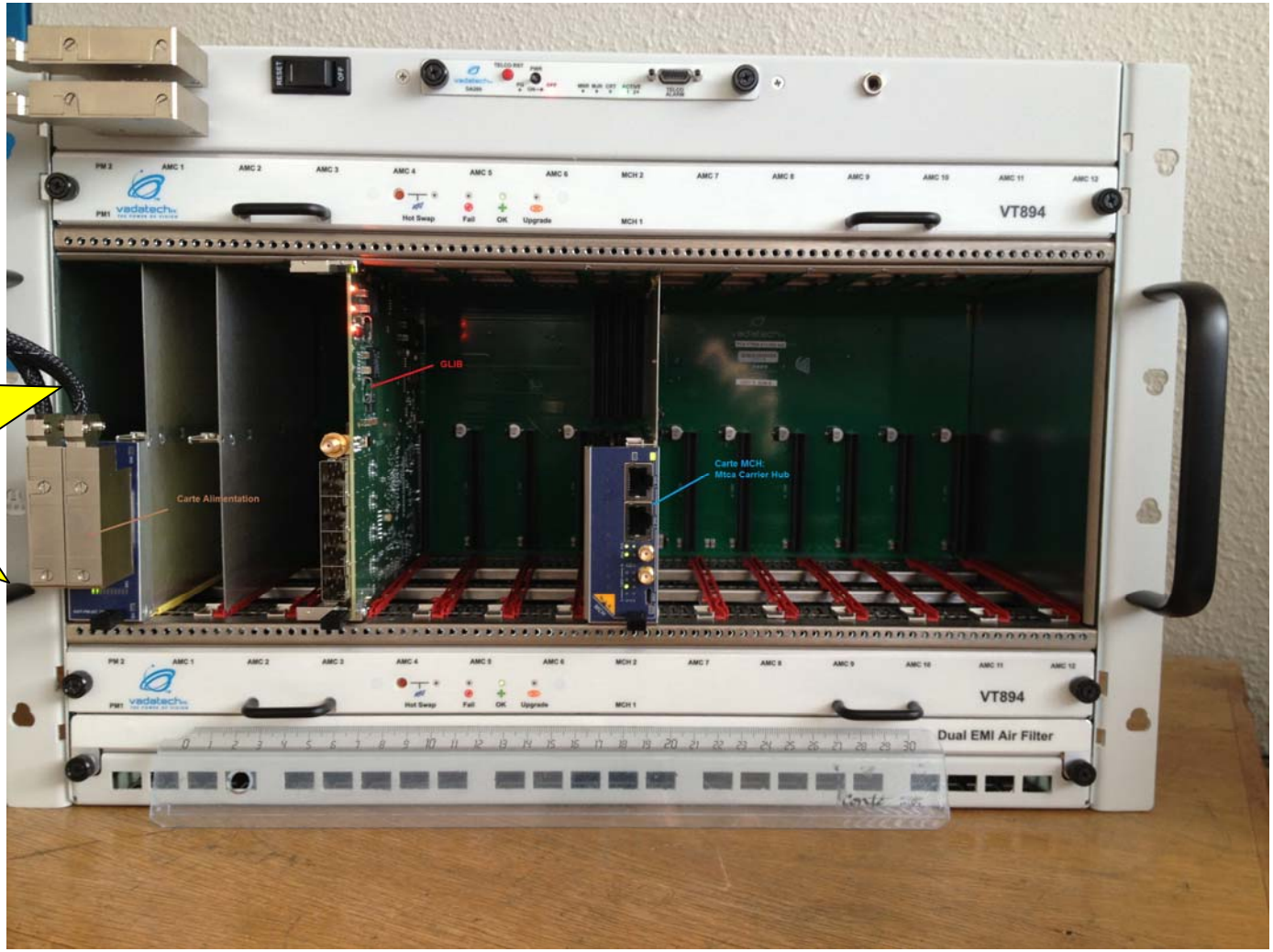
GLIB usage two : CMS compatible test bench

This test bench has been tested on site, in parasitic mode, during UA9 beam test

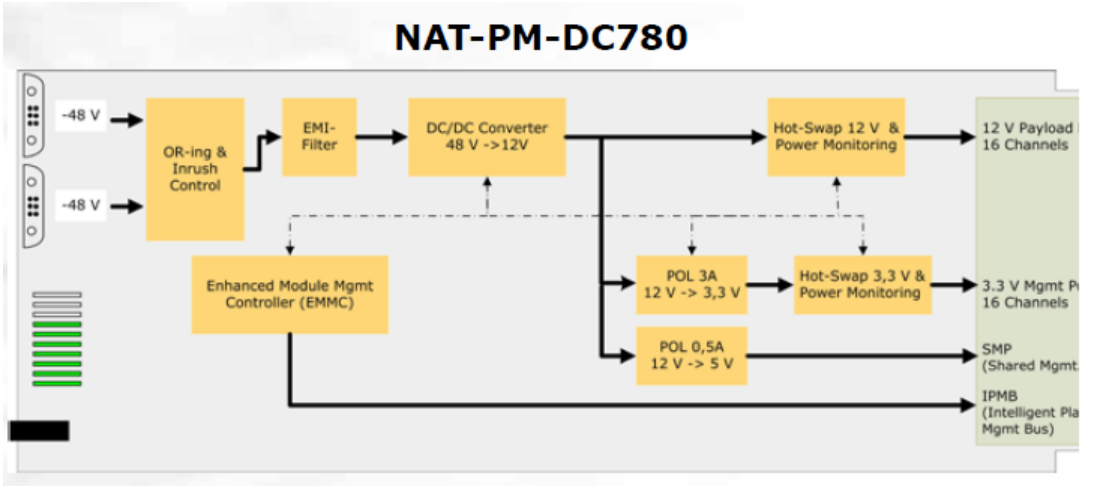


VT894 CRATE TEST SETUP

VADATECH
5600€
12 semaines !!

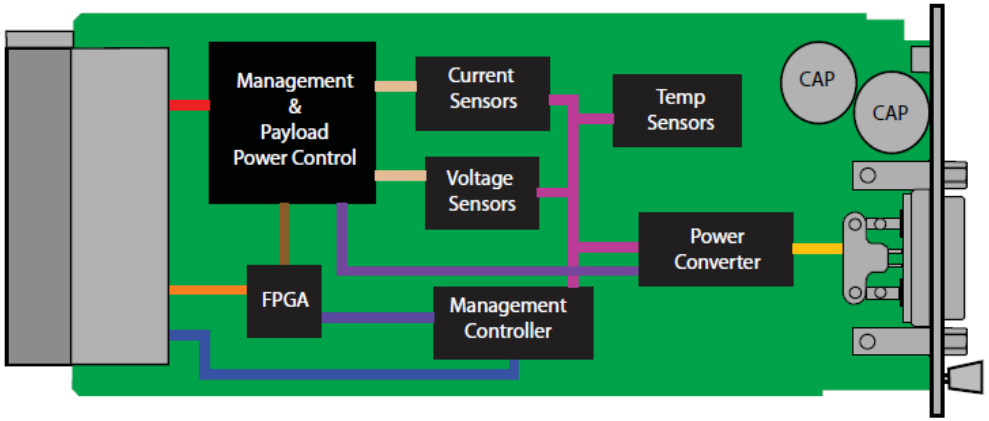


POWER MODULE µTCA CHASSIS



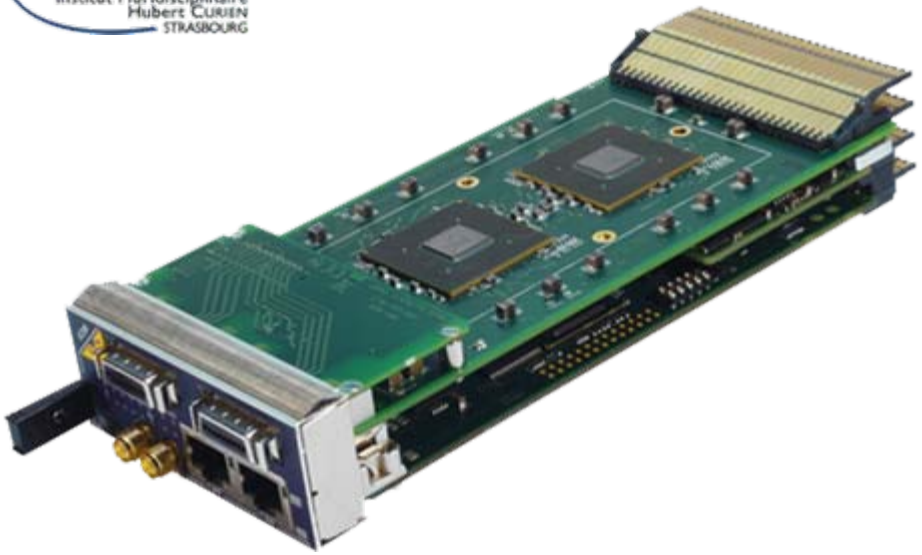
NAT Power Module 780W
Prix: 620€
Délais: 3 semaines

VADATECH UTC010-200



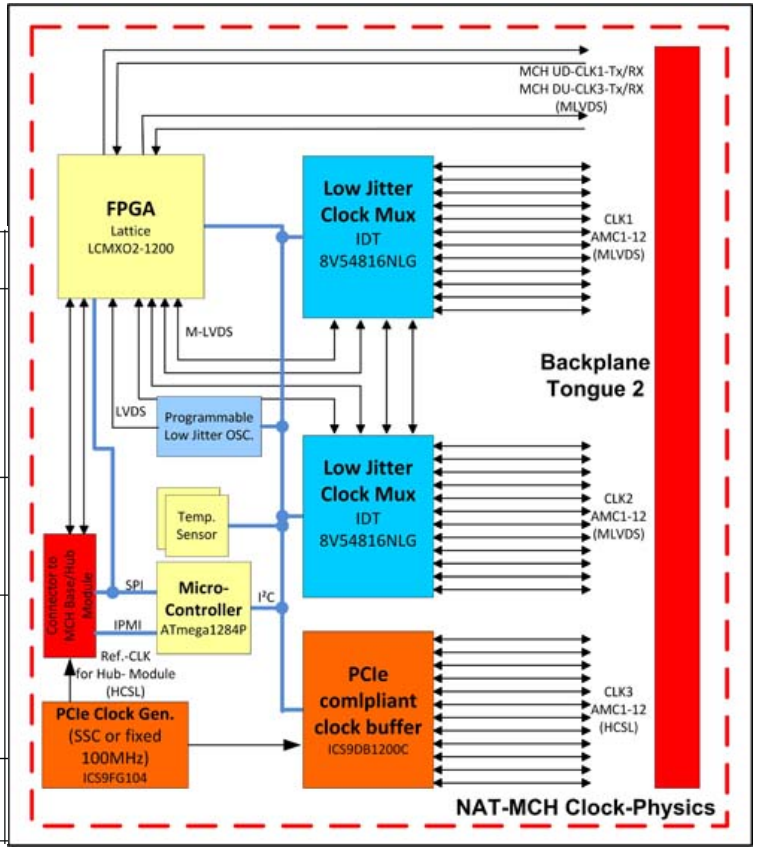
ECRIN Power Module 792W
Prix: 1345€
Délais: 12 semaines

NAT MCH MODULE µTCA CHASSIS



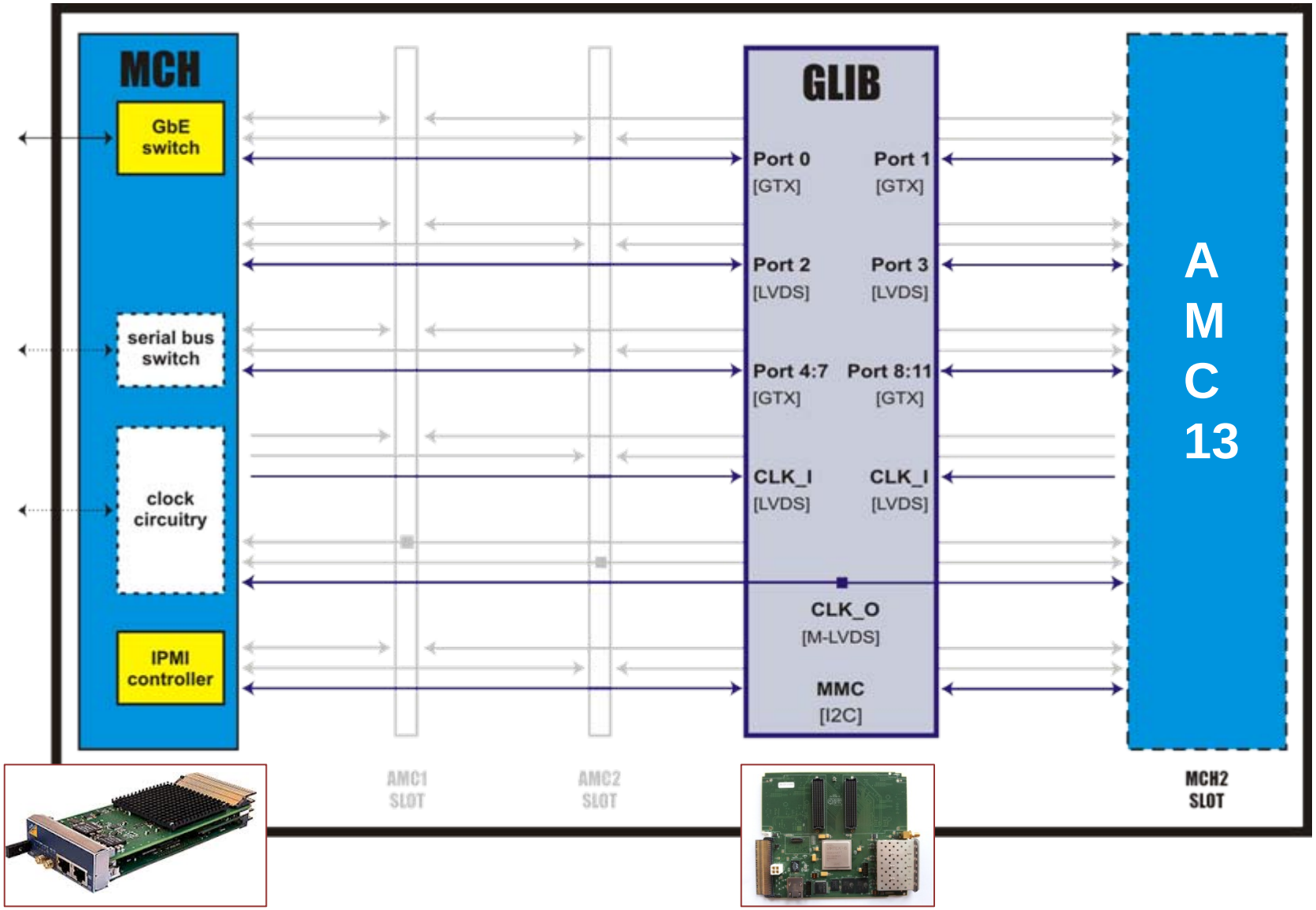
Physics Clock Mezzanine

→ *very low jitter and constant latency*



Item	Description	Type	Unit L-price [EUR]
1	**standard version of MCH base** module: 2xGbE Uplink; USB; Fabric A to 12 AMCs; status LEDs for AMCs, PMs and CUs; management for 12 AMCs; on-board Carrier manager; on-board open HPI compliant shelf-manager; CLI via Telnet or USB; firmware update and script based configuration via TFTP; on-board Webserver; NATview-EASY	**NAT-MCH-Base12-GbE**	795,00
2	**Clock Module** with PCIe clock functionality. A spread spectrum clock (100MHz mean) or a 100MHz fixed clock at HCSL level is provided on CLK3 to all AMCs, can be combined with option NAT-MCH-TCxxxx.	**NAT-MCH-SSCH**	185,00
3	**PHYS clock** PNAT-MCH Clock Module providing special clock functionality (CLK1-2) dedicated to Physics applications and a PCIe spread spectrum or fixed mean clock (CLK3) at HCSL level; reference input for CLK 1/3 selectable as either CLK2 from one of the AMCs or from the CLK input connectors at the front panel	**NAT-MCH-PHYS**	595.00
4	**PCIe x4** supplement (Fabrics D-G incl. update channels) for up to 12 AMCs with PEX8748 and support for AMC13 slot	**NAT-MCH-PCIEx48-Gen3**	885,00

GLIB in a Crate

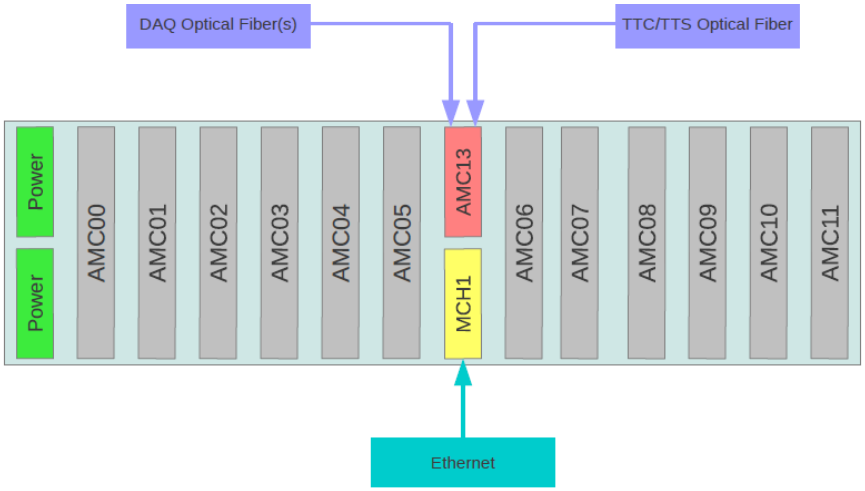


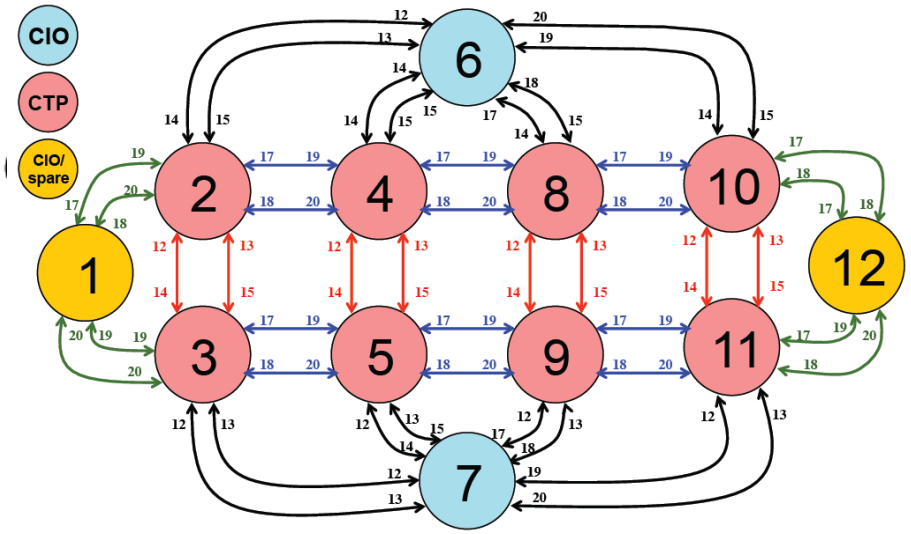
AMC 13 OVERVIEW

- **MCH2—contains Boston University module, "AMC13", for TTC downlink and crate DAQ interface**

The AMC13 is responsible for processing data fragments received from the µTCA crate's advanced mezzanine cards (AMCs) and constructing formatted events for readout. The module is also responsible for acquiring trigger and timing information and distributing it to the rest of the µTCA crate.

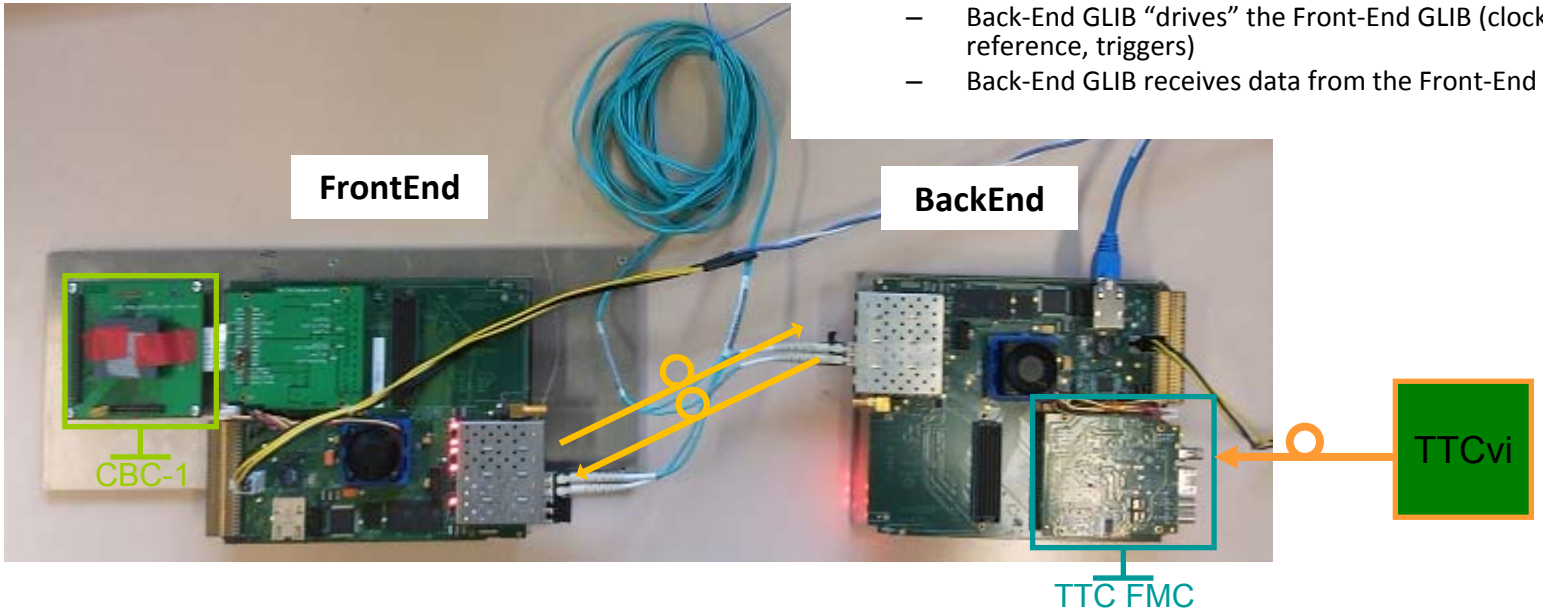
- **Each AMC Slot Contains backplane 20 ports with a Tx & Rx pair**
  - Ports 0-3—for GbE, TTC, DAQ
  - Ports 4-7—star fabric to slot MCH1
  - Ports 8-11—star fabric to slot MCH2
  - Port 12-15 and 17-20—not connected on VT892, but enhanced with custom fabric on VT894





SETUP: GLIB BackEnd to GLIB FrontEnd

- GLIB-to-GLIB communication via GBT emulation



- Back-End GLIB "drives" the Front-End GLIB (clock reference, triggers)
- Back-End GLIB receives data from the Front-End GLIB

Objectif :

Schéma de DAQ final de l'upgrade tracker la GLIB de front-end sera remplacée par un module (Capteur silicium + hybride + GBT)


תודה
Dankie
Gracias
Спасибо
شكراً
Merci
Takk
Köszönjük
Terima kasih
Grazie
Dziękujemy
Děkojame
Ďakujeme
Vielen Dank
Paldies
Kiitos
Täname teid
谢谢
Thank You
Tak
感謝您
Obrigado
Teşekkür Ederiz
감사합니다
Σας Ευχαριστούμ
ขอบคุณ
Bedankt
Děkujeme vám
ありがとうございます
Tack