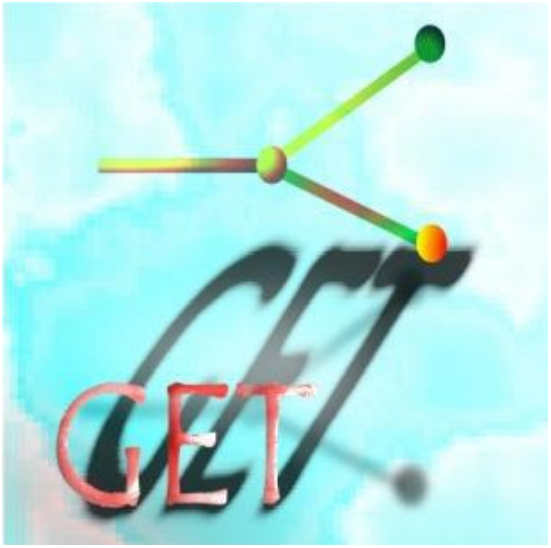


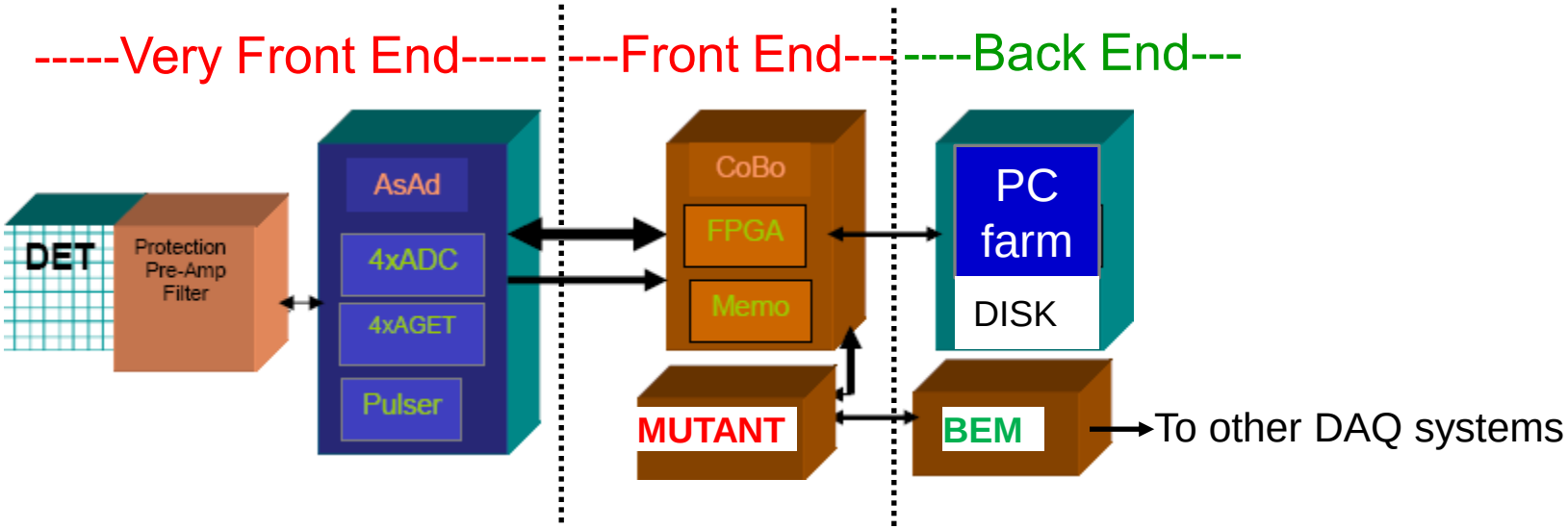
General Electronics for TPC

A project based on the µTCA™ standard

(MTCA.0 specifications)

design status

DAQ block diagram



AGET: Asic for GET – 64 analog channels - 512 cells/channel

ASAD: AGET Support for Analog to Digital – 4 AGET

COBO: COncentration BOard – 4 ASAD - 1024 digital channels

MUTANT: MUtiplicity, Trigger ANd Time (3 trigger levels)

BEM: Back End Module (coupling, logical inspections, …)

IRFU

CENBG

NSCL/MSU

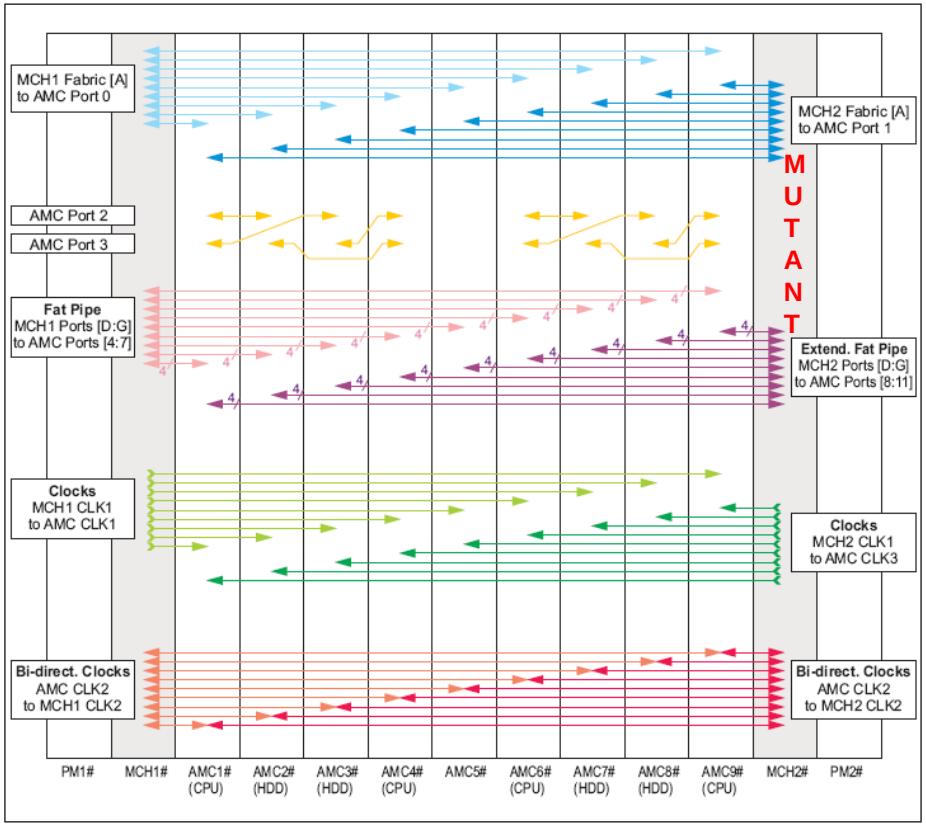
Collaboration based on an "ANR" grant for the French labs

Choice of µTCA standard for the project

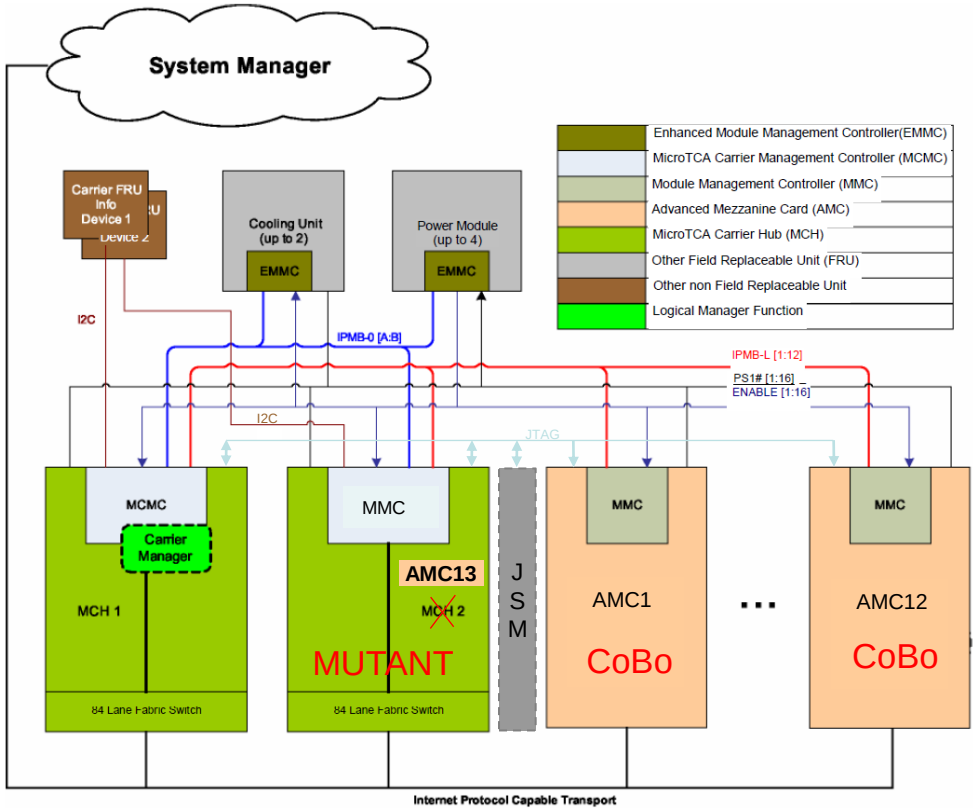
GANIL Laboratory
⇨leader & referent for µTCA of GET

« Dual Star » topology shelf
(redundancy)

SCHROFF & VADATECH (VT893) shelves approved



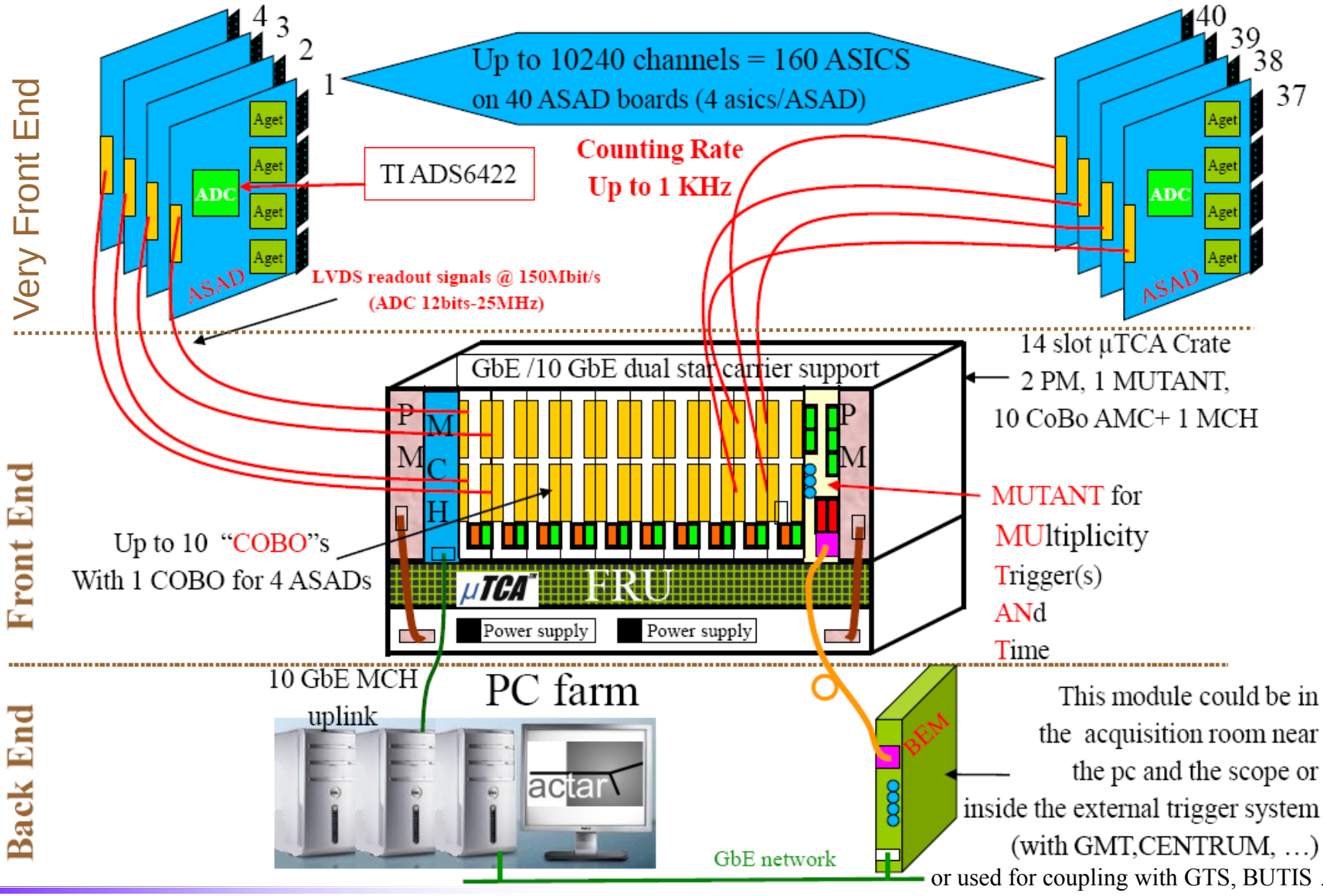
Up to 6.5 Gbit/s by serial port (1TX/1RX)



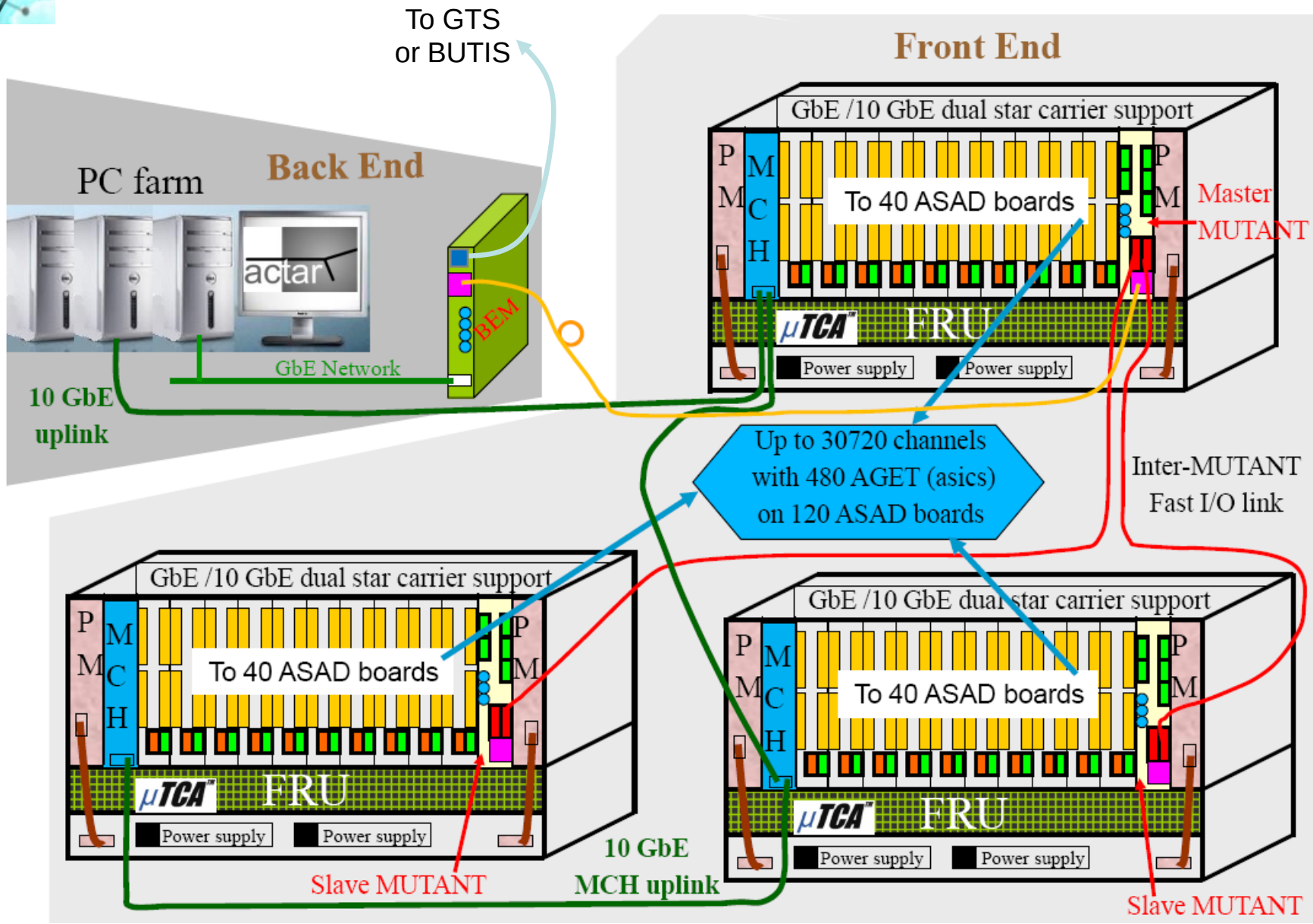
Associated **F**ield **R**eplaceable **U**nits:

- MicroTCA Carrier Hub (MCH)
  Carrier management / Network Switch
- Power Module (PM)
- Advance Mezzanine Card (AMC)
- JTAG Switch Module (JSM)
- Cooling Units (CU)

Typical architecture for 1 µTCA shelf



Full architecture – 3 µTCA shelves

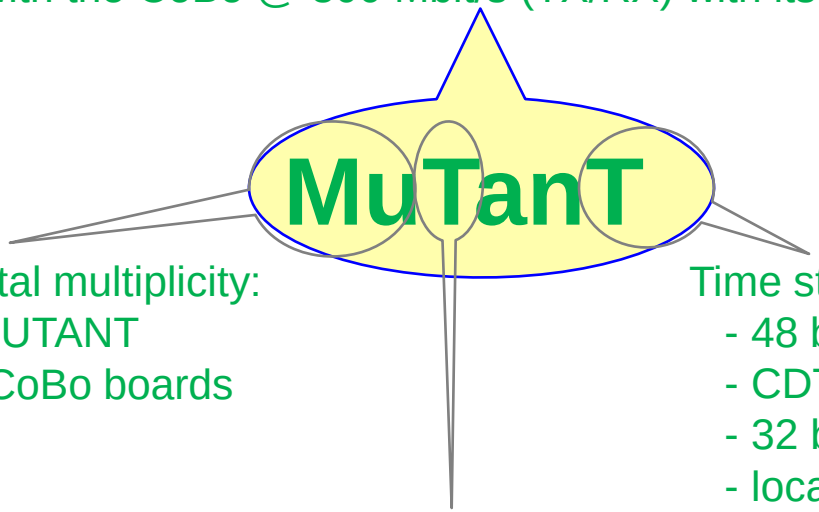


Main tasks of MUTANT

Distribution of a 100 MHz clock to every CoBo of each crate, phase aligned (skew< 1ns - TDC) ⇨ µTCA-CLK1

Distribution of a synchronous start/stop sampling (phase aligned) ⇨ µTCA-CLK2

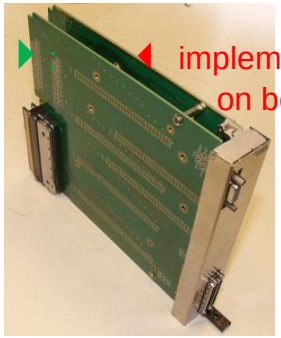
Exchanging data in parallel with the CoBo @ 800 Mbit/s (TX/RX) with its own shelf or slave shelves



Building the whole TPC Digital multiplicity:
- Master Mutant + slave MUTANT
- Each MUTANT with the CoBo boards every 40 ns

Time stamp:
- 48 bits / 10 ns
- CDT/autonomous mode
- 32 bit event number (CDT)
- local/remote (via BEM)

implemented on board B



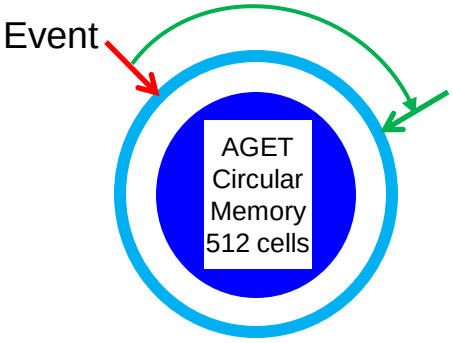
implemented on board A

3 Trigger levels:
- -LØ= External Trigger
- -L1 = Multiplicity Trigger
- -L2 = Hit Pattern Trigger

MUTANT- CoBos data exchanges
main time values

AGET: Sampling Frequency = 1-100 MHz
Trigger roundtrip: 512 x 10 ns = 5.12 µs
to 512 x 1µs = 512 µs

Full memory

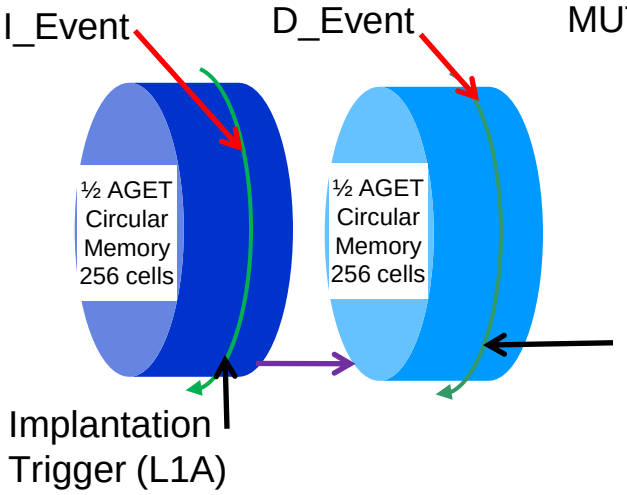


MUTANT Programmable Delay & Gates are 16 bits wide
Attached to GMC (10 ns)

CoBo to MUTANT : L1: new multiplicity value @ 25 MHz max
nothing to do @ MUTANT level for lower frequency
L2: 1.3µs to receive the TPC hit pattern (one shelf)
12.8 µs for added shelves

MUTANT trigger "OK" to CoBo "STOP": -LØ : 30 ns/655 µs max
- L1 : 80 ns /655 µs max
- L2 : depends on the algorithm !

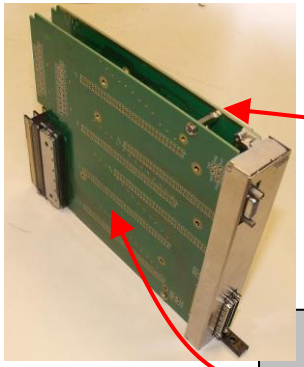
2 x half-memories (2p decay)



MUTANT information's to CoBo:
- L2 mask pattern: 1.3 µs
- Time stamp + Event Number: 120 ns
- Time stamp only: 80 ns

Decay Trigger (L1B) or
Time-out (programmable)

Synoptic and board assembly



Tongue 1

Port A +Fat Pipe (Ports D,E,F,G) X 10 Tongue 3 & 4 (200 signals)

MUTANT Master/Slave Front panel VHDCI link

CENTRUM/SCALERS Front panel Interface

TRIGGER I/O Front panel Interface

LVDS buffers

LVDS/ LVPECL buffers

NECL buffers

buffers

XILINX-V5FX70T

PowerPC 440 Processor

TRIGGER & TIME STAMPER ENGINE

DDR2

FLASH

B

VT026 AMC management

GbE RS232

Front panel

XILINX-V5FX30T

ICE

VxWorks

PowerPC 440 Processor

EMC

OPTICAL transceivers ribbon fibbers

To BEM (Optical link)

FLASH

DDR2

A

TDC

Global Master Clock Management/Distribution

Tongue 2

Front panel

2 boards to design = 2 projects !

Board B

Board A

TONGUE

4

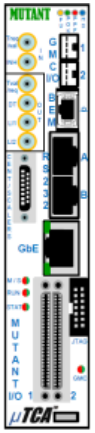
3

2

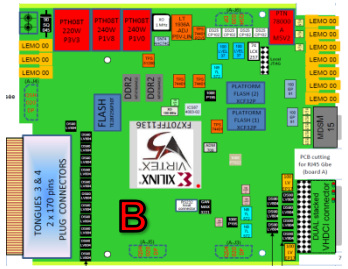
1

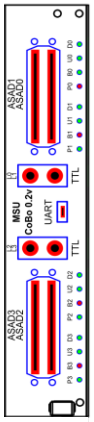
1 tongue = 2 x 85 pins
4 tongues to manage
= 680 pins!

MUTANT in terms of schedule



- MUTANT module is on track
  - Board A is tested
    (as a kit on the table then inside the crate with management)
  - One board is running at NSCL/MSU (USA)
  - Electronic study of board B is ready
    PCB design is in progress
  - Full MUTANT prototype is expected in October 2013





- CoBo module is also under test @ NSCL
  - 3 boards tested
  - Production is foreseen by the end of this year

- First µTCA configuration (CoBos + MUTANT) end 2013/early 2014

- **First use at GANIL/SPIRAL II with ACTAR TPC and S^3 (Spiral2 Super Spectrometer)**
- **Beyond the laboratories concerned by the collaboration (GANIL,NSCL,IRFU Saclay, CENBG), other foreign laboratories are interested by the GET system:**

  -> Tokyo & Riken labs (Japan), INFN Catania (Italy), IBS Daejeon (South Korea), …