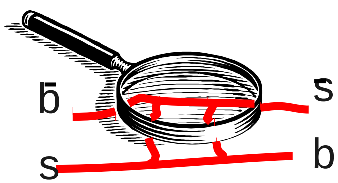
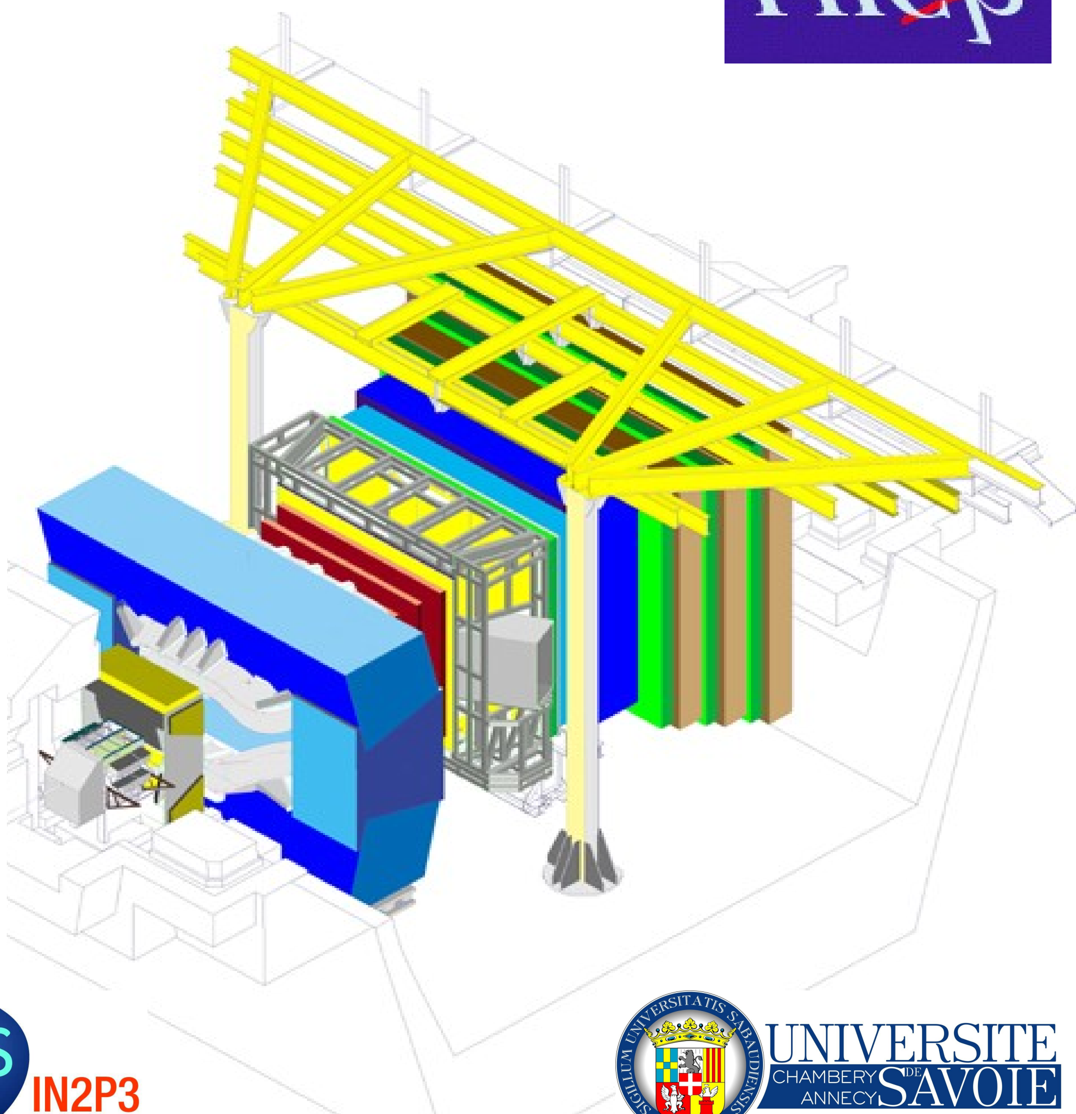
LHCb : Upgrade et implication du LAPP

Journée prospective

3 octobre 2013



Stéphane T'JAMPENS



Outline

Motivations

Current LHCb

Overview of the LHCb Upgrade

LAPP involvement

Flavor in the Era of LHC

Ritchie – IF 2013

New Physics found at LHC

⇒ New particles with unknown flavor- and CP-violating couplings

Precision flavor-physics expts will be needed sort out the flavor- and CP-violating couplings of the NP.

New Physics NOT found at LHC

Precision flavor-physics expts will be needed since they are sensitive to NP at mass scales beyond the LHC.

Precision quark-flavor experiments (and lepton-flavor too) are essential.

Need experimental precision and theoretical cleanliness to increase NP sensitivity

LHCb Physics Prospects

EPJC **73** (2013) 2373

~10 years

Type	Observable	Current precision	LHCb 2018	**Upgrade** ($50\,\mathrm{fb}^{-1}$)	Theory uncertainty
B_s^0 mixing	$2\beta_s\ (B_s^0 \to J/\psi\ \phi)$	0.10 [137]	0.025	0.008	~ 0.003
	$2\beta_s\ (B_s^0 \to J/\psi\ f_0(980))$	0.17 [213]	0.045	0.014	~ 0.01
	a_{sl}^s	6.4×10^{-3} [43]	0.6×10^{-3}	0.2×10^{-3}	0.03×10^{-3}
Gluonic penguins	$2\beta_s^{\mathrm{eff}}(B_s^0 \to \phi\phi)$	–	0.17	0.03	0.02
	$2\beta_s^{\mathrm{eff}}(B_s^0 \to K^{*0}\bar{K}^{*0})$	–	0.13	0.02	< 0.02
	$2\beta^{\mathrm{eff}}(B^0 \to \phi K_S^0)$	0.17 [43]	0.30	0.05	0.02
Right-handed currents	$2\beta_s^{\mathrm{eff}}(B_s^0 \to \phi\gamma)$	–	0.09	0.02	< 0.01
	$\tau^{\mathrm{eff}}(B_s^0 \to \phi\gamma)/\tau_{B_s^0}$	–	5 %	1 %	0.2 %
Electroweak penguins	$S_3(B^0 \to K^{*0}\mu^+\mu^-; 1 < q^2 < 6\,\mathrm{GeV}^2/c^4)$	0.08 [67]	0.025	0.008	0.02
	$s_0\,A_{\mathrm{FB}}(B^0 \to K^{*0}\mu^+\mu^-)$	25 % [67]	6 %	2 %	7 %
	$A_{\mathrm{I}}(K\mu^+\mu^-; 1 < q^2 < 6\,\mathrm{GeV}^2/c^4)$	0.25 [76]	0.08	0.025	~ 0.02
	$\mathcal{B}(B^+ \to \pi^+\mu^+\mu^-)/\mathcal{B}(B^+ \to K^+\mu^+\mu^-)$	25 % [85]	8 %	2.5 %	$\sim 10\,\%$
Higgs penguins	$\mathcal{B}(B_s^0 \to \mu^+\mu^-)$	1.5×10^{-9} [13]	0.5×10^{-9}	0.15×10^{-9}	0.3×10^{-9}
	$\mathcal{B}(B^0 \to \mu^+\mu^-)/\mathcal{B}(B_s^0 \to \mu^+\mu^-)$	–	$\sim 100\,\%$	$\sim 35\,\%$	$\sim 5\,\%$
Unitarity triangle angles	$\gamma\ (B \to D^{(*)}K^{(*)})$	~ 10–12° [243, 257]	4°	0.9°	negligible
	$\gamma\ (B_s^0 \to D_s K)$	–	11°	2.0°	negligible
	$\beta\ (B^0 \to J/\psi\ K_S^0)$	0.8° [43]	0.6°	0.2°	negligible
Charm CP violation	A_Γ	2.3×10^{-3} [43]	0.40×10^{-3}	0.07×10^{-3}	–
	$\Delta\mathcal{A}_{CP}$	2.1×10^{-3} [18]	0.65×10^{-3}	0.12×10^{-3}	–

Current Sensitivity limited by statistics, not theory

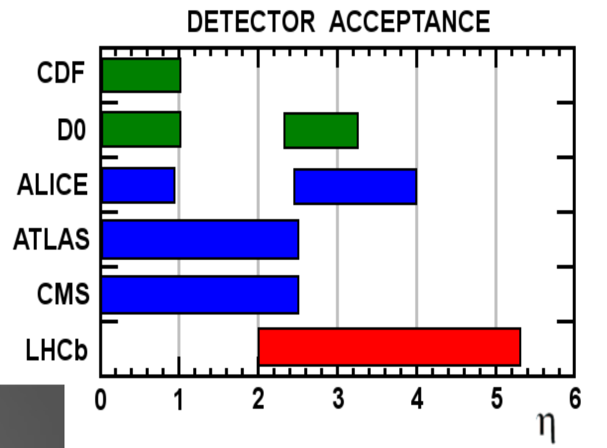
Upgrade: comparable to or better than the theoretical uncertainties

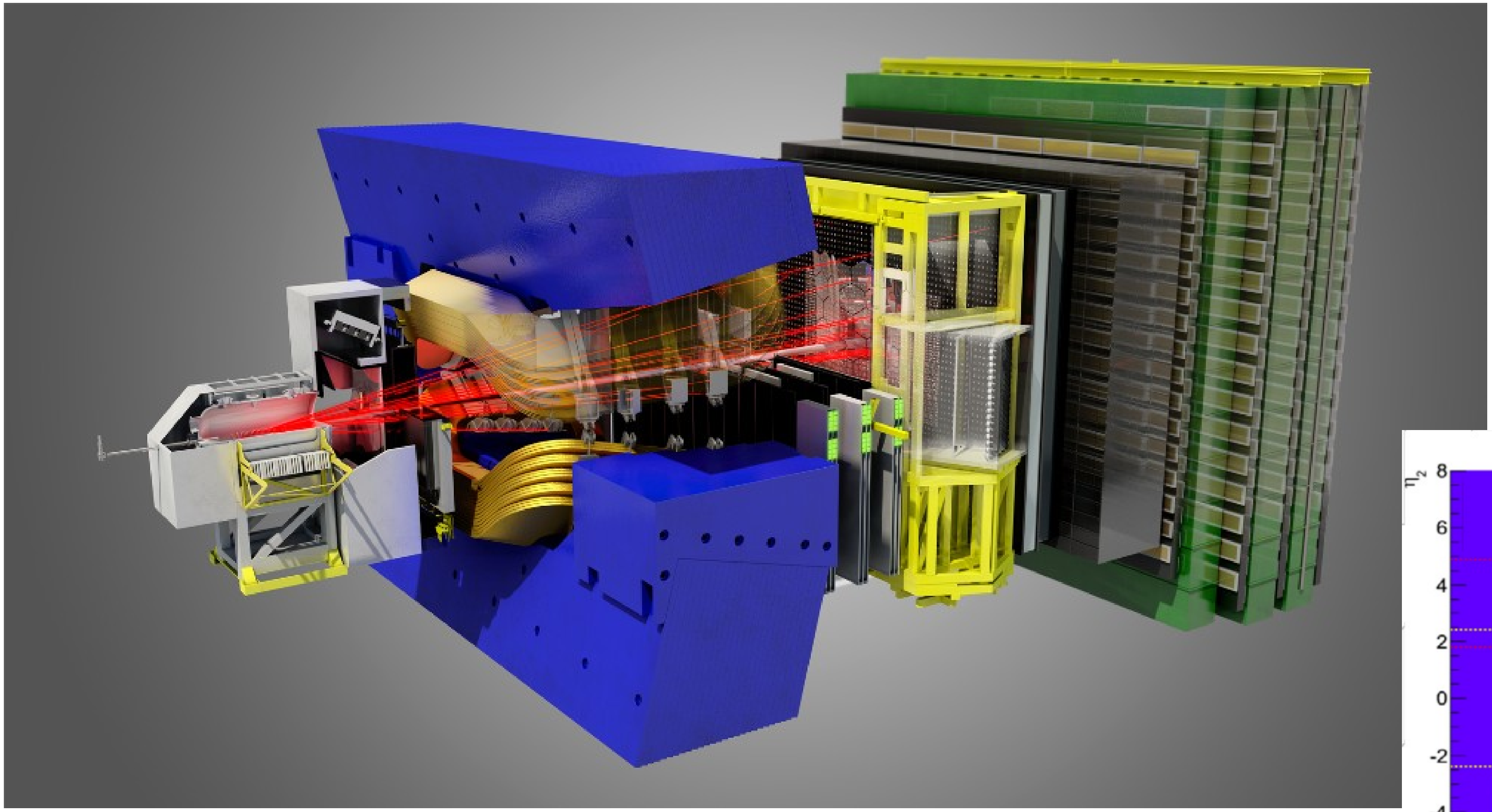
Current LHCb

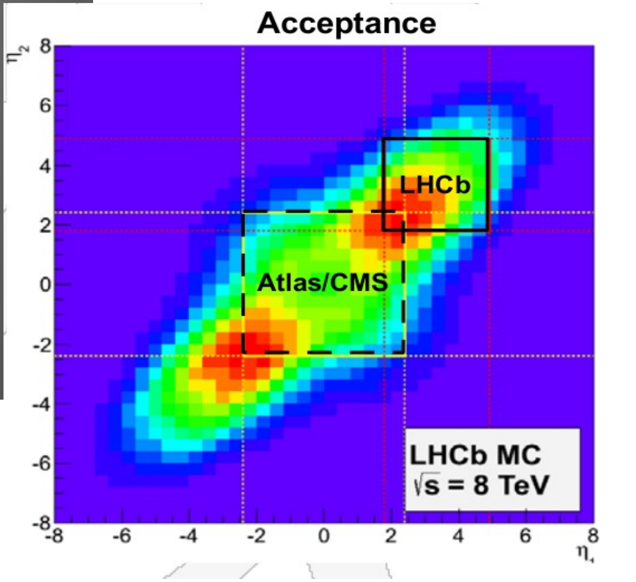
LHCb Detector

Forward- and backward-peaked $b\bar{b}$ production:

- LHCb is a single-arm forward spectrometer: $2 < \eta < 5$
- 4% of solid angle







Captures ~40% of heavy-quark production cross-section

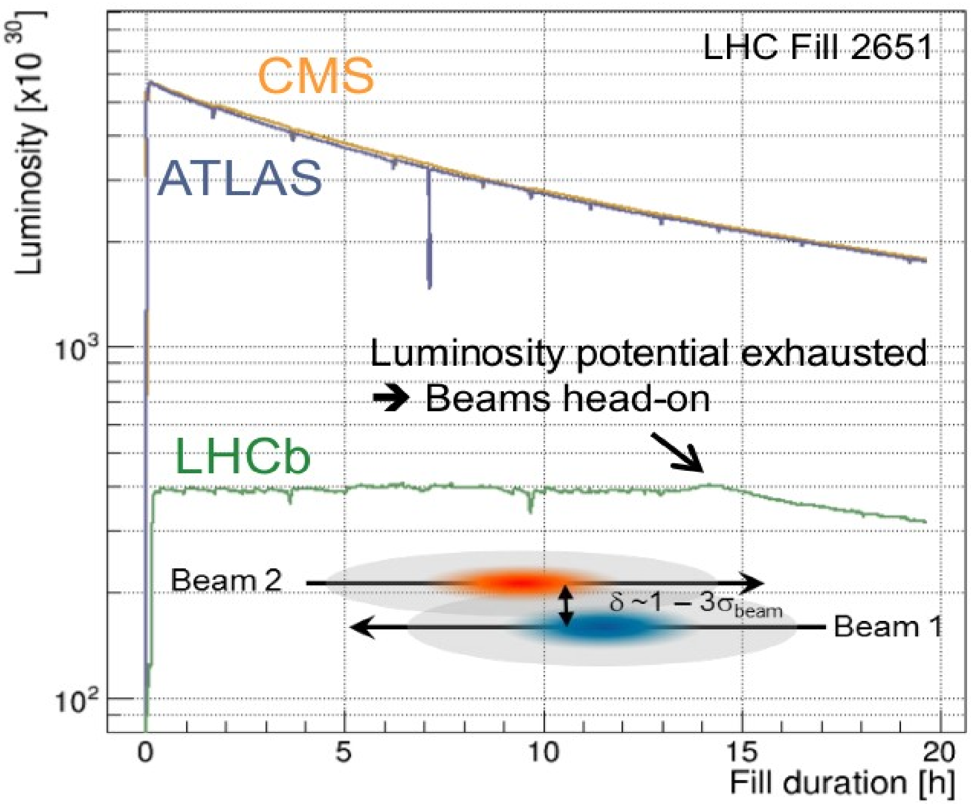
LHCb Operation in 2011-2012

Design: $L_{inst} = 2 \times 10^{32}\ cm^{-2}s^{-1}$ with $\mu=0.4$ [2622 bunches, 25ns, 14 TeV]

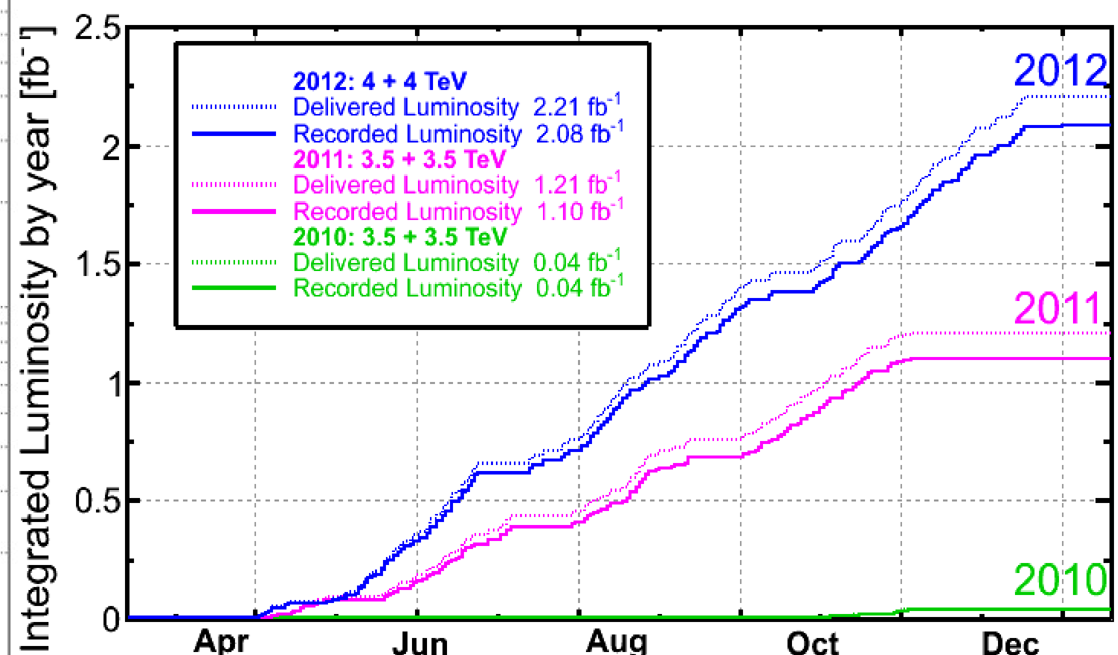
LHCb has excellent performance (beyond design)

Year	$\sqrt{s}$ [TeV]	$\mathcal{L} \times 10^{32} [cm^{-2}s^{-1}]$	$\frac{\text{Interactions}}{\text{crossing}}$	HLT rate	L $[fb^{-1}]$
2011	7	$2-4$	$0.4-2.5$	3 kHz	>1.0
2012	8	4	1.6	5 kHz	>2.0

Luminosity Levelling:

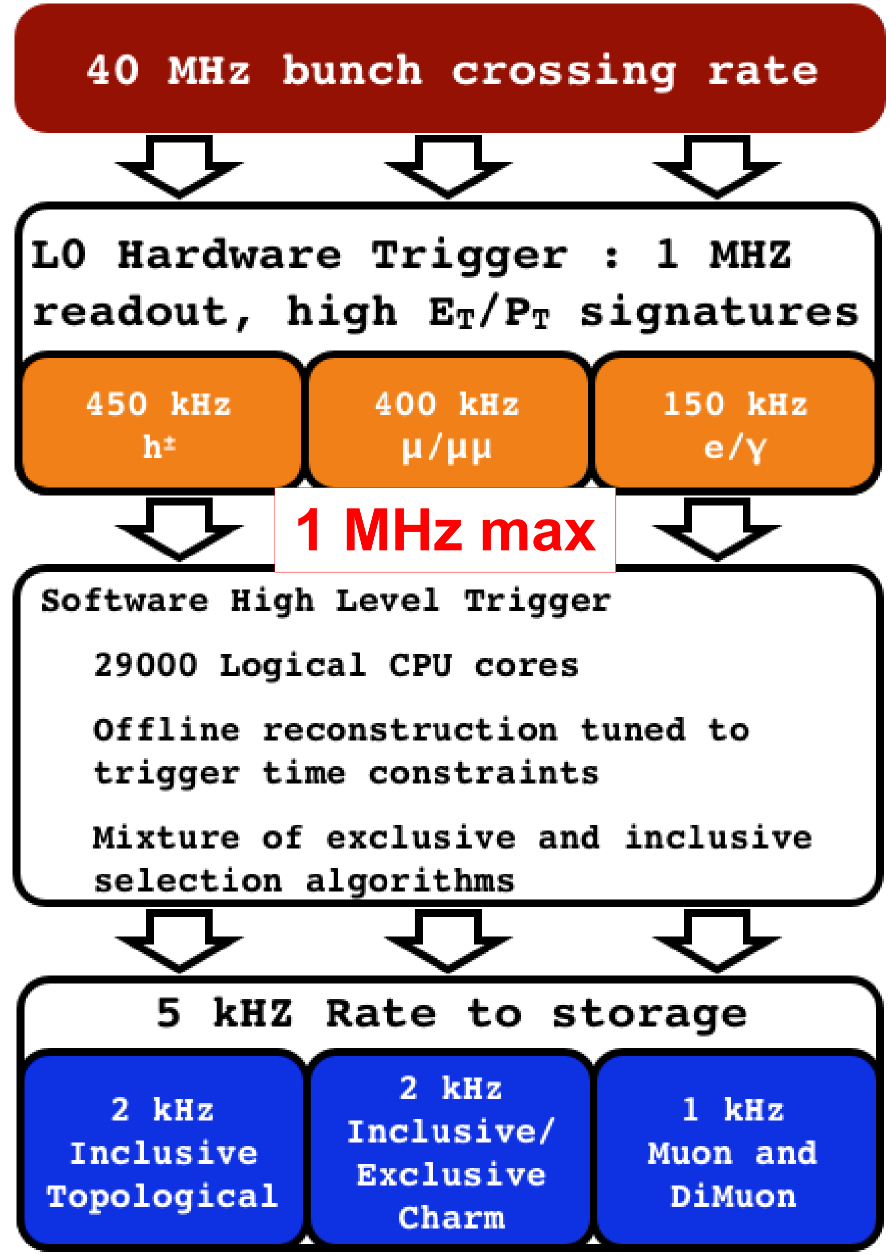


Integrated luminosity:



Current Trigger Architecture

- Level-0 trigger: hardware
  - 4 μs latency @ 40MHz
  - "Moderate" E_T/p_T threshold:
    - $E_T(e/\gamma)>2.7$ GeV; $E_T(h)>3.6$ GeV
    - $p_T(\mu)>1.4$ GeV/c
- HLT trigger: software
  - ~30000 tasks in parallel on ~1500 nodes
  - Processing time available O(35-40 ms)
- Storage rate: 5 kHz
- Combined efficiency (L0+HLT):
  - ~90 % for di-muon channels
  - ~30 % for multi-body hadronic final states
  - ~10-20% for charm decays

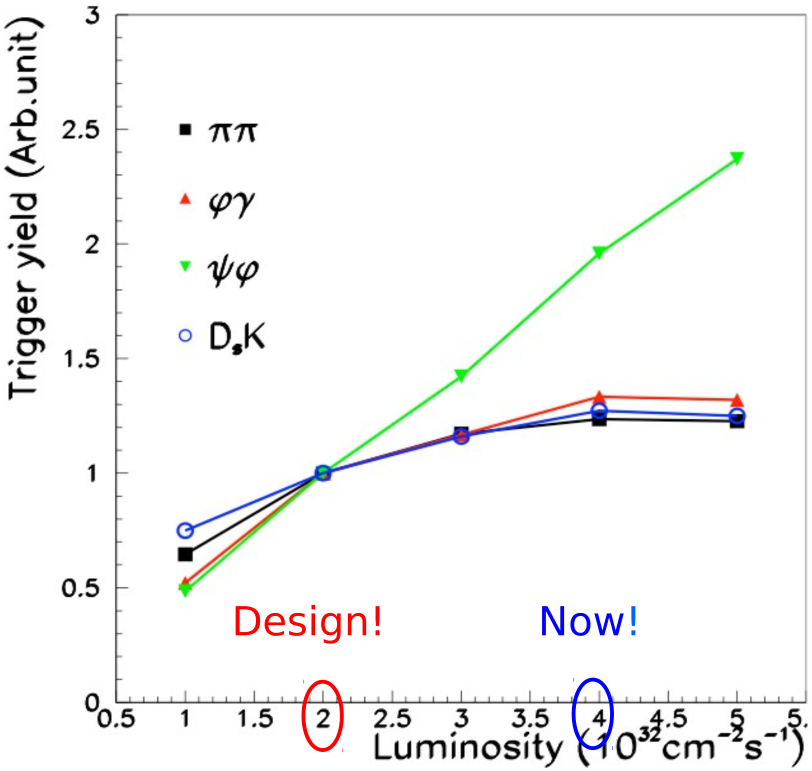


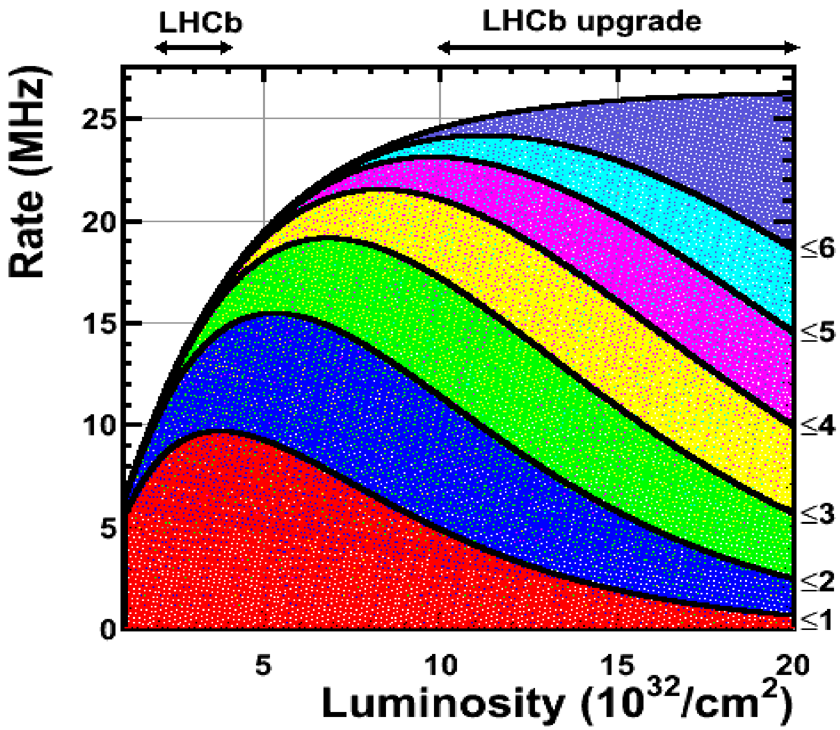
Current Limitations

What prevents us from running at higher luminosity already?

Data bandwidth limited to 1.1 MHz by L0 hardware trigger

⇨ Factor ~2 between di-muon events and fully hadronic decays





At higher luminosities:

→ harsher cuts on p_T and E_T

→ Events busier, reconstruction more difficult

→ Detector aging and degradation

for no real gain in statistics …

Upgrading LHCb

Upgrade Strategy

Efficient selection requires IP and p_T of tracks

- Remove L0 bottle neck (almost → LLT)

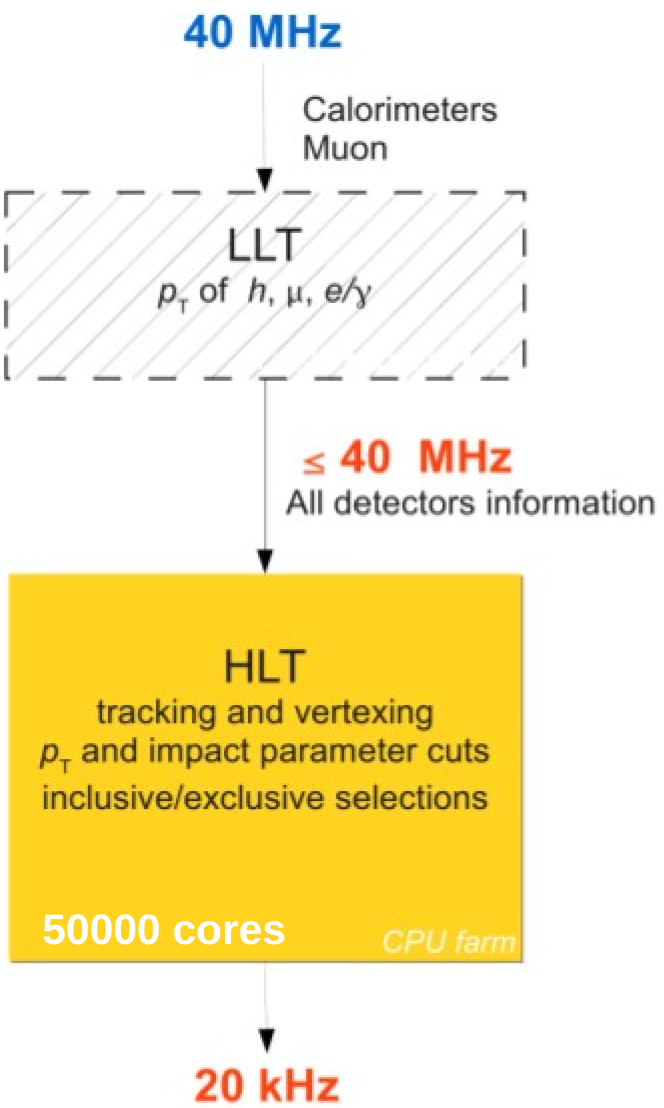
  LLT Calo: C. Drancourt

Implications of upgrade strategy:

- Readout every LHC bunch crossing: 40 MHz instead of 1.1 MHz
  - Trigger-less Front-End electronics
  - Multi-Tb/s readout network
- Fully software flexible trigger (HLT): output bandwidth~20kHz

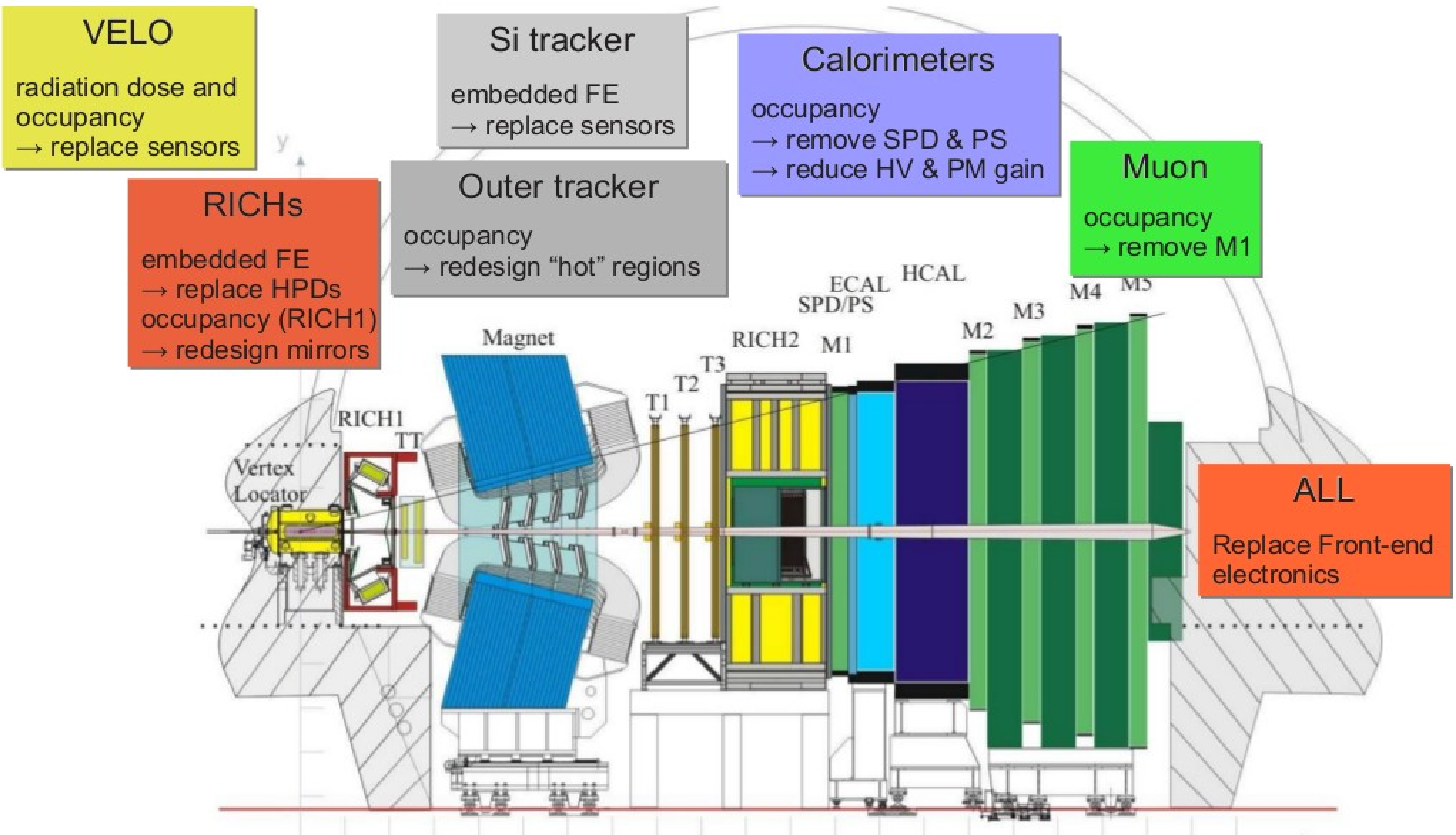
Running Conditions:

- Design upgraded sub-detectors to sustain instantaneous luminosity up to L_{inst} = 20x10^{32} cm^{-2}s^{-1} [μ=4.9, 2622 bunches, 25ns, 14 TeV]



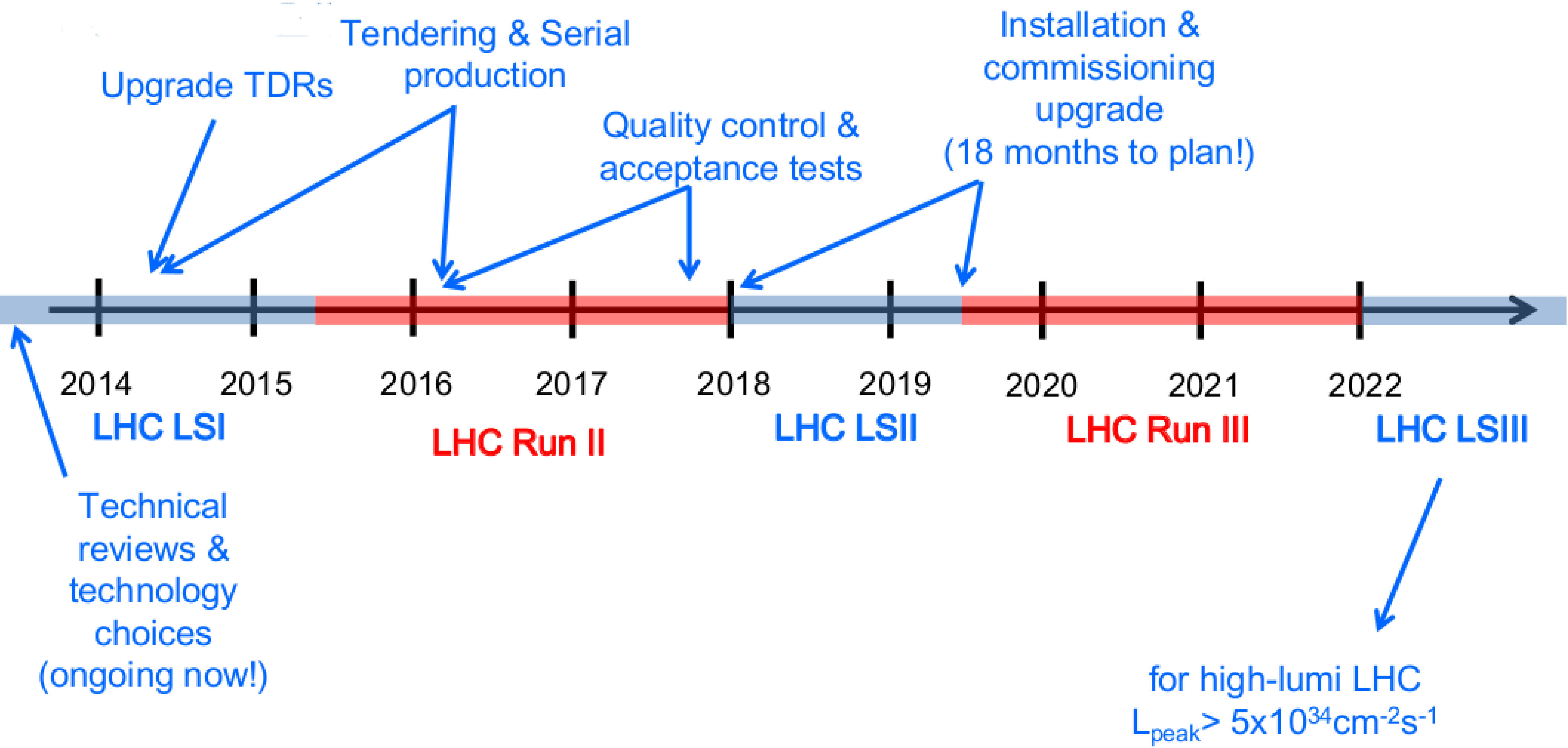
Starting point: 5-10 MHz (LLT) event processing in processing farm at 10x10^{32} cm^{-2}s^{-1}

The 40 MHz Detector



- all subsystems are impacted

LHCb Upgrade Plan

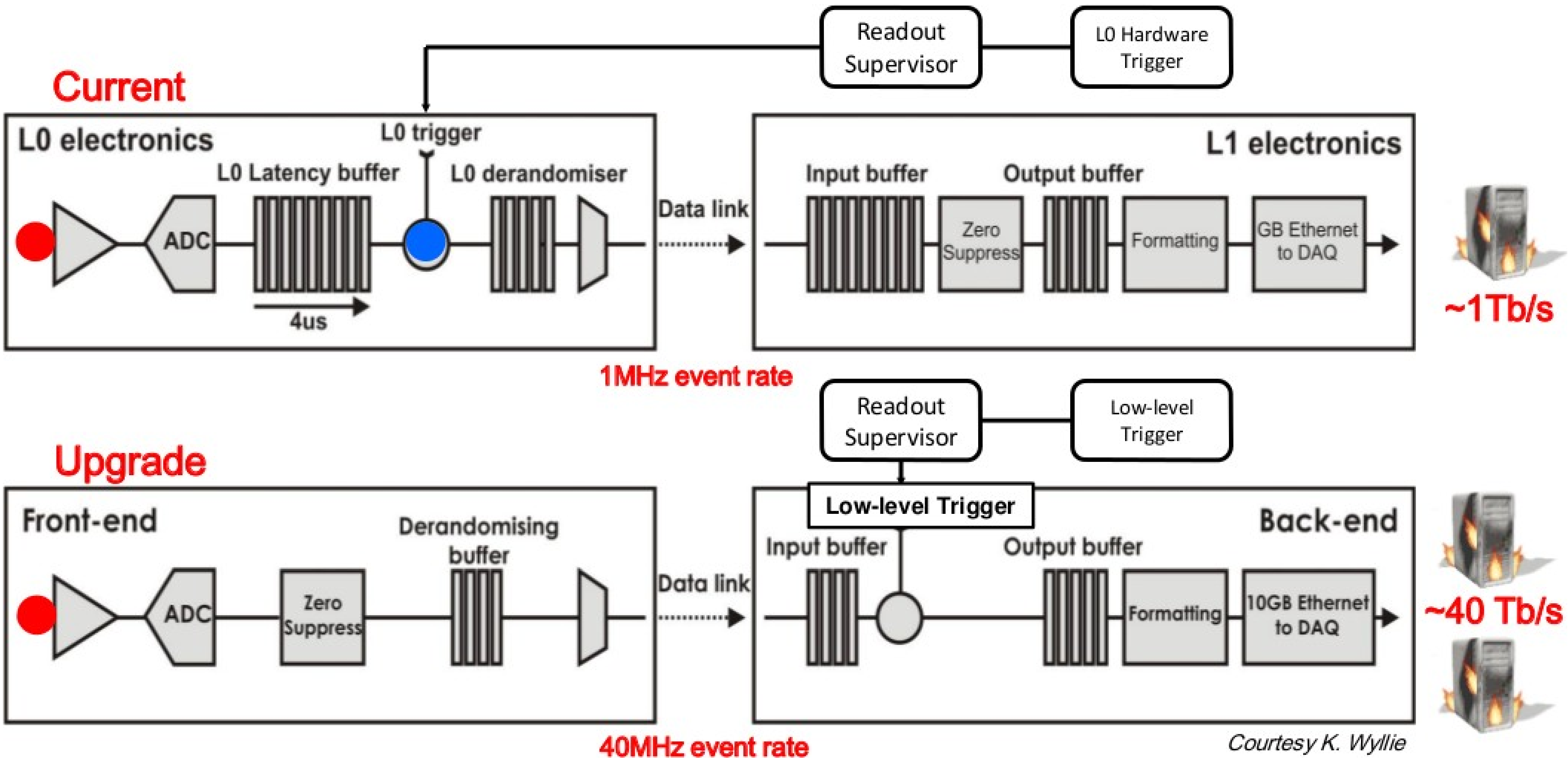


Upgrading LHCb:

DAQ

Upgraded Readout Architecture

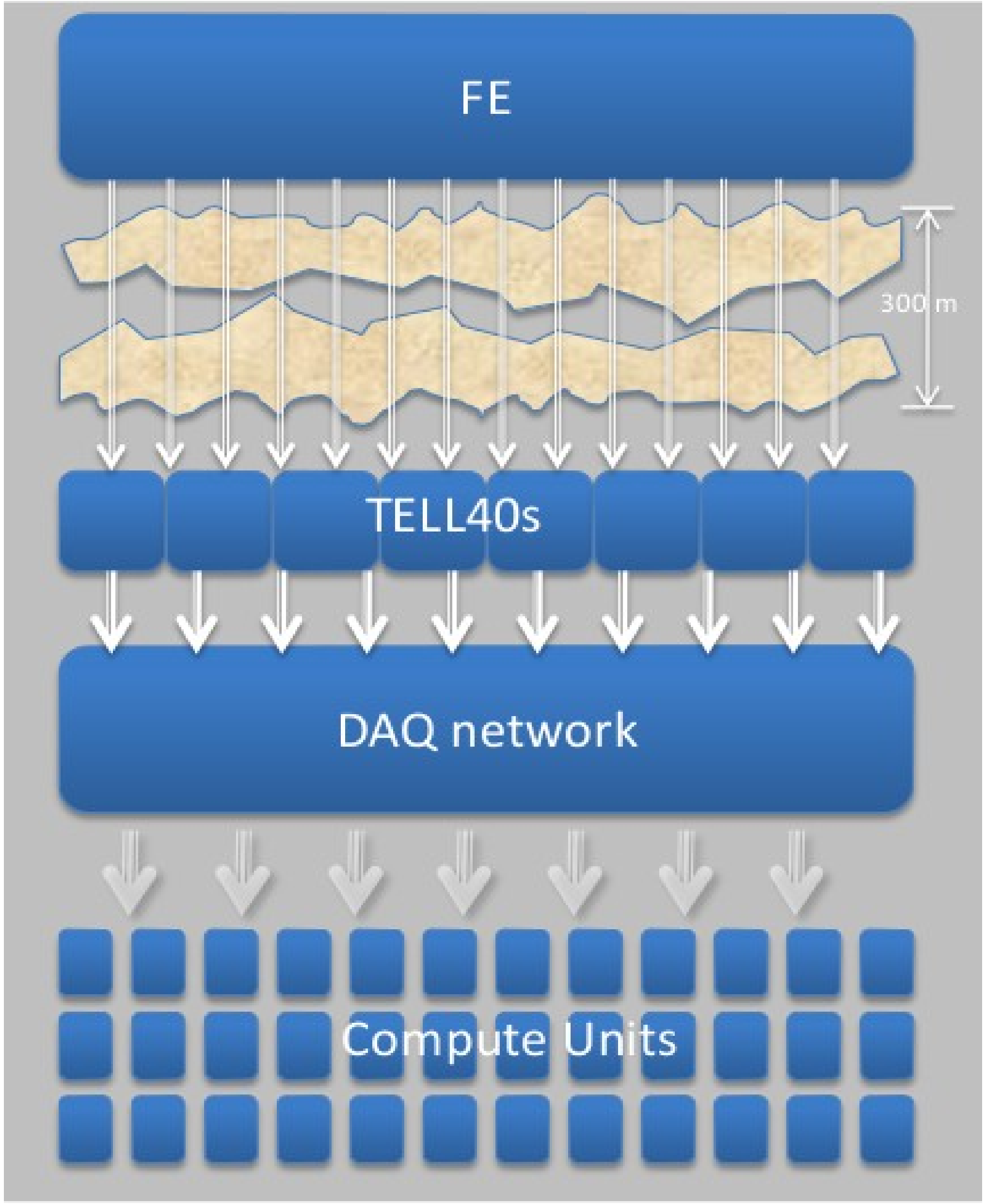
Front-End electronics: transmit data every LHC bunch crossing (25ns)



Compress (zero-suppress) data already at the FE

- reduce # of links from ~80000 to ~12500 (~20 MCHF to ~3.1 MCHF)
- data driven readout (asynchronous) + variable latencies!

Counting Rooms in the Surface



40 Tb/s (event size ~ 100 kB)

Long distance covered by versatile links (GBT)

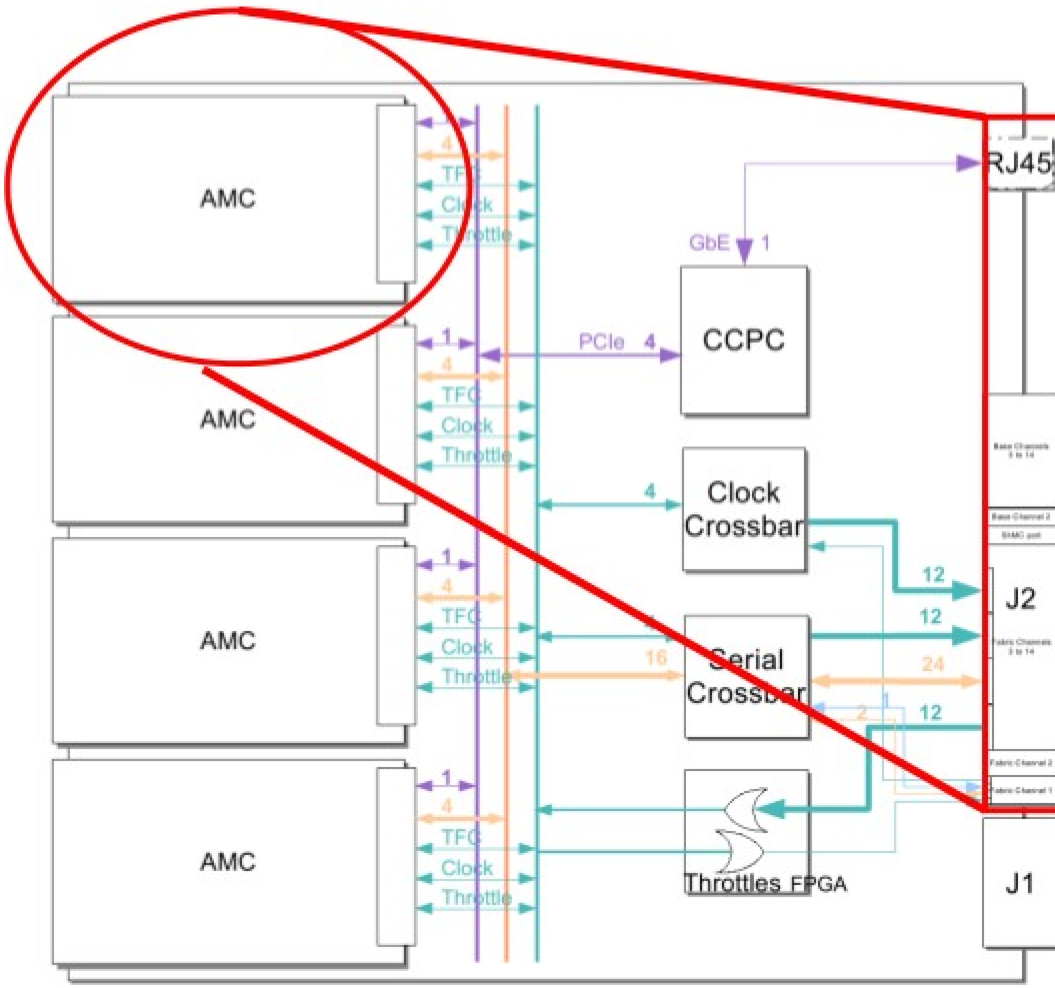
Maximum of 303 m from FE on detector to AMC40 input

Measurements with prototype FE and AMC40 show that this works well with excellent margins

Can use cheapest commercial optical links

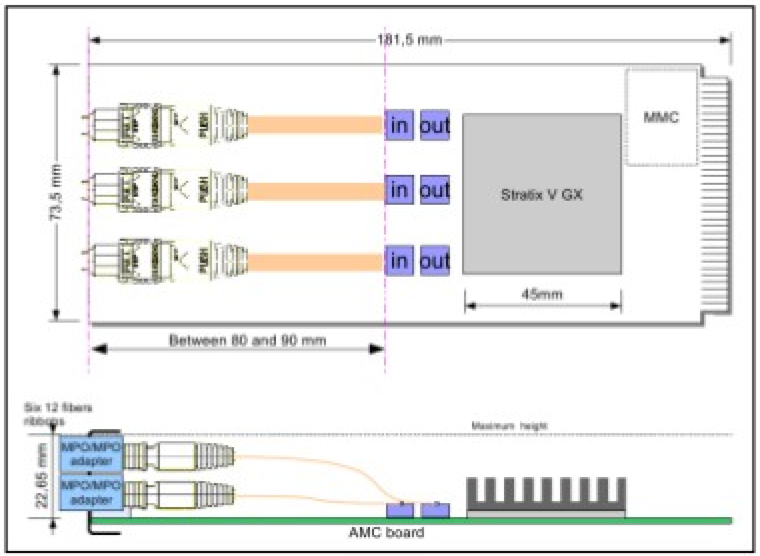
Back-End: new LHCb TELL40 Readout Board

Classical approach: ~0.5 Tb/s data aggregator board with 10 GbE to FARM



24 inputs
@ 4.8 Gb
GBT format

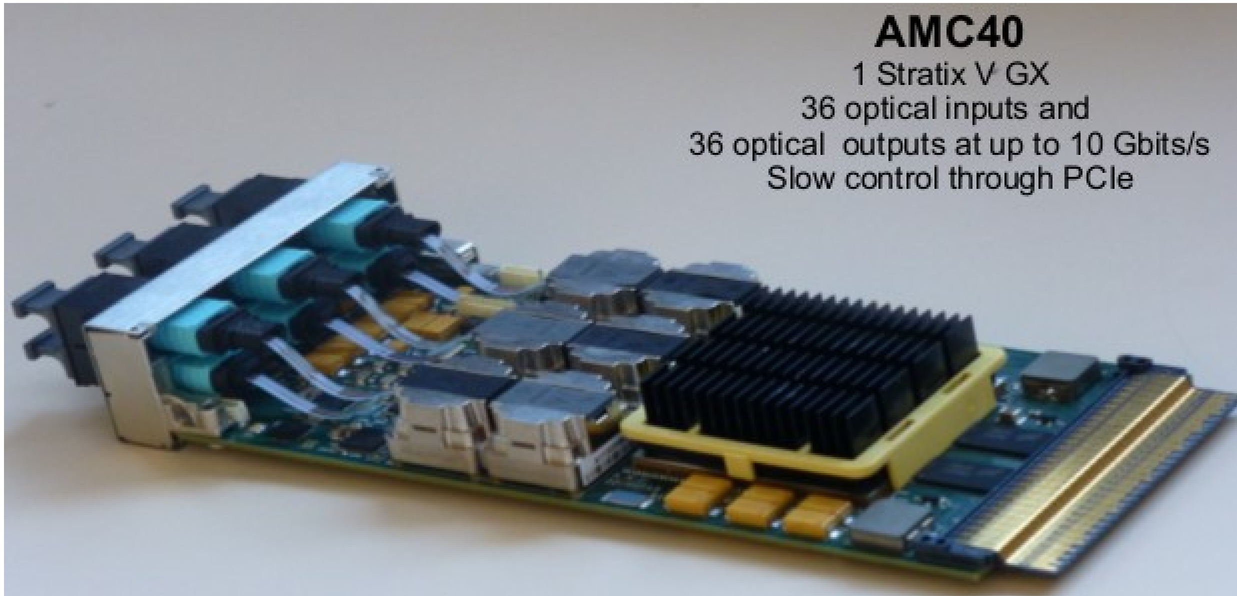
12 outputs/
inputs
@ 10Gb
ethernet



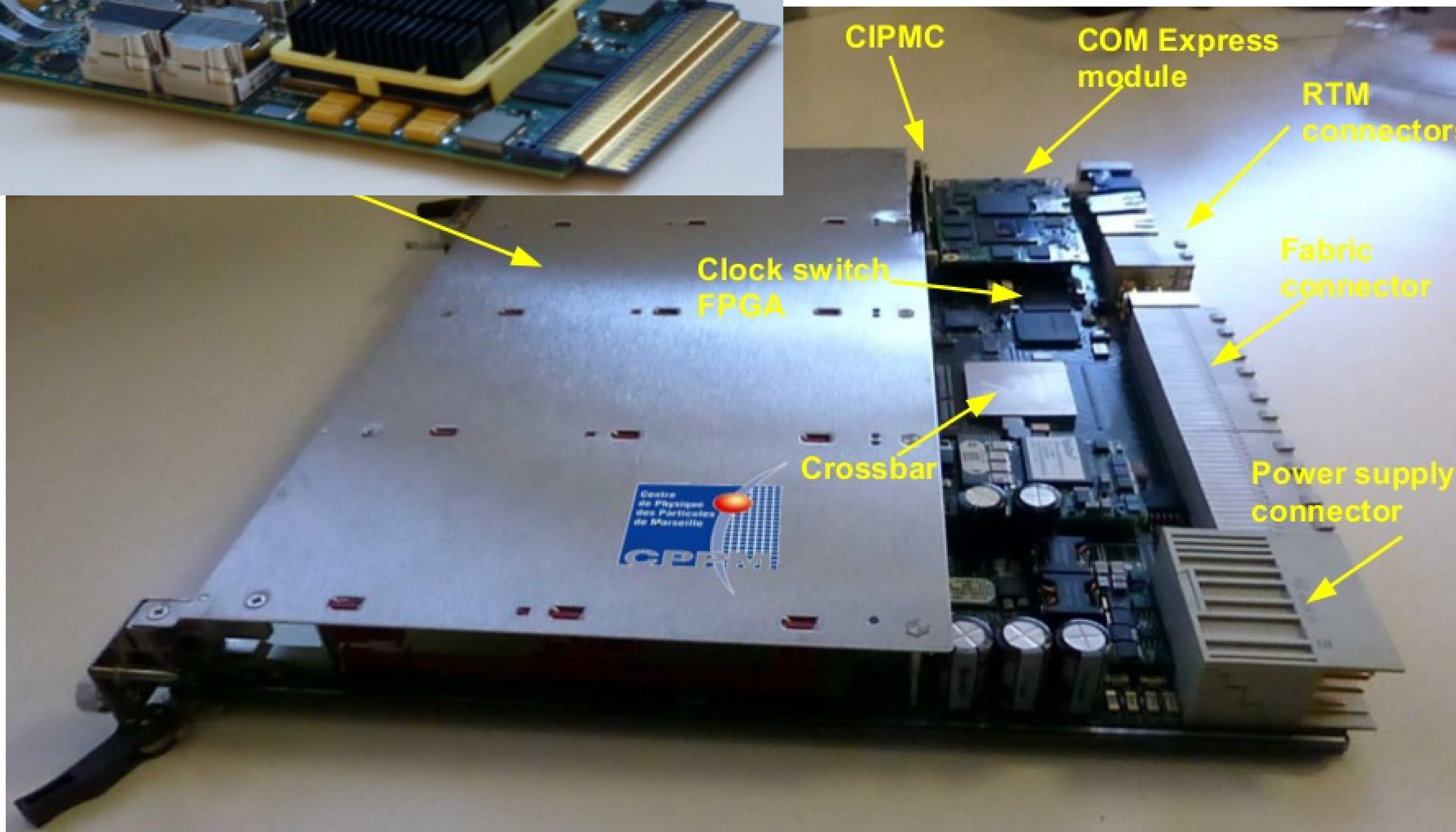
AMC

96 inputs @ 4.8 Gb → processing in FPGA → 48 x 10G ethernet ports

ATCA TELL40 & AMC40

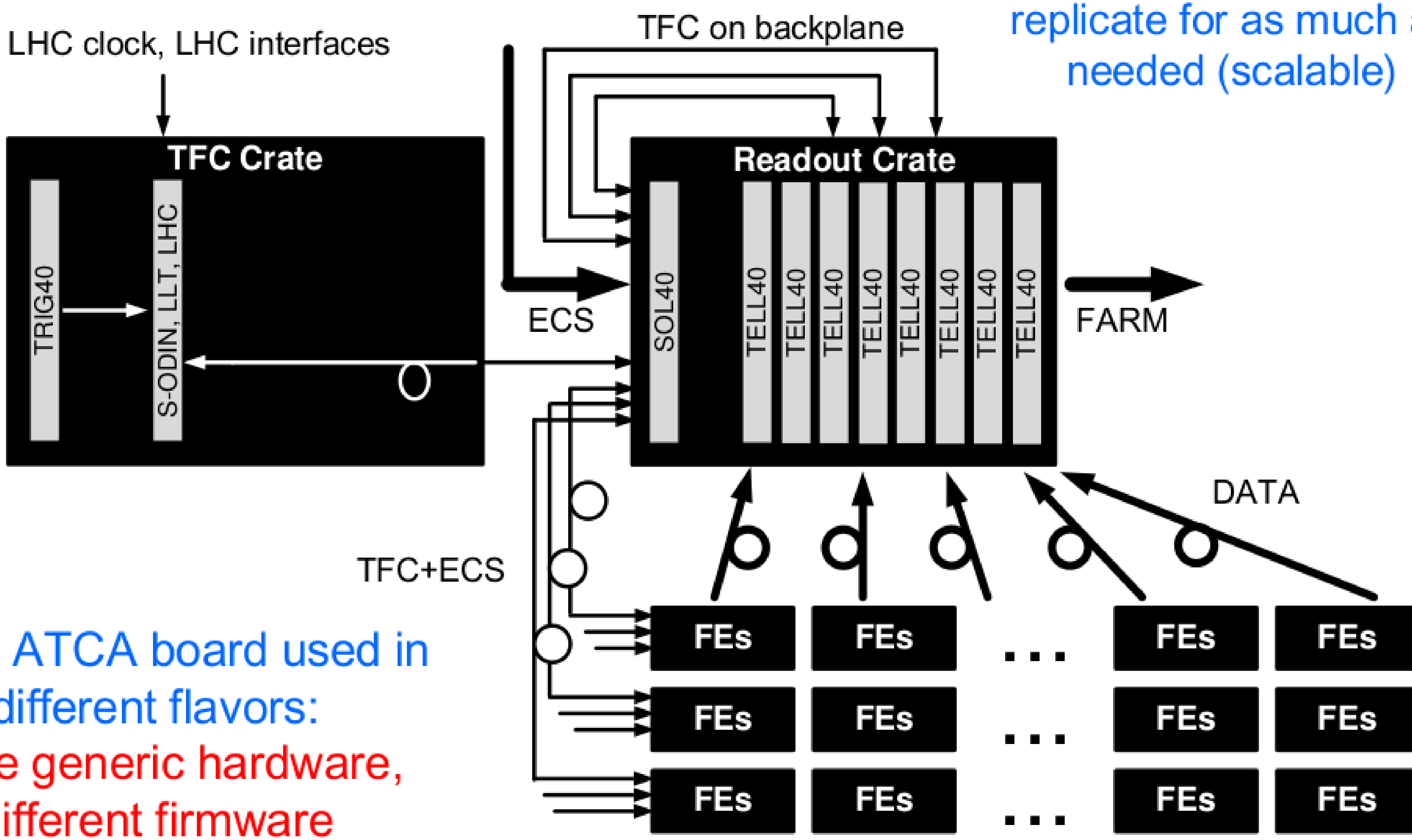


CPPM Marseille



LHCb Readout Slice

replicate for as much as needed (scalable)

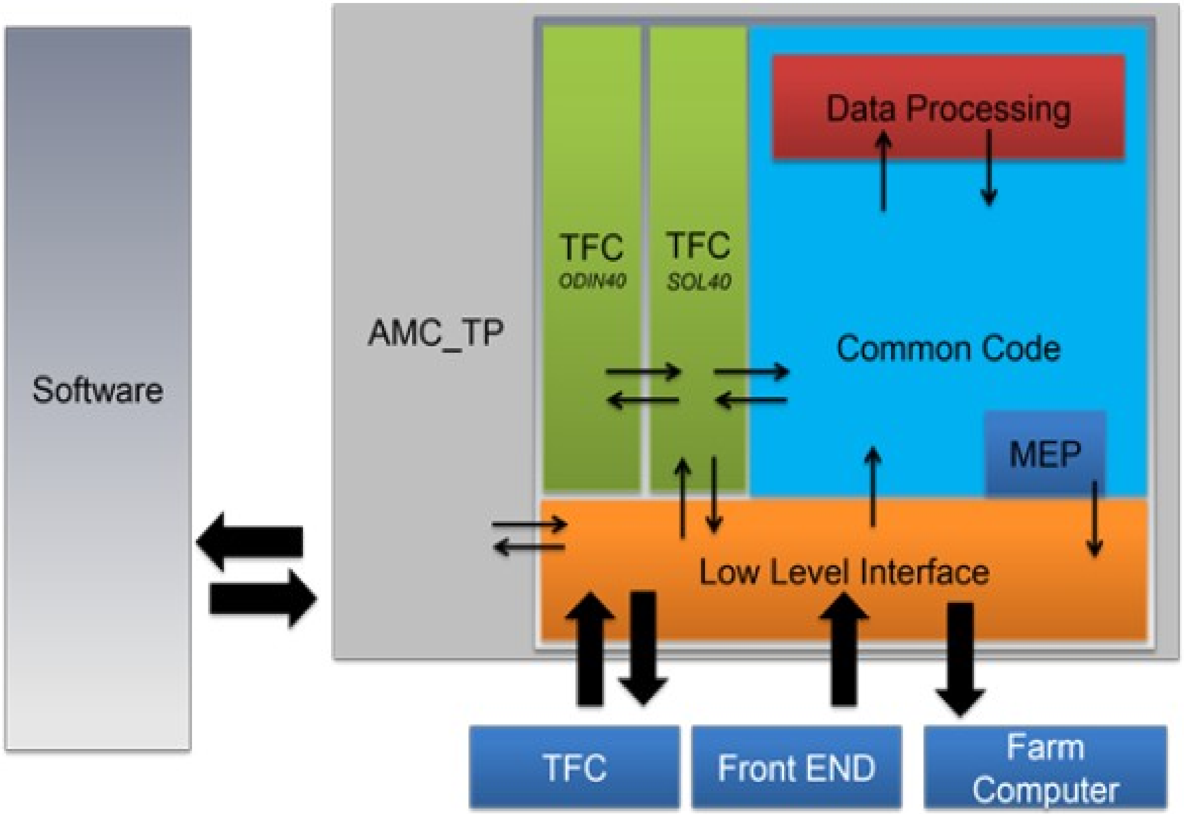


Same ATCA board used in different flavors:
same generic hardware, different firmware

Mini-DAQ System

A small readout slice on the table
→ Full AMC40 card + Credit-Card size PC + interface to FARM + all flavors of firmware in one card

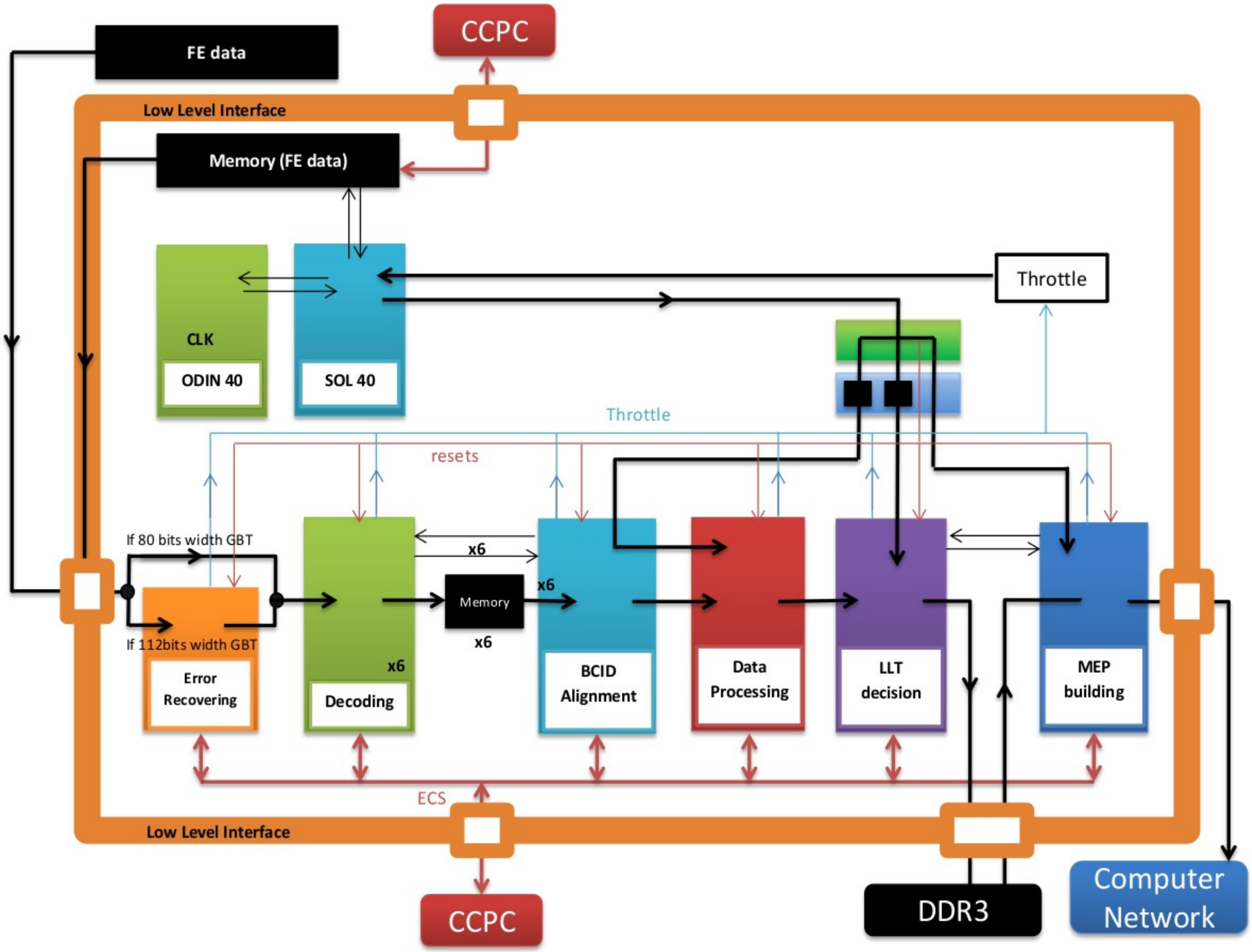
Used as a common test bench for
- developing code
- test logic
- optimize resources
- test beams



Common simulation framework based on Mini-DAQ under development

→ FE electronics will be validated both in simulation and with the Mini-DAQ to enforce specs compatibilities

Sub-detector User-code Logic



LAPP Annecy
CPPM Marseille
CERN
+ sub-detector group if specific Data processing

LAPP:

- Coordination
- Common blocks
- Generic Data Processing
- Slow Control

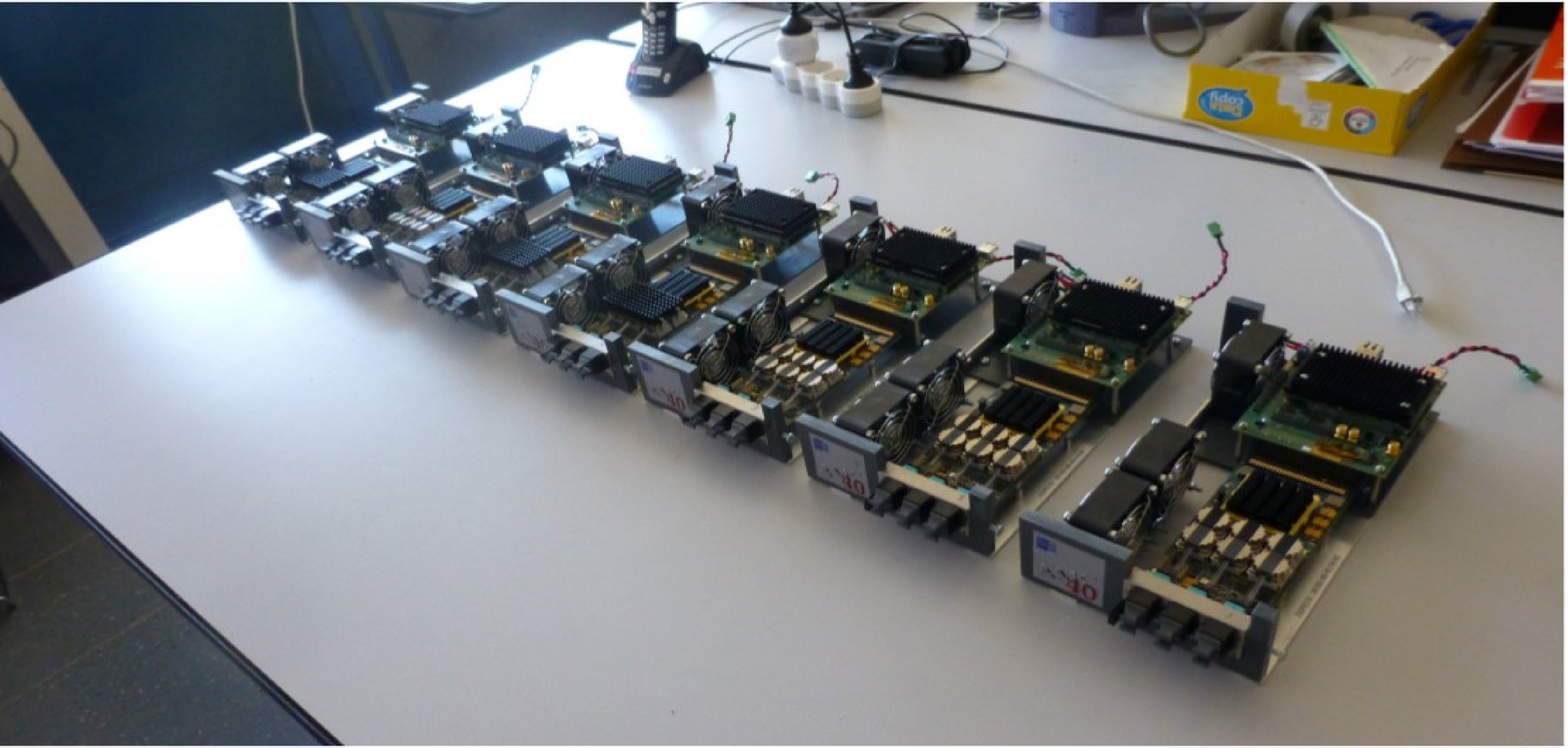
S. T'Jampens
G. Vouters
S. Cap
L. Fournier

Readout board must support asynchronous readout!

► Alignment block to realign all inputs and create an event packet

Mini-DAQ Setup: Ready

7 Mini-DAQ produced: one for LAPP :)

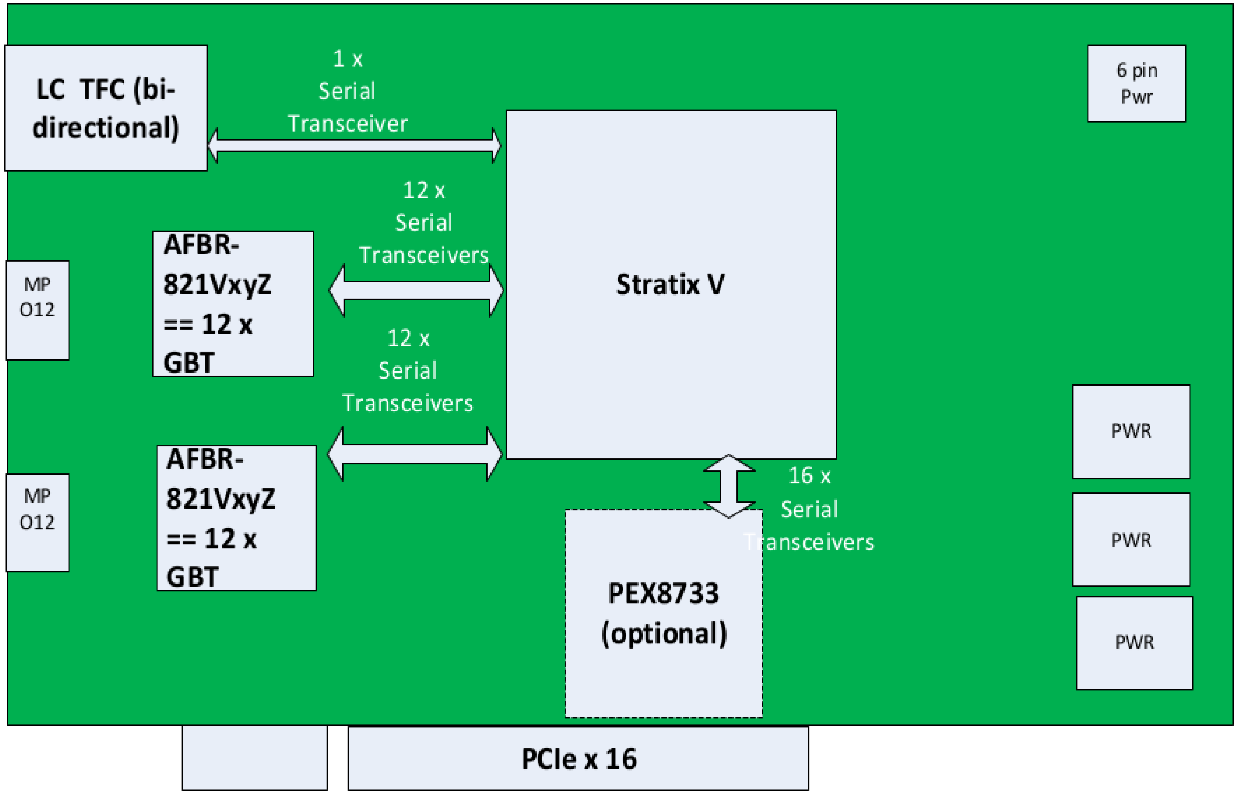


Alternative Proposal: PCIe

Instead of ATCA crates and boards

PCIe Gen3 NIC cards with FPGAs and ~150 Mb/s throughput to host PC (data-center approach)

Proposal currently under investigation



Conclusion

The LHCb Upgrade has been fully approved by CERN

Need to increase by at least an order of magnitude the amount of data to test the SM up to its theoretical uncertainties ►LHCb Upgrade (50 fb^{-1} in 10 years)

Read the detector at 40 MHz sustaining a levelled luminosity of $2 \cdot 10^{33}$ $cm^{-2}s^{-1}$

The LHCb Upgrade is a technologically challenging project and schedule is tight ►Extensive R&D ongoing, TDRs for December '13 and March '14.

The LHCb detector will be upgraded in one go during LS2 and take data during phase 2 and phase 3 (> 2022).

BACKUP SLIDES

▶ *Future prospects*

General decomposition of flavor-violating observables:

$$A = A_0 \left[c_{SM} \frac{1}{M_W^2} + c_{NP} \frac{1}{\Lambda^2} \right]$$

⬇

- The sensitivity to the energy scale grows slowly with the statistics or the luminosity of the experiment ($\sigma(\Lambda) \sim 1/N^{1/4}$)
- The interest of a given flavor obs. depends on the magnitude of c_{SM} vs. c_{NP} and on the theoretical error of c_{SM} => concentrate on clean & rare processes

In the quark sector, the present exp. accuracy ranges from 10% to 100% for loop-induced processes => we need to reach the few % level of precision (*in the few cases where the theory error is not dominant*)

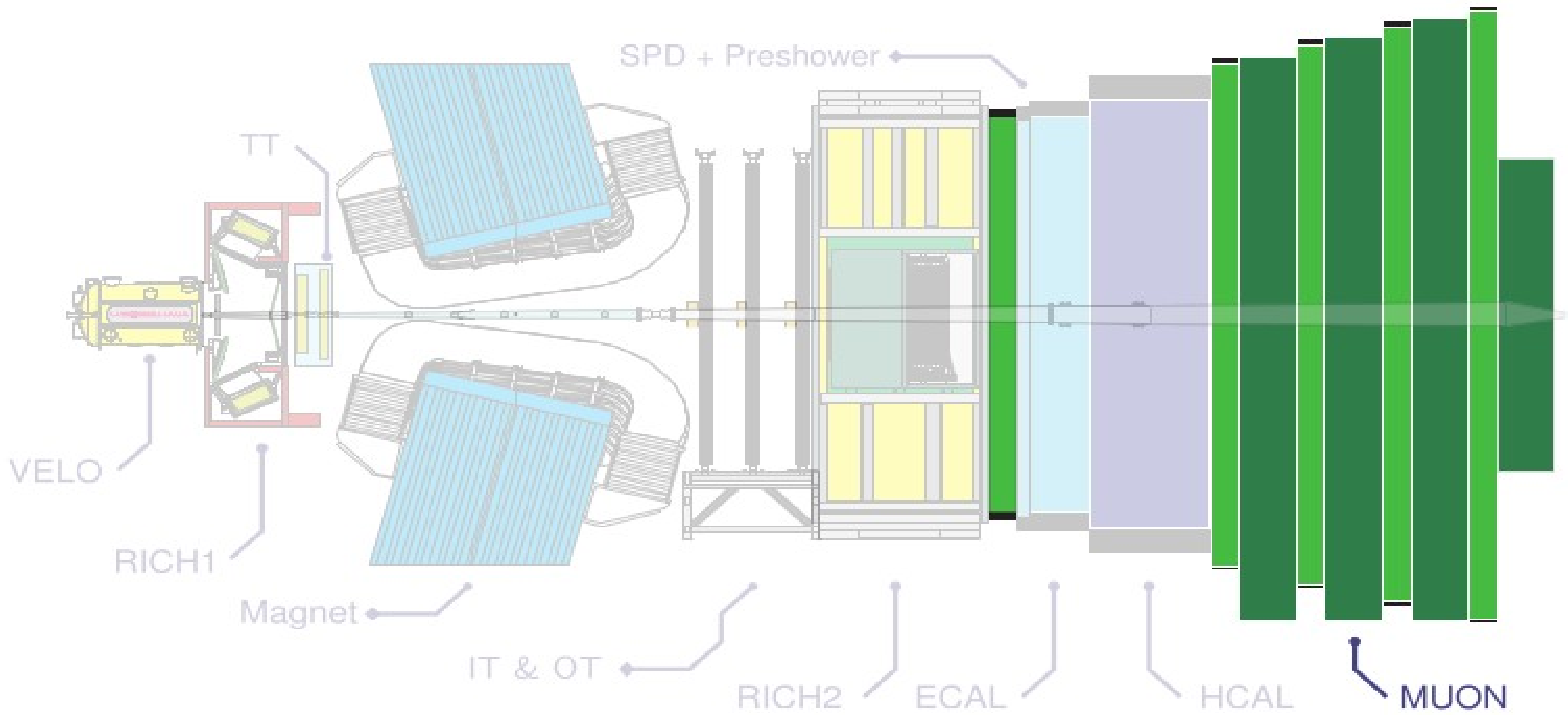
LHCb: Heavy Flavour Super Factory at LHC

- LHCb is the dedicated **flavour physics experiment** at the LHC
  - Precision studies of *flavour changing* processes and *CP violation* with b and c-hadron decays
  - test SM/indirect evidence of NP + constraints on NP flavour structure

- Advantages to run at the LHC:
  - $b\bar{b}$ cross section: **~280 μb** (~75 ± 14 μb in LHCb acceptance) at $\sqrt{s}$=7 TeV [PLB 694 (2010) 209]
  - Charm production is 20 times larger: $\sigma(pp \rightarrow c\bar{c}X)$ = **~6 mb** [arXiv:1302.2864]
    - LHCb acceptance / 1 fb^{-1}:
      - **~10^{11} $b\bar{b}$ decays** [all species produced: B^0,B^+,B_s,B_c, Λ_b,..]
      - **~10^{12} $c\bar{c}$ decays**
  - Large boost: b-hadrons fly several millimeters before decaying
    - Signature for selecting events

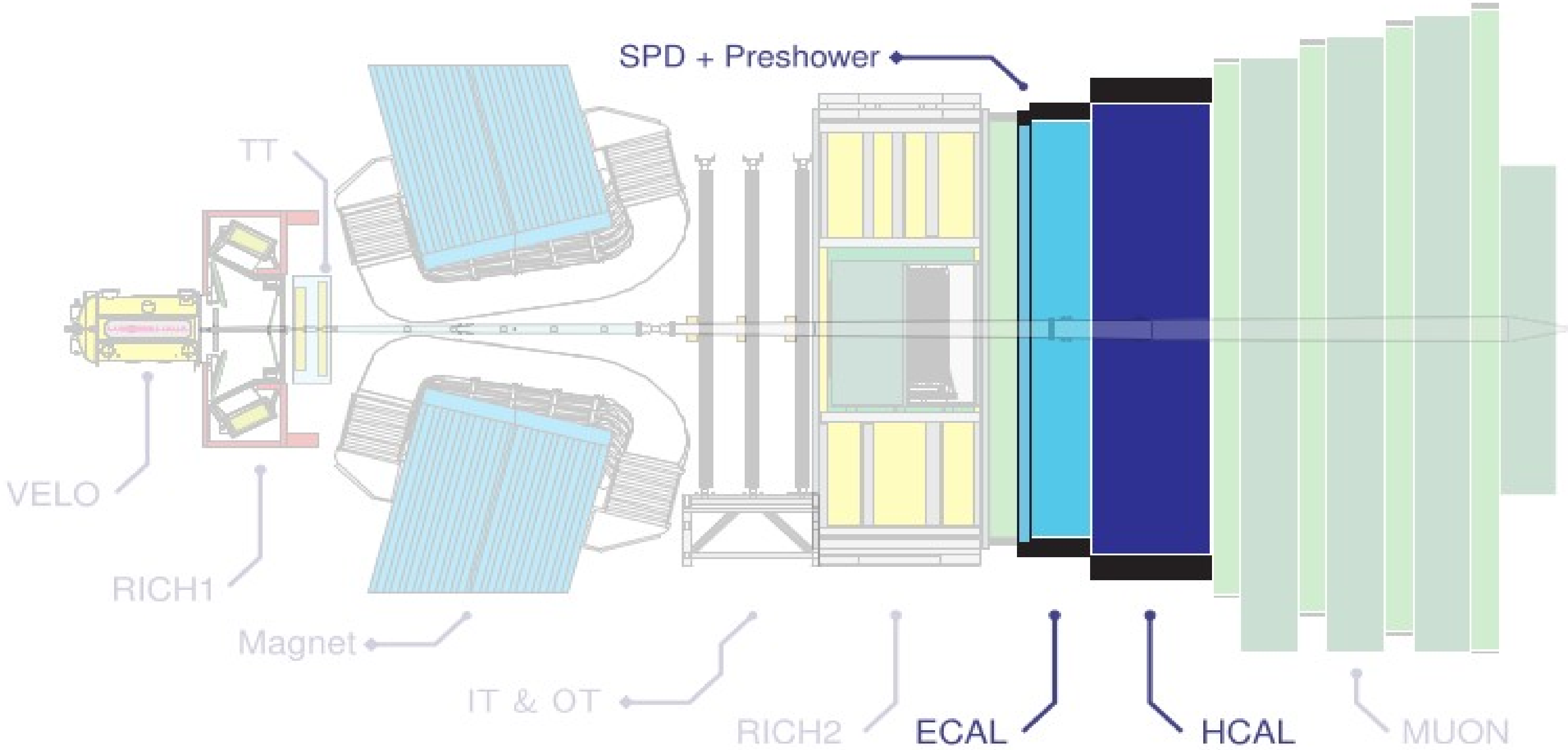
- Challenging background condition: efficient trigger essential
  - $\sigma(pp \rightarrow X)_{inel}$ = ~60 mb at $\sqrt{s}$=7 TeV [JINST (2012) P01010]

L0 muon trigger



- Momentum resolution $\Delta p/p \sim 20\%$
- Single- and Di-muon triggers: $p_{\mathrm{T}} > 1.5$ GeV, $p_{\mathrm{T}1} \times p_{\mathrm{T}2} > 1.3$ GeV^2
- 90% efficient for most dimuon channels
- L0 muon rate: 400 kHz

L0 calo trigger



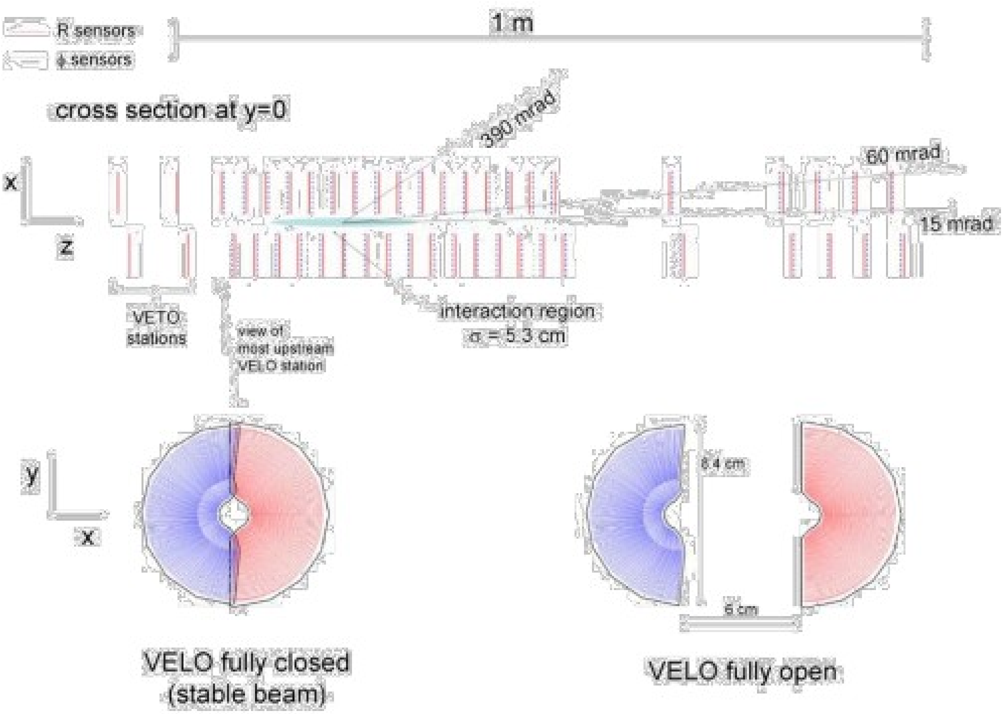
- Selects High E_{T} hadrons, $\mathrm{e}^{\pm}$, γ
- Threshold $E_{\mathrm{T}} > 2.5 - 3.5$ GeV
- Preshower and SPD discriminate between $\mathrm{e}^{\pm}$, γ

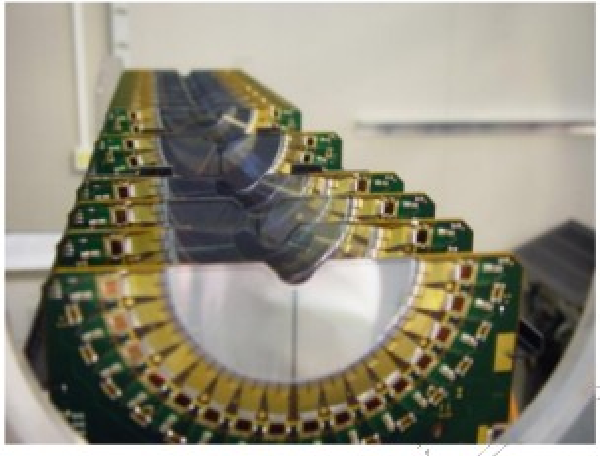
- Hadronic B-decay efficiency 50%
- 80% efficient for radiative $\mathrm{B} \to \mathrm{X}\gamma$ decays
- L0 $\mathrm{e}^{\pm}/\gamma$ rate: $\sim$150 kHz
- L0 hadron rate: $\sim$450 kHz

Current LHCb Vertex Detector

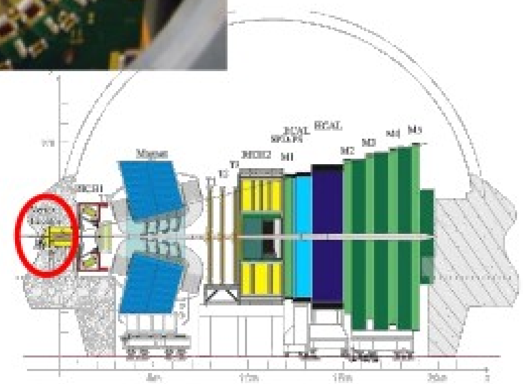
Current Vertex Detector (VELO) is at the heart of LHCb tracking, triggering and vertexing

- Excellent performance, reliable, cluster efficiency >99.5%, best hit resolution down to <4μm
- Movable device! ~50mm to ~5mm close to LHC beams when in collisions (autonomously…)





Si-strips measuring r and ϕ



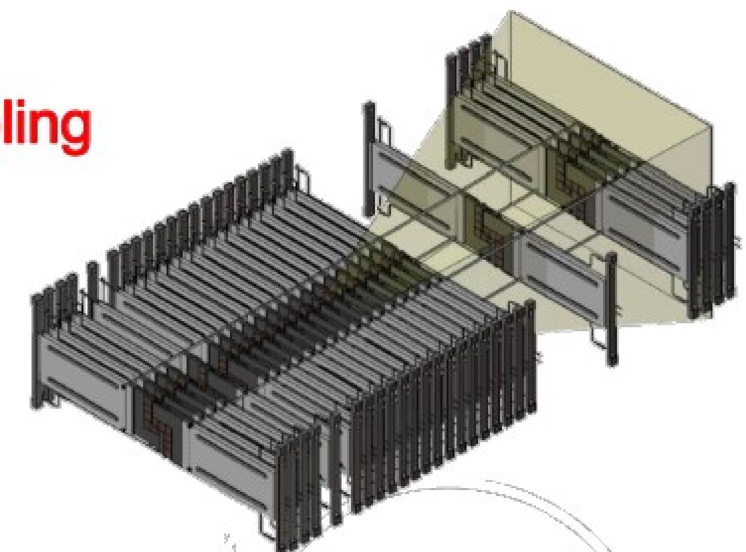
New LHCb Vertex Detector

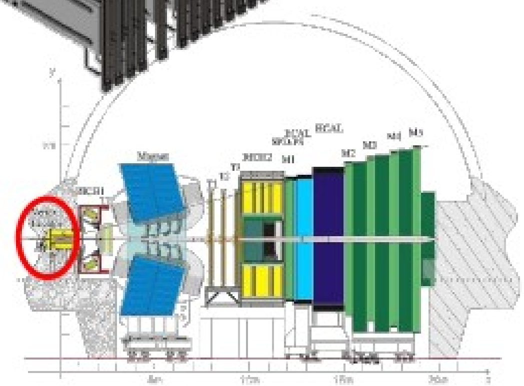
Future VELO must maintain same performance, but in harsher conditions

- Low material budget, cope with > radiation damage, deal with > multiplicities
- Trigger-less readout ASICs and provide fast and efficient reconstruction at HW level

→ Recent technology reviews favored the choice of a

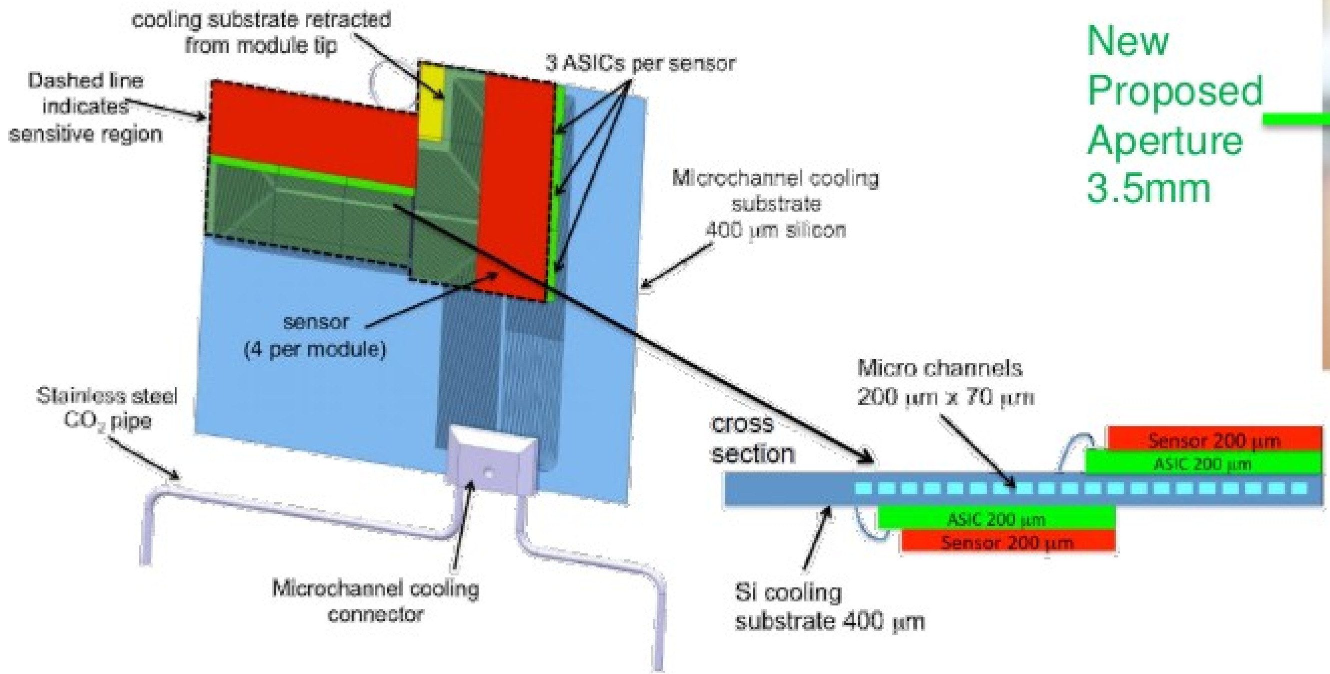
Si-pixel detector with microchannel cooling

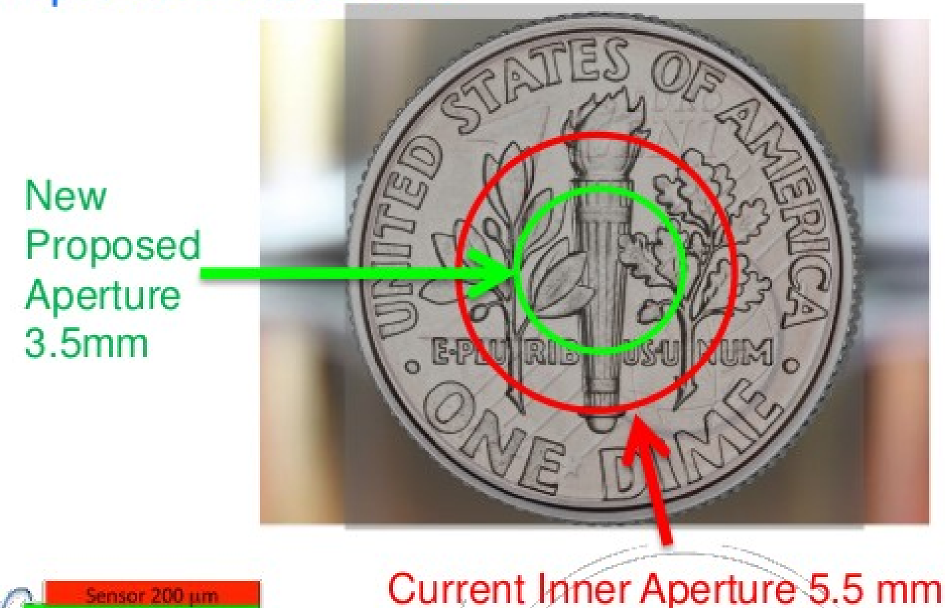


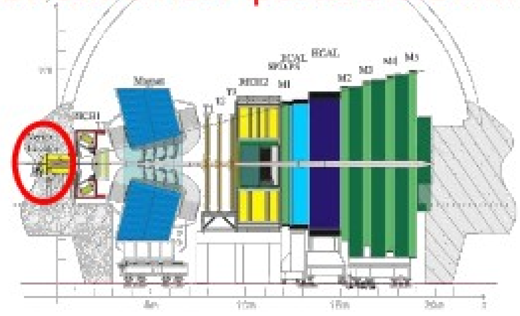


New LHCb Vertex Detector

- Pixel Silicon detector modules cooled down with fluid (bi-phase CO_2) which passes under the chips in etched microchannels (ΔT = 4-7 °C between fluid and sensor)
- Getting closer to beam (agreed with LHC!) to improve IP resolution!



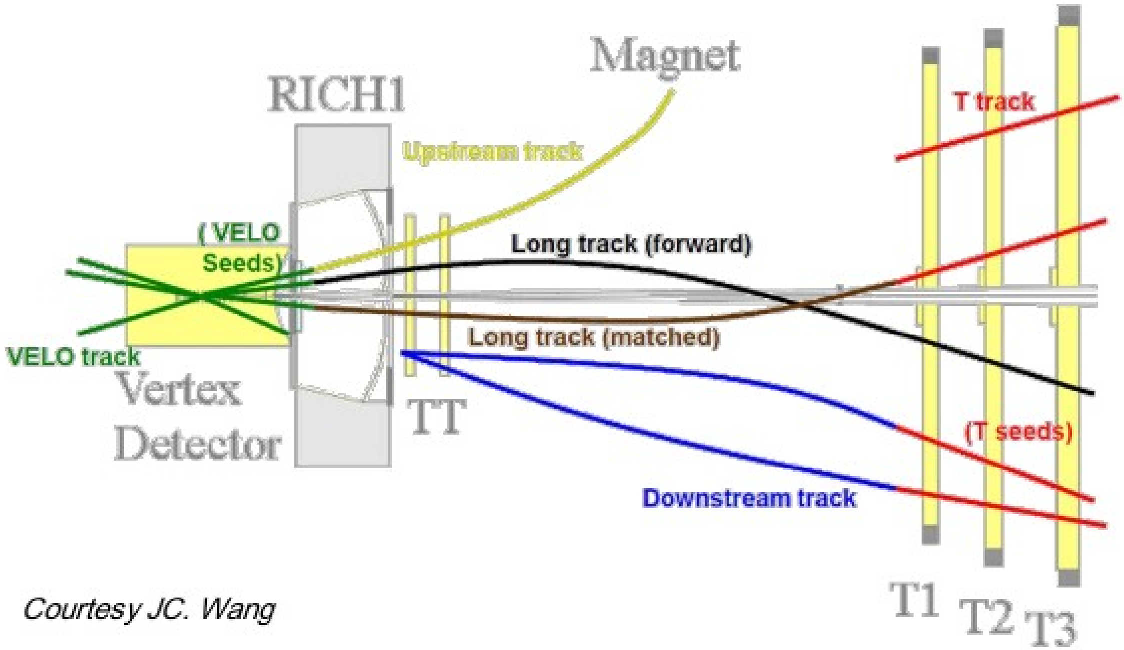




Current LHCb Tracking system

Present Tracking System will be upgraded:

- VELO + TT (Si-strip) + DIPOLE (no change) + IT (2% inner area, Si) / OT (Straw Tubes)



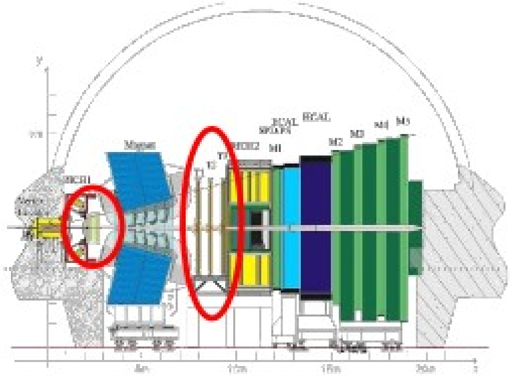
Courtesy JC. Wang

Current pattern-recognition based on current tracking system would not be efficient in upgraded scenario

- Too high occupancy in central region
- R&D for different solutions

  → for downstream and upstream tracking

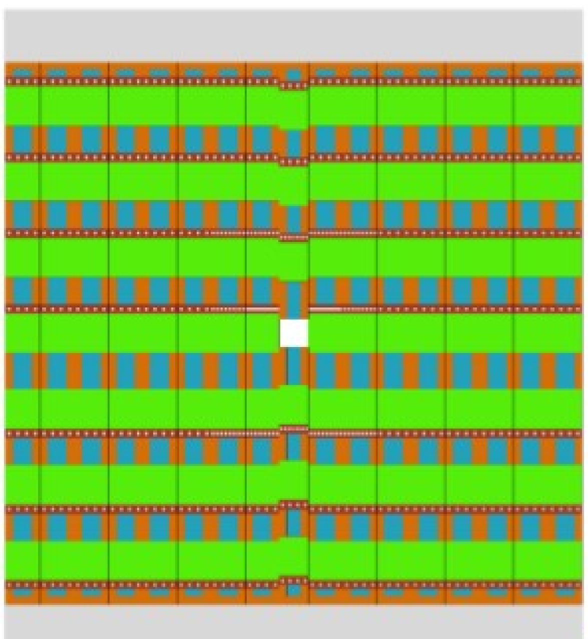
Sidenote: R&D in increasing Dipole field (x1.8 Bdl)

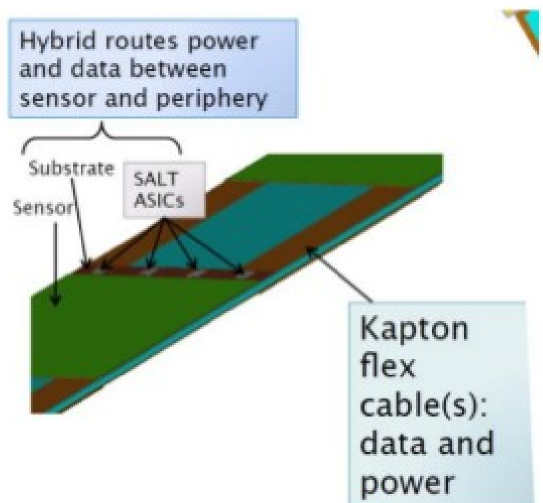


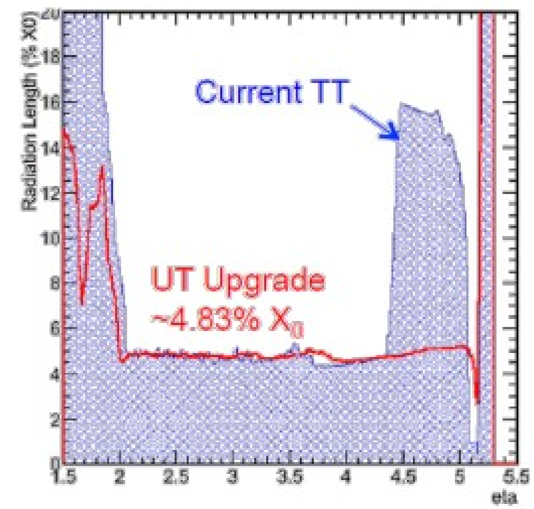
New Upstream Tracking Stations

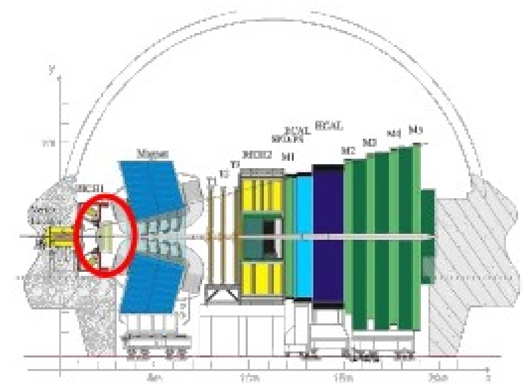
R&D upstream:

- Replace current TT with UT (*Upstream Tracker*) , also based on Si-strips
  - reduced thickness
  - finer granularity
  - improved coverage (innermost cut-out at 34 mm)
  - much less material budget (<5% X_0)







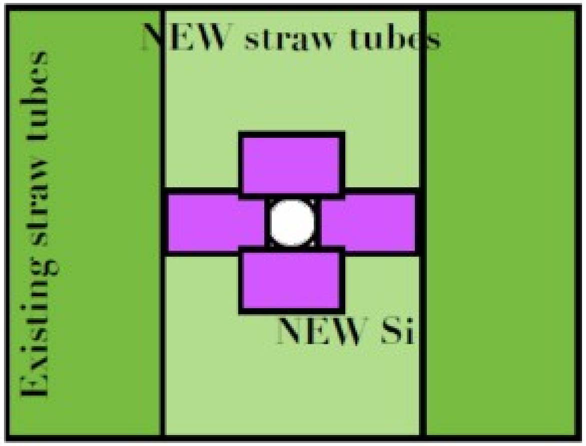


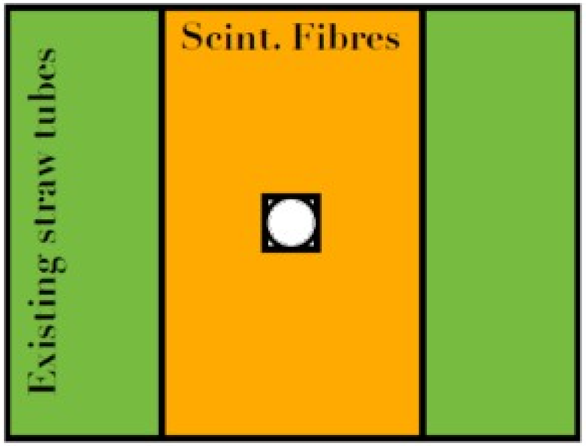
New Downstream Tracking Stations

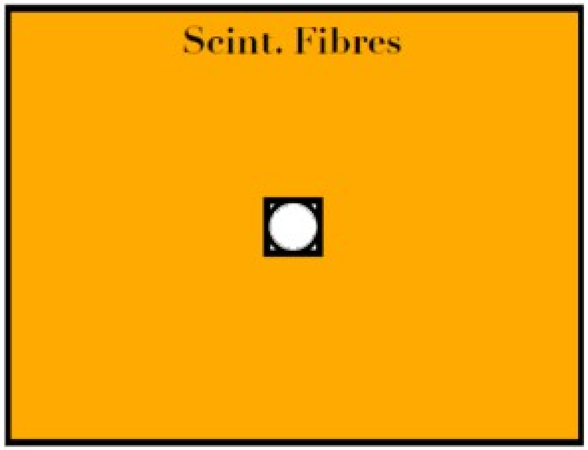
R&D donwstream:

- Various options still on the table
  - all aimed at reducing the occupancy in the inner region

Baseline option!







Enlarged, thinner and lighter IT

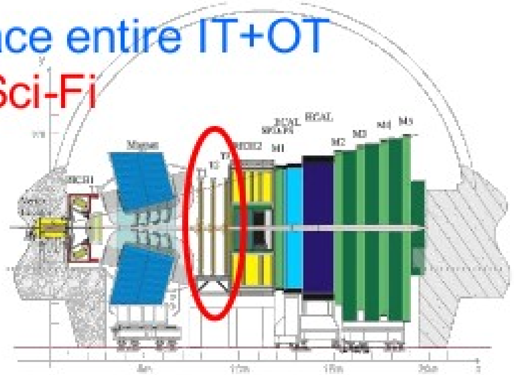
→ Based on Si-strip

→ New OT straw tubes in central region

Replace central region with Central Tracker (Sci-Fi detector)

→ Based on Scintillating fibers and SiliconPM

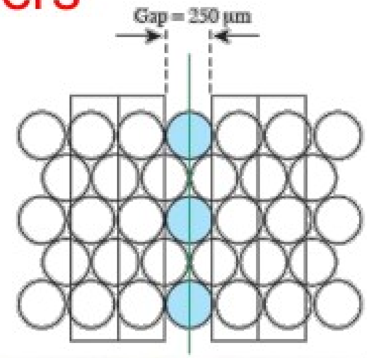
Replace entire IT+OT with Sci-Fi

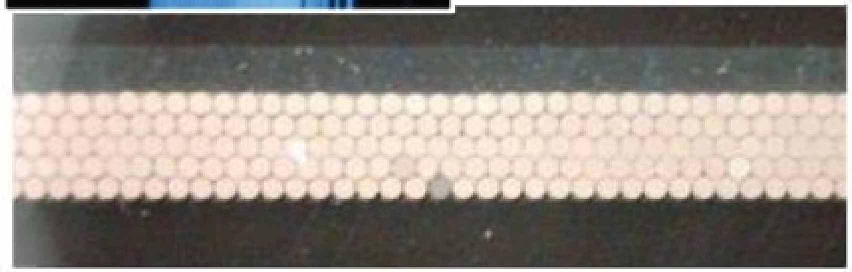


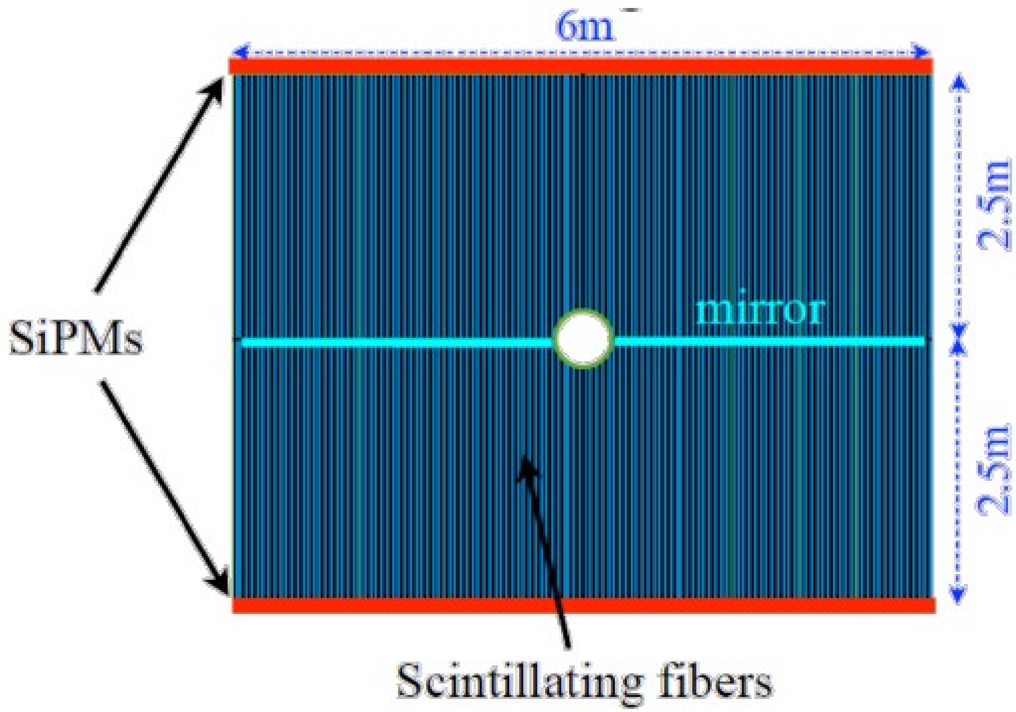
New LHCb Sci-Fi detector

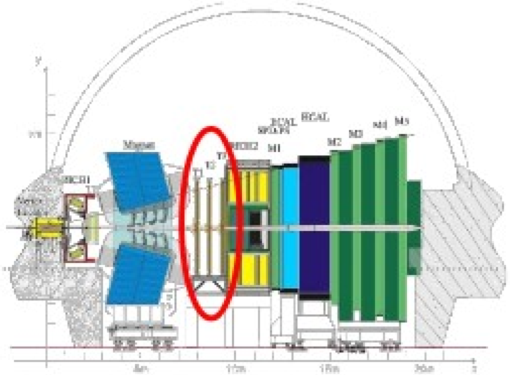
Build a completely new detector based on Scintillating Thin Fibers

- Blue-emitting multi clad fibers, laid down as a mat
- 2.5m long, 250 um diameter (2.8 ns decay time)
- 12 layers of modules in different layout (x-u-v-x)
- read out with SiPM (at -50C): new trigger-less FE





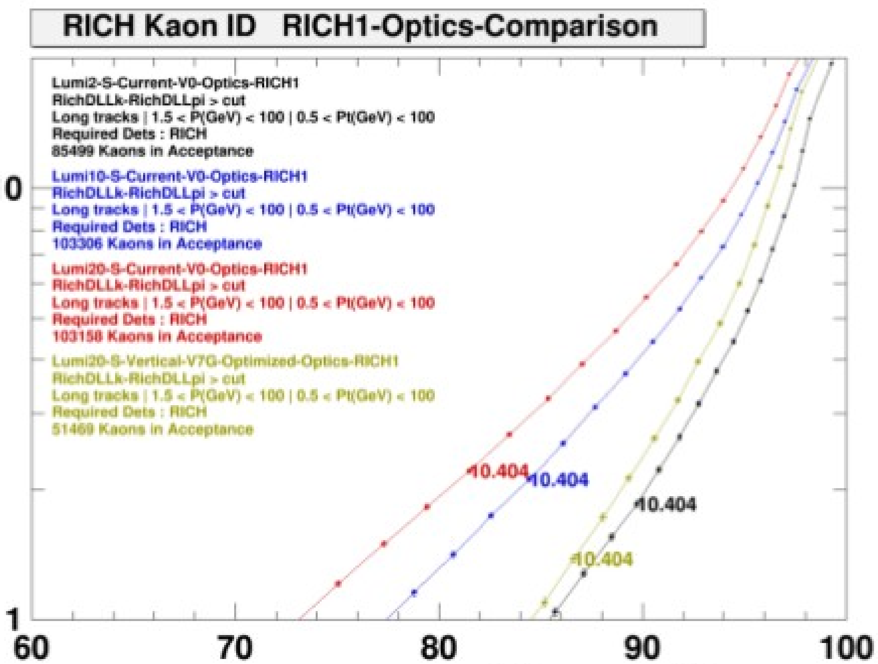




Upgraded Particle ID

Present Ring-Imaging Cherenkov (RICH) detector will be upgraded:

- Current RICH1 (aerogel C_4F_{10}) + RICH2 (CF_4)



Main changes:

Remove aerogel radiator

- to compensate for increased occupancy

Remove Hybrid-PhotoDetectors (HPD) with Multi-AnodePMTs

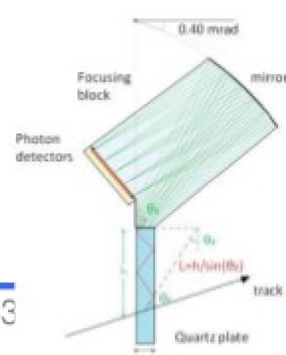
- Hamamatsu R11265 with 80% active area

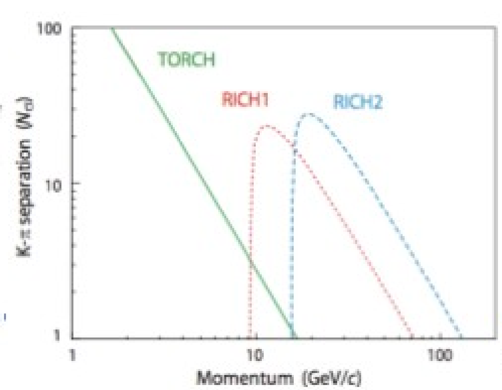
Front-End electronics will be redeveloped

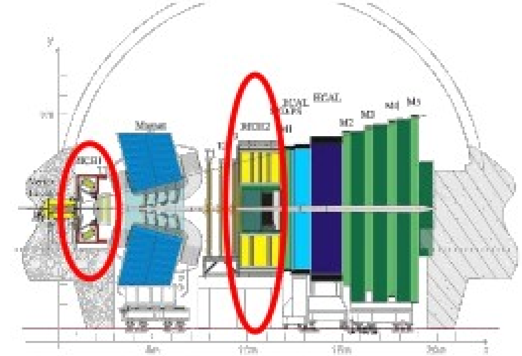
R&D:

Add new detector TORCH

- 1-10 GeV/c







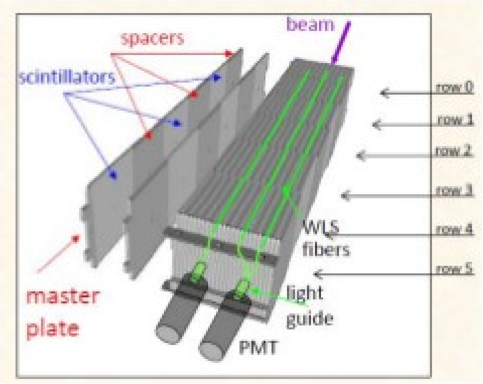
Upgraded Calorimeters

Present Calorimeters detectors will be kept:

- ECAL (Shashlik 25 X_0 Pb + scintillator)
- HCAL (TileCal Fe + scintillator)

→ PreShower / ScintillatingPadDetector (PS/SPD) will be removed

HCAL



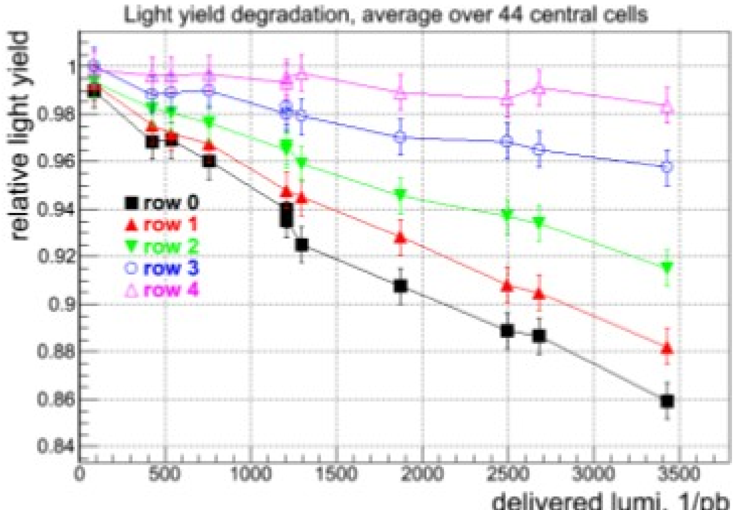
Main changes:

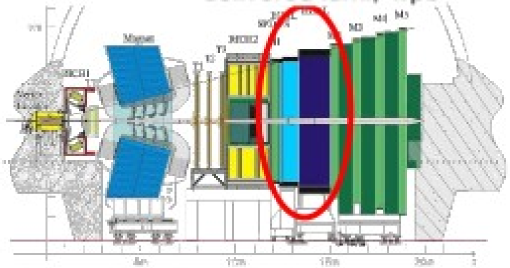
PMT gain will be reduced by a factor 5

- to reduce ageing due to higher luminosities

Front-End electronics will be redeveloped

- to be compatible with the reduced gain (R&D)
- to be compatible with trigger-less readout





Upgraded Muon Detectors

Present Muon detector will be kept:

- 4 layers (M2-M5) of Multi-Wire Proportional Chambers (MWPC)

→ first layer of Muon Detector (M1 – used in first-level trigger, with GEMs) will be removed

Main changes:

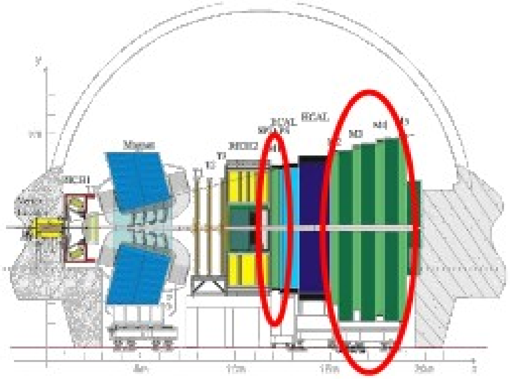
Front-End electronics will be redeveloped

- to be compatible with trigger-less readout

R&D:

Replace inner part of M2 (closest to IP) with GEMs detectors

- to have higher-granularity



InfiniBand

- Driven by a relatively small, agile company: Mellanox
- Essentially HPC + some DB and storage applications
- Only competitor: Intel (ex-Qlogic)
- Extremely cost-effective in terms of Gbit/s / $
- Open standard, but almost single-vendor – unlikely for a small startup to enter
- Software stack (OFED including RDMA) also supported by Ethernet (NIC) vendors
- Many recent Mellanox products (as of FDR) compatible with Ethernet