Groupe de travail xTCA DAQ de l'IN2P3

Résumé workshops

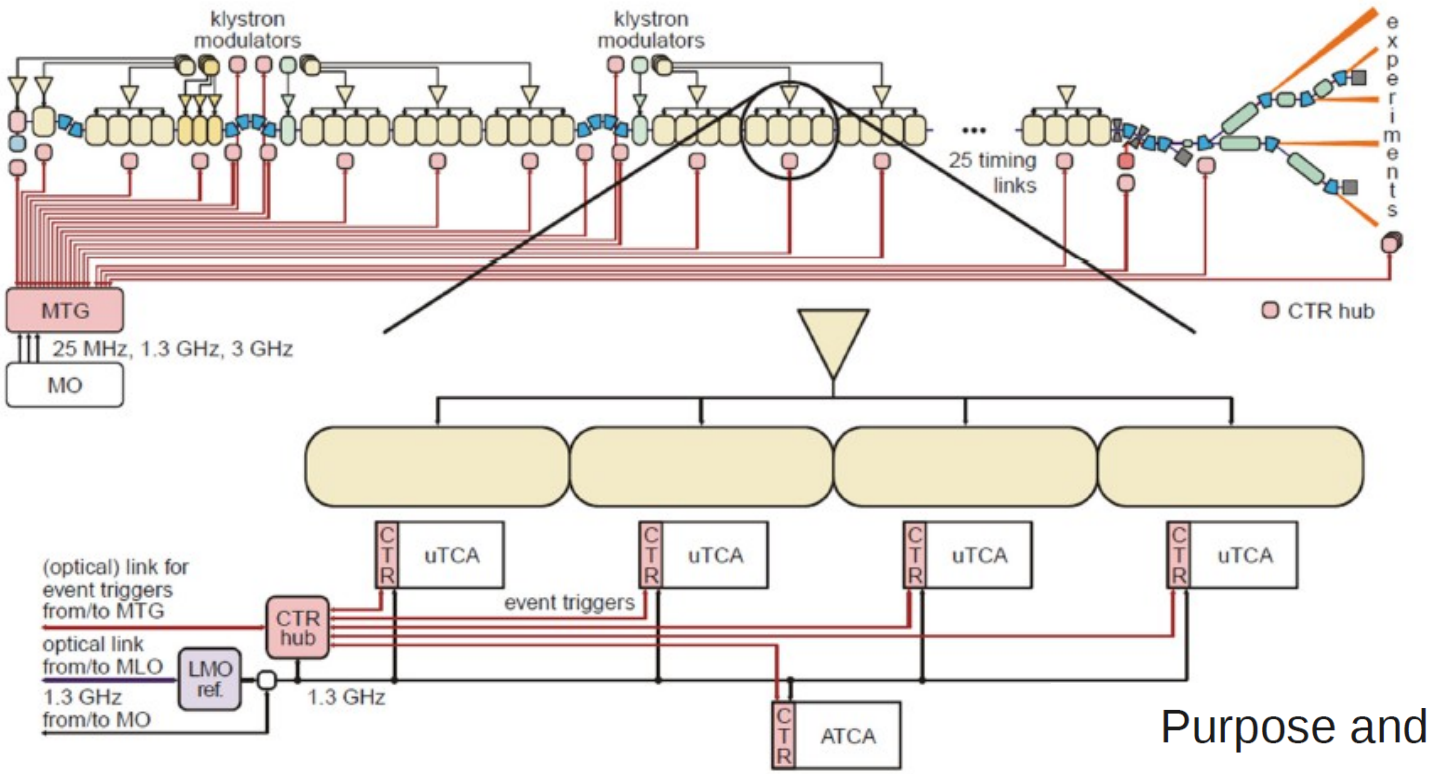
J.-P. Cachemiche
CPPM

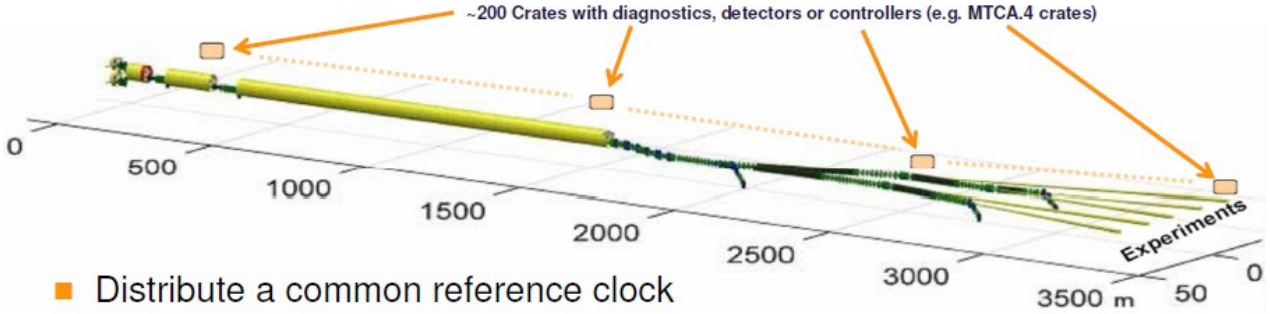
Sommaire

- **Résumé xTCA workshop RT2012**
- **Résumé xTCA workshop TWEPP2012**
- **Résumé journée xTCA Ecole électronique IN2P3**

xTCA Workshop RT2012

Distribution d'horloge XFEL





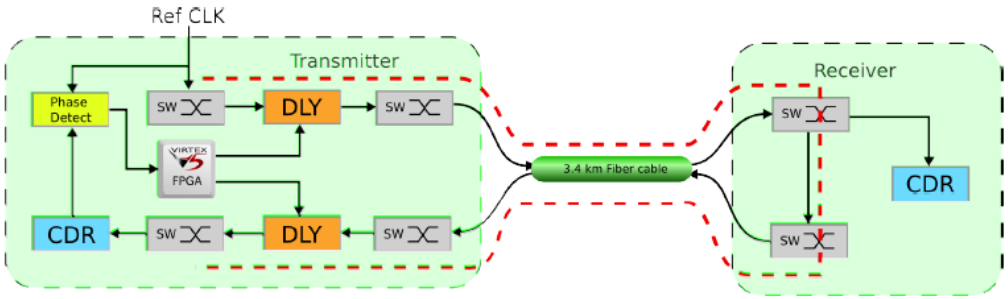
- Distribute a common reference clock

Purpose and requirements

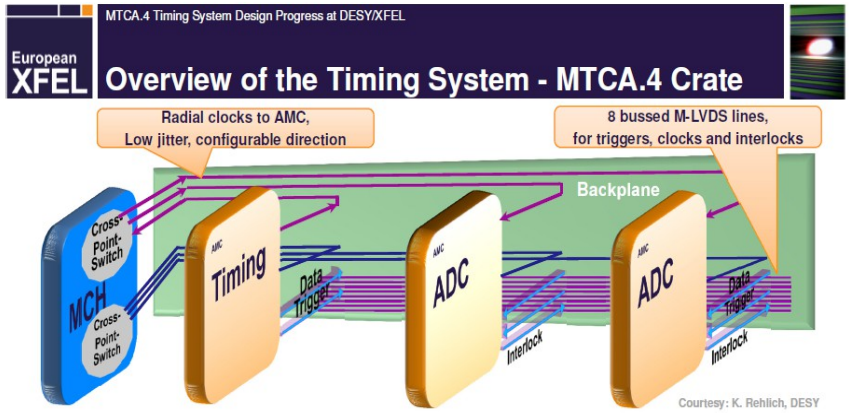
- Distribute clocks and trigger information to the European XFEL accelerator system and experiments.
- Deliver the 1.3 GHz main RF-frequency and other derived frequencies.
- Synchronize the clock-phases and keep them drift free, with a total jitter <5 ps (RMS).
- Deliver clocks and triggers through the backplane and through the front panel.
- Cost efficiency

Distribution d'horloge XFEL

Basic principle of the drift-compensation



- Total delay is 2x (fiber delay + PCB track)
- Tx and Rx path is kept equal and constant
- Clock phases and temperatures are measured at kev locations
- Drifts are detected by phase-detectors.
- Total loop is adjusted by delay components.
- Drifts are assumed to be relatively slow
- Loop-control implemented in an FPGA/MCU



- Timing module generates clock and distributes them via the MCH
  - Well terminated point-to-point
  - Performance limited by switch in MCH → Solved in next Generation
- Generated triggers are distributed via bus lines
- Meta data is distributed serially with synchronous clock via bus lines
- All these signals are also available via connectors on the face plate

Attila Hidvégi, Stockholm University - Physics Dept.

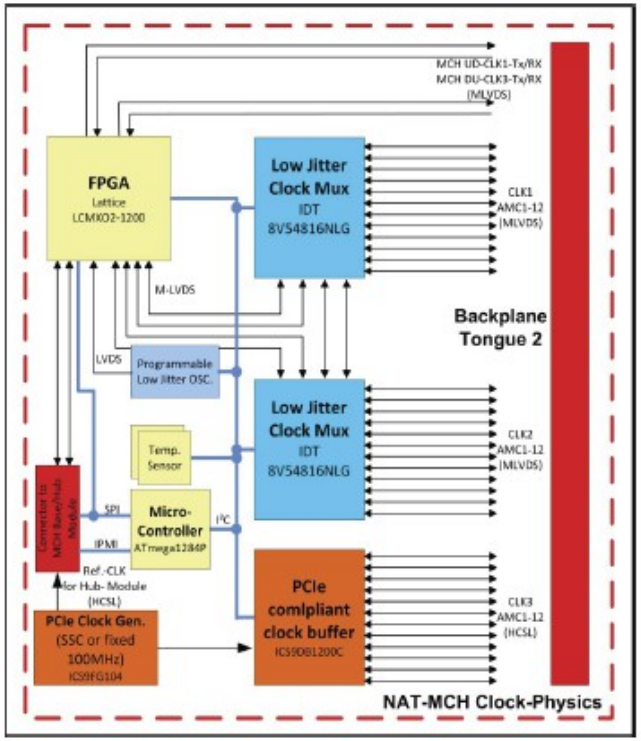
AMC prototype results

- <1.5 ps (RMS) random jitter on some of its outputs
- <120 fs (RMS) loop-time stability, <600 fs (p-p)
- Triggers delivered with 1.3 GHz phase resolution
- Test and support software has been developed for the board

Distribution d'horloges

NAT-MCH
Clock for Physics

Vollrath Dirksen
MTCA.4
System Design, MCH,
Multi-clustering, Testing



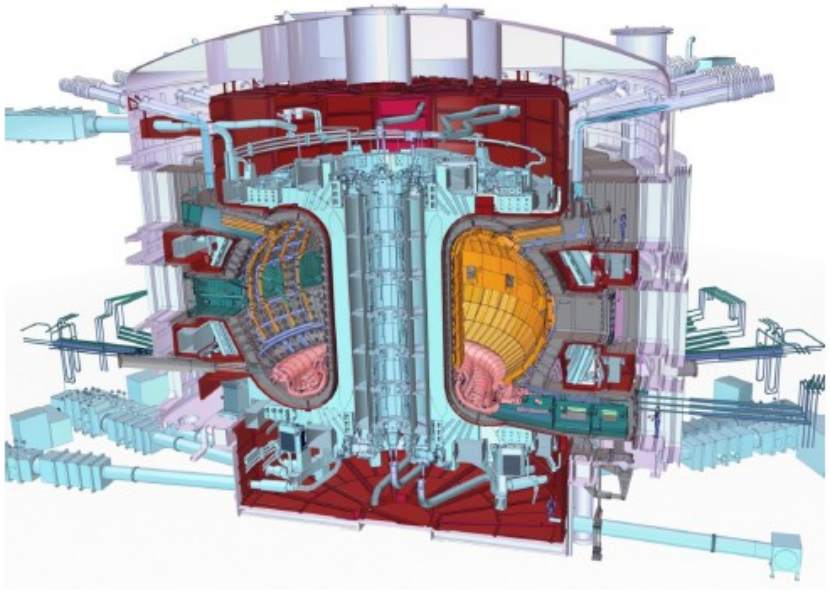
Physics Clock Mezzanine

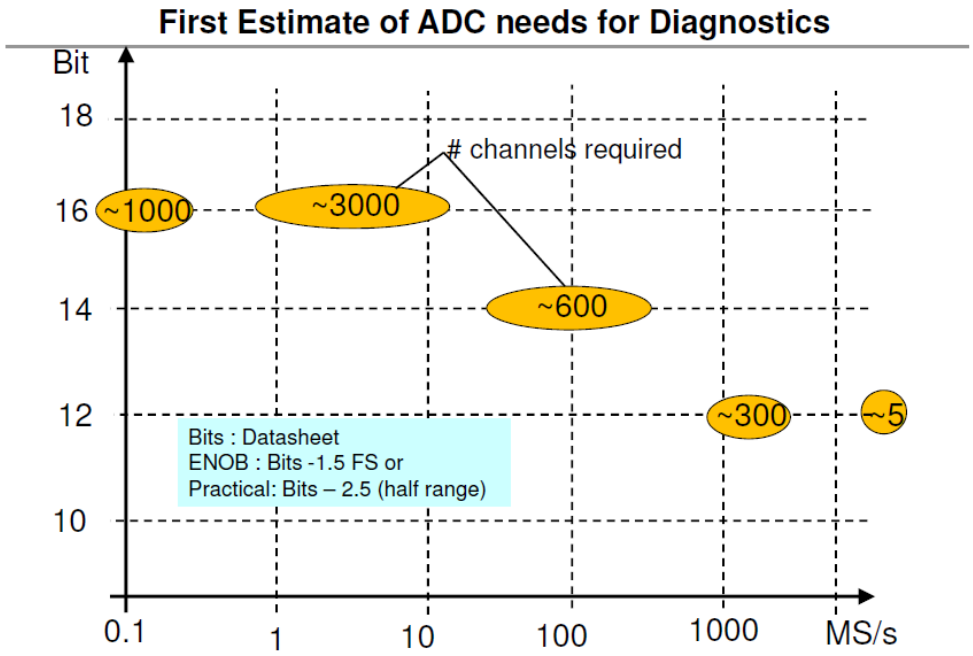
The development of this module is driven by the demands of physics group requiring very low jitter and constant latency. These features are realised by using a specialized Clock Multiplexer developed in cooperation with IDT (Integrated Device Technology Inc.).

Key Features

- CLK1 connections for all 12 AMC multiplexed by one device.
- CLK2 connections for all 12 AMC multiplexed by one device.
- two direct multiplexer interconnections
- fixed low jitter reference clock
- connection to front panel clock interface
- PCIe reference clock distribution for 12 AMCs via CLK3 (AMC.0 R2.0 - FCLKA)

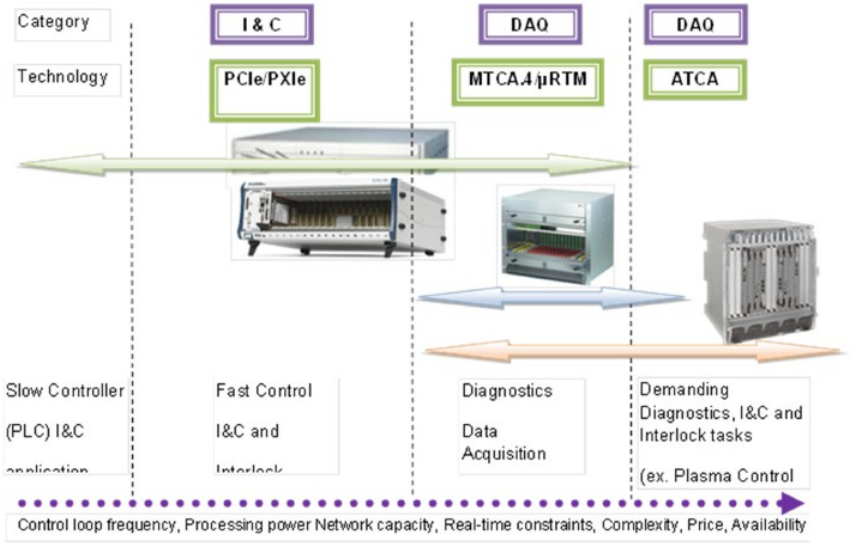
ITER





IO approach to deal with it…

- Develop global roadmap for fast controllers



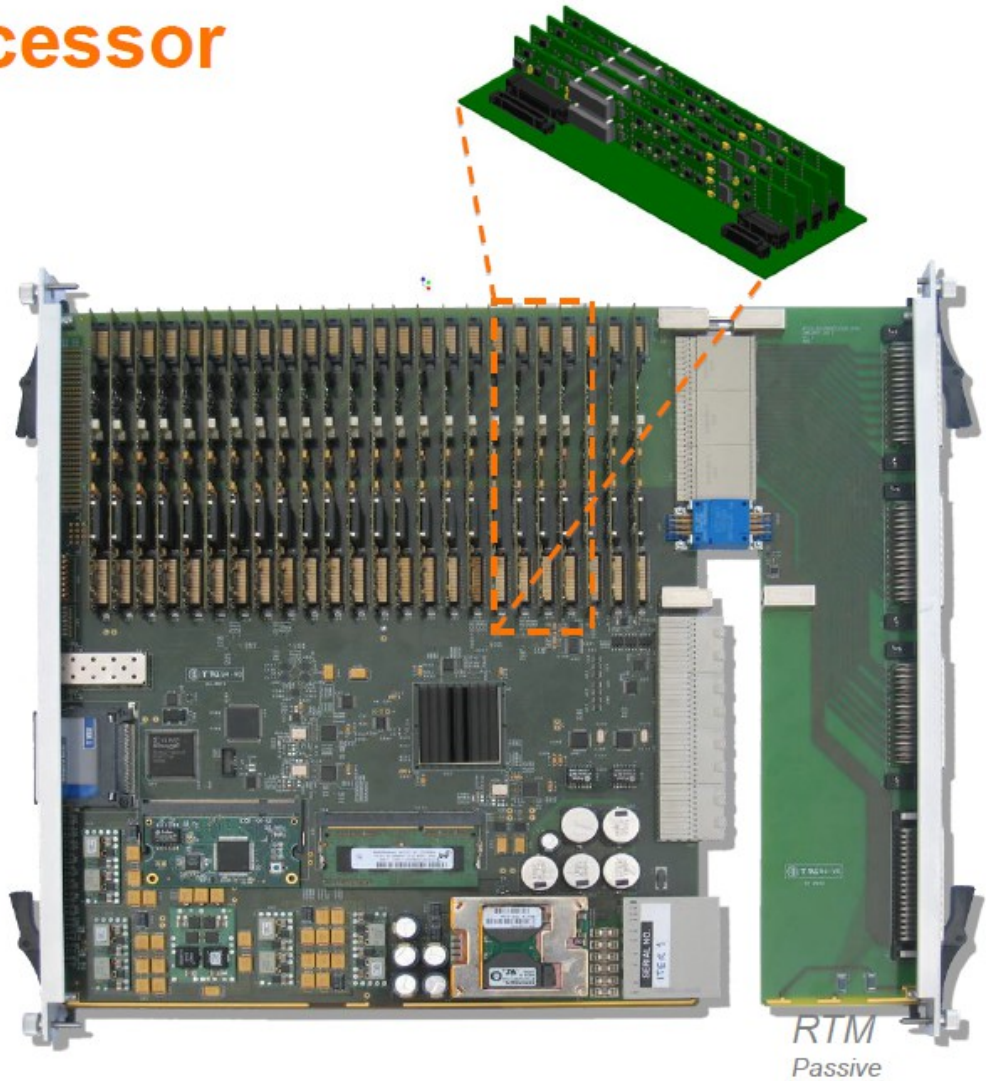
ITER

ATCA-IO-Processor

48 IO channels

ADC module
with ADC x2 and chopper mode

DAC module
with DAC x2



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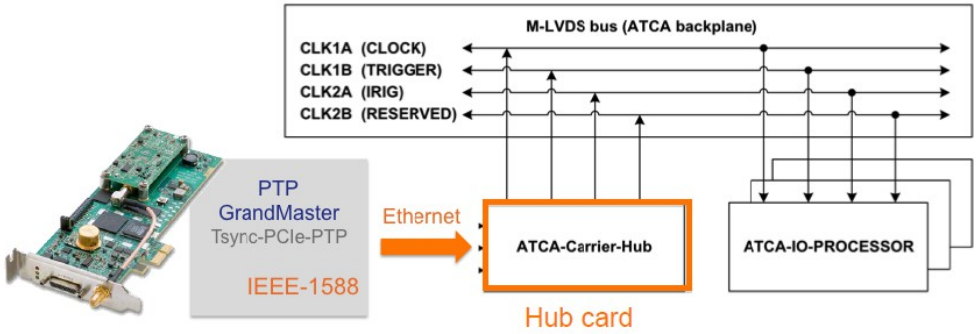
B. Gonçalves | Berkeley, June 10, 2012 | xTCA Workshop

ITER

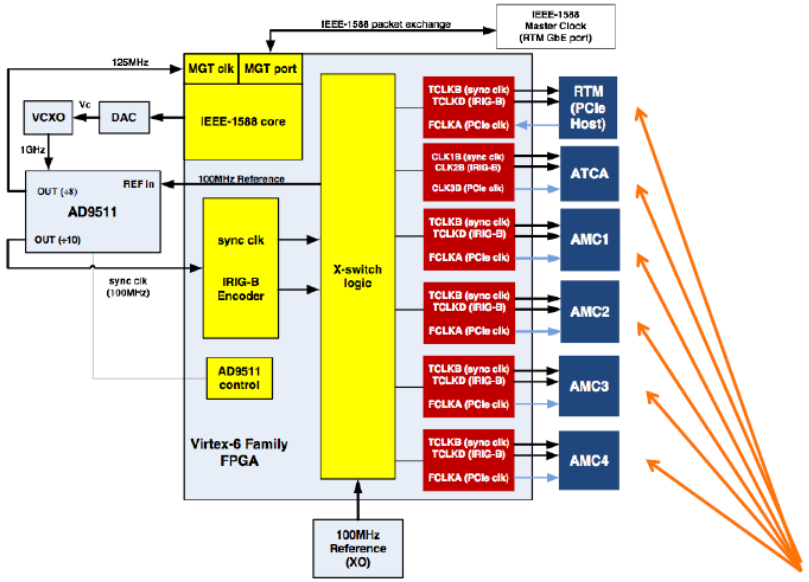
ATCA backplane synchronization | signals distribution



- Data time stamping using IRIG time distributed by hub card
  Internal time counter synchronised with IEEE-1588-2008 card
- Programmable timing unit for generating specific clock or trigger sequences for sampling
- Common synchronized clock

White Rabbit PTP core being developed

Timing signals are managed and routed by a crosspoint-switch implemented on a Virtex-6 FPGA

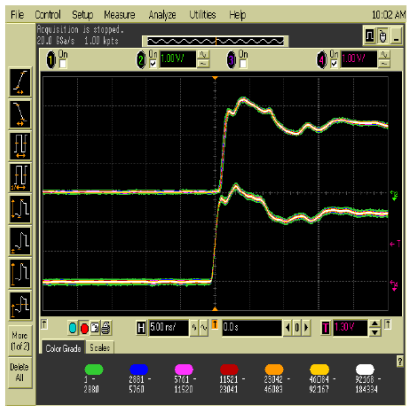


Each clock signal source may be independently located
(on each of the AMC cards, RTM or ATCA backplane)

Synchronization

Signals are decoded from ATCA backplane IRIG signal

- relative jitter below 1 ns
- delay between two cards ~2 ns



Statistics over 5 hours of the synchronized PPS signals from two ATCA-IO-Processor boards

ITER

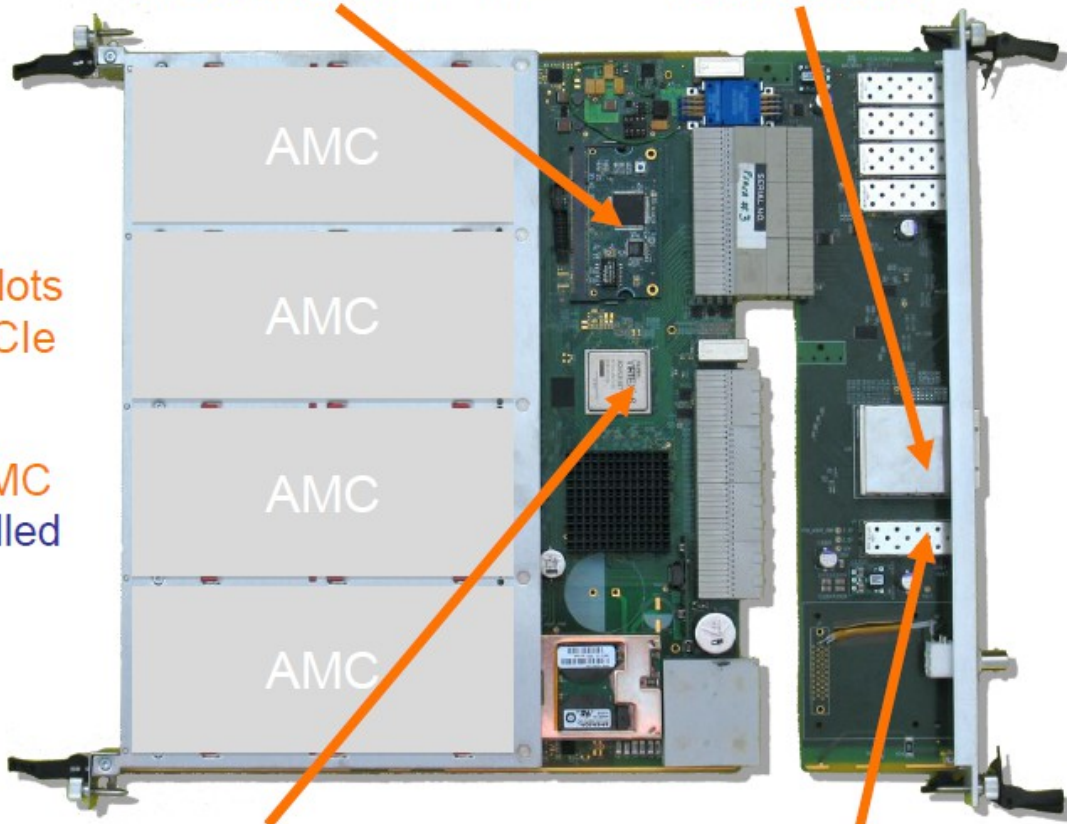
ATCA AMC Carrier / Hub

ATCA-PTSW-AMC4

PCIe on fabric
not available from industry

Support multiple processors on AMC slots or external through PCIe cable connection

Mid/full-size COTS AMC modules can be installed



Bell II readout à KEK

Belle II/PXD+SVD Project at KEK Japan

- Requirement of PXD readout
  - >240Gbps bandwidth
  - 400GB buffer
  - 1/10 reduction
- Solution
  - New CN
    - ACBA(ATCA Carrier Board for AMCs) boar
    - AMC cards
    - 6Gbps ports
    - 4G Buffer

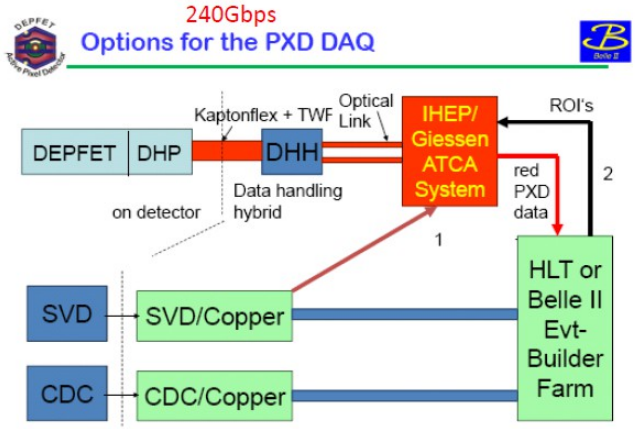
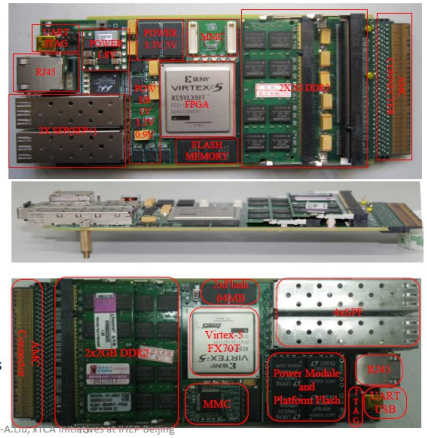


Photo of xFP with FPGA of 50T and 70t w/ PPC

Rightupper: 50T, 2 opt ports

70T with 4 opt ports

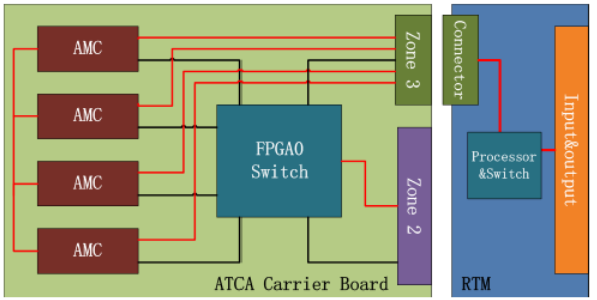


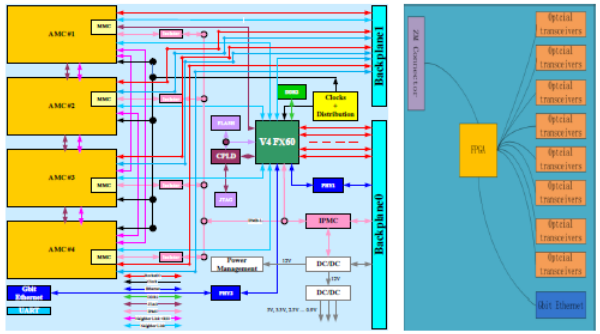
Rightlower: 70T, 2 opt ports

Jun.10 2012 Z.-A.Liu, xTCA initiatives at IHEP Beijing

Development of New CN

- The ACBA board
  - based on xTCA
  - allowing backplane data transmission
  - 4 AMC connectors
  - FPGA0 for switch
  - IPMC routing
  - Clock/trigger/ distributions
  - Power conversions
  - RTM reservation

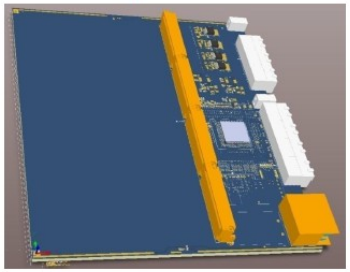




Jun.10 2012 Z.-A.Liu, xTCA initiatives at IHEP Beijing 9

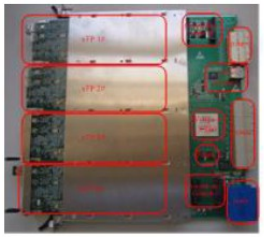
ACBA Carrier Board development

- Mother board
- Power board
- Protection box



ACAB PCB

Power board



ACAB with AMCs

ACAB with case

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MTCA.4

Pentair Technical Products

MTCA.4 shelves for Physics applications

Schroff

- **New MTCA.4 shelf with 7 AMC slots for laboratory and deployment use**

- **Front:**
  - 6 x AMC slots double-wide, mid-size
  - 1 x AMC slots double-wide, full-size
  - 1 x PM (Power Module) Slot
  - 1 x MCA slot
- **Rear:**
  - 6 x RTM slots double-wide, mid-size
  - 1 x RTM slots double-wide, mid-size
- **Hot Swappable CU (Cooling Unit)**
- **Removable Air filter**

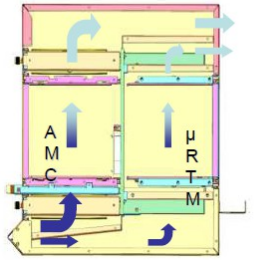
Pentair Technical Products

MTCA.4 shelves for Physics applications

Schroff

- **Updated Deployment chassis for 12 AMC slots**

- **Front Module Slots:**
  - 12 x AMC slots double-wide, mid-size
  - 4 x PM (Power Module) Slot
  - 2 x MCA slot
- **Rear Module Slots:**
  - 12 x RTM slots double-wide, mid-size
- **19" wide x 9U high**
- **Push-Pull cooling with front removable fan trays**
- **Front removable Air filter**
- **Air flow front bottom air intake, to rear air exhaust**



Pentair Technical Products

MTCA.4 shelves for Physics applications

Schroff

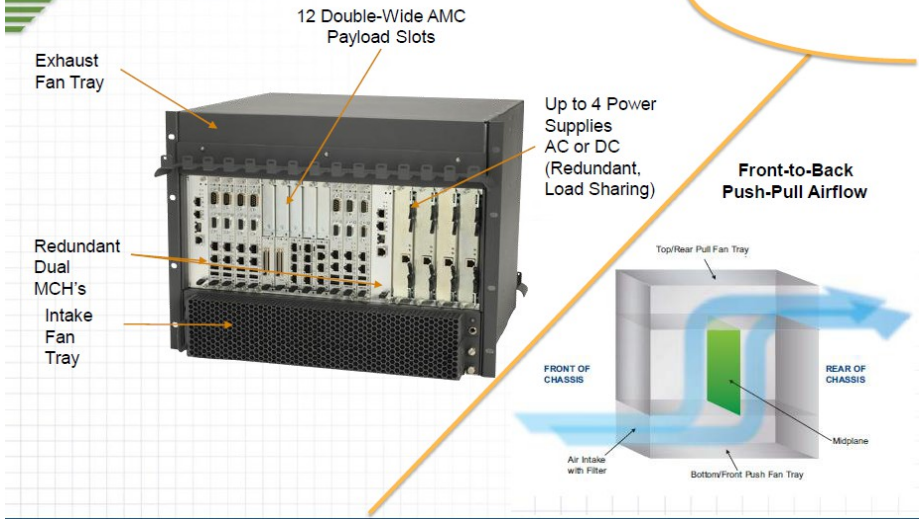
- **New 2U 6-Slot Shelf**

powerBridge Computer

- **Front Module Slots:**
  - 6 x AMC slots double-wide, mid-size
  - 1 x MCA slot
- **Rear Module Slots:**
  - 6 x RTM slots double-wide, mid-size
  - 1 x PM slot
- **19" wide x 2U high**
- **Front removable CU (Cooling Unit) including air filter**
- **Air flow front air intake, to left air exhaust**
- **Customized solution for powerBridge computer**

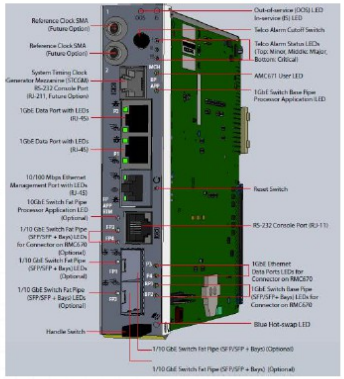
MTCA.4

Monterey 8000: Front



AMC671 MCH w/ Fat Pipe Options

- MicroTCA.0 and MicroTCA.4 compliant
  - MCH and MCH RTM
- Base Fabric: 1GbE to each AMC
  - Dual 1GbE Uplinks to Front/Rear
  - Dual 10GbE Uplinks to Rear
- Fat Pipes Option:
  - 10GbE Fabric
  - 40GbE Fabric
  - PCI-Express (Gen III)
- IPMI Platform Management
- 10/100MbE OOB Management Port
- Clock Distribution to each AMC
- Telco Alarm Relay
- Console Port Front/Rear:
  - Platform Manager
  - Switch Management Processor
  - Fat Pipes Switch Management Processor



AMC124: Quad Core x86 AMC

- Intel® i7 Xeon Processor: Quad-Core
  - 1.73GHz
  - 2.13GHz option
- Up to 48 GB DDR3 w/ECC
- Front Panel with Dual 1GbE, Console, Dual USB
- AMC Connectivity
  - 1GbE
  - Fat Pipes: 10GbE or PCI-E
  - SATA
- RPIO Connectivity
  - PCI-E (e.g. convert to 1GbE or 10GbE uplinks)
  - SATA
  - USB
- On-Board SATA Flash Storage
- OS Support:
  - NexusWare® CGL OS and Development Environment
  - Linux®
  - Windows® XP
  - Solaris™ 9/10

MTCA.4 RTM

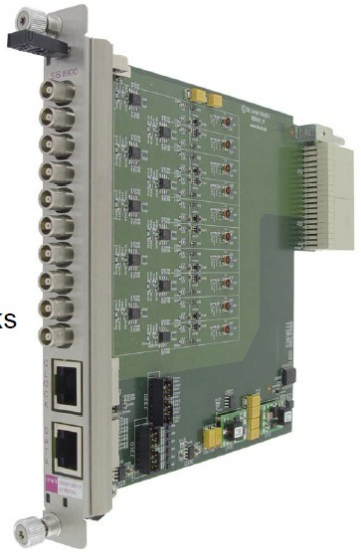
SIS8300 Digitizer Properties

- MTCA.4
- 4 lane PCI Express → 640 MB/s readout
- 10 channels 125 MS/s 16-bit ADC
- 10 MS/s to 125 MS/s per channel
- AC and DC input stage
- two 250 MS/s 16-bit DACs for fast feedback implementation
- high precision, flexible clock distribution logic
- Internal, front panel, RTM and backplane clock sources
- Programmable delay of twin ADC groups
- Gigabit Link Port implementation to backplane
- Double SFP cage for high speed system interconnects
- Virtex V FPGA
- up to 32 MSample Memory per channel
- additional point to point links over backplane
- In field firmware upgrade

struck innovative systeme

SIS8900 Single Ended Input RTM

- 10 LEMO 00 connectors (FMB option)
- 50 Ohm input impedance
- -1 V,...,+1 V default input range
- analog signals can be routed to AC and DC input stage
- RJ45 jack for RTM clocks
- RJ45 jack for Digital I/O
- +5V, 250 mA power option for RJ45 jacks
- two metric on board pin headers for 6 LVDS input/output signals each

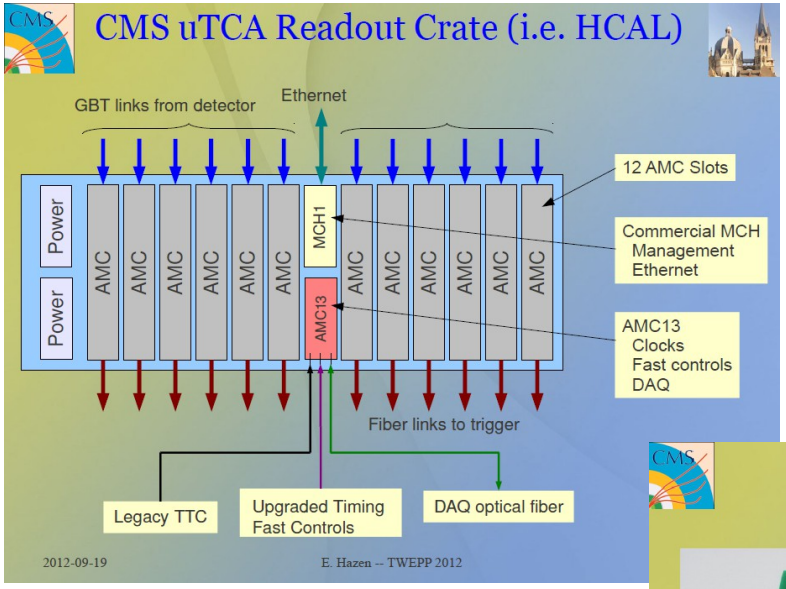


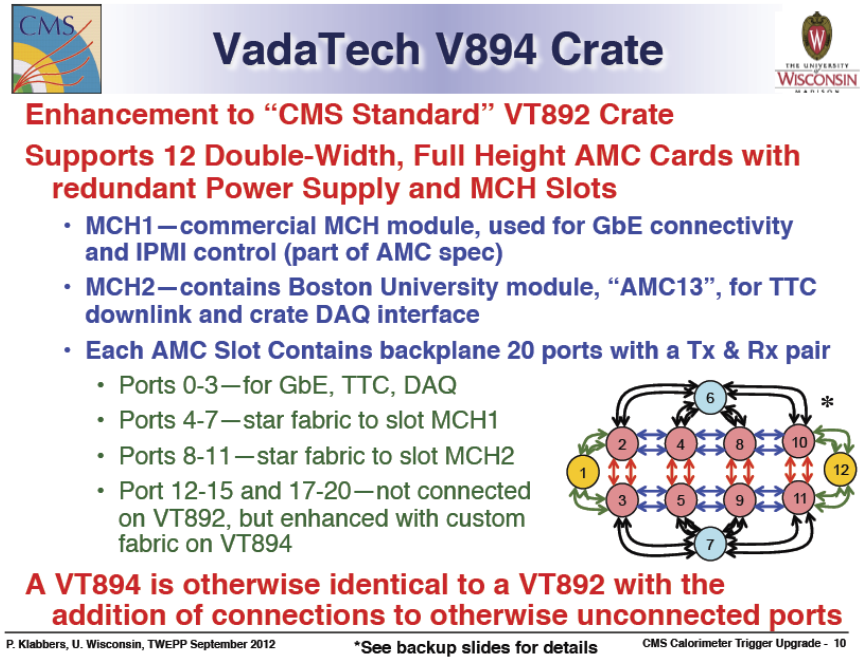
xTCA workshop TWEPP 2012

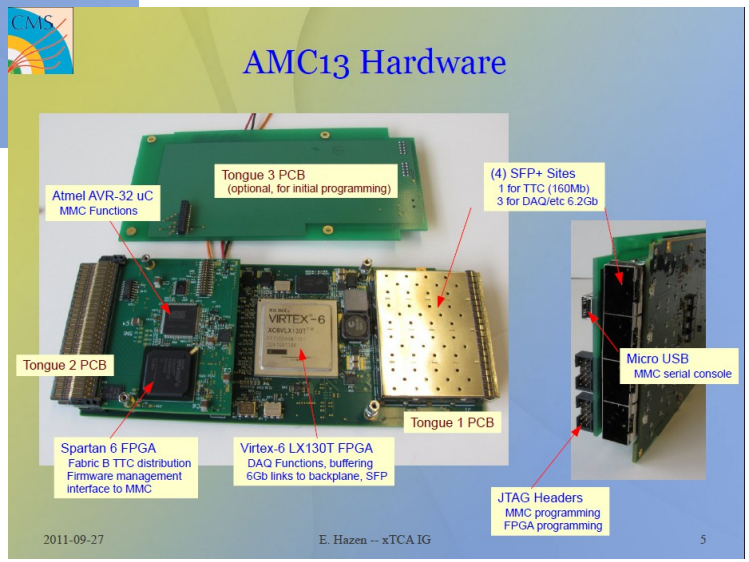
CMS

Architecture sur mesure

- VT894 Crate + custom backplane
- MCH + AMC13







CMS

MP7	Card	
Virtex 7VX690T	Processor	
690k	Logic Cell Count	
72	Input Optical Links	Number
10.3 Gbps		Speed
740 Gbps		Bandwidth
72	Output Optical Links	Number
10.3 Gbps		Speed
740 Gbps		Bandwidth
Ethernet, PCIe×4, TTC, DAQ, SATA/SAS 11× 1.8Gbps LVDS links in 11× 1.8Gbps LVDS links out	Backplane connectivity	
30× 1.8Gbps link Samtec header	Other electrical connectivity	
(Optional up to) 2× 144Mb 550MHz QDR II+ SRAM	RAM	
• 32GB µSD card for multiple firmware revisions and configuration data • USB serial console	Other features	

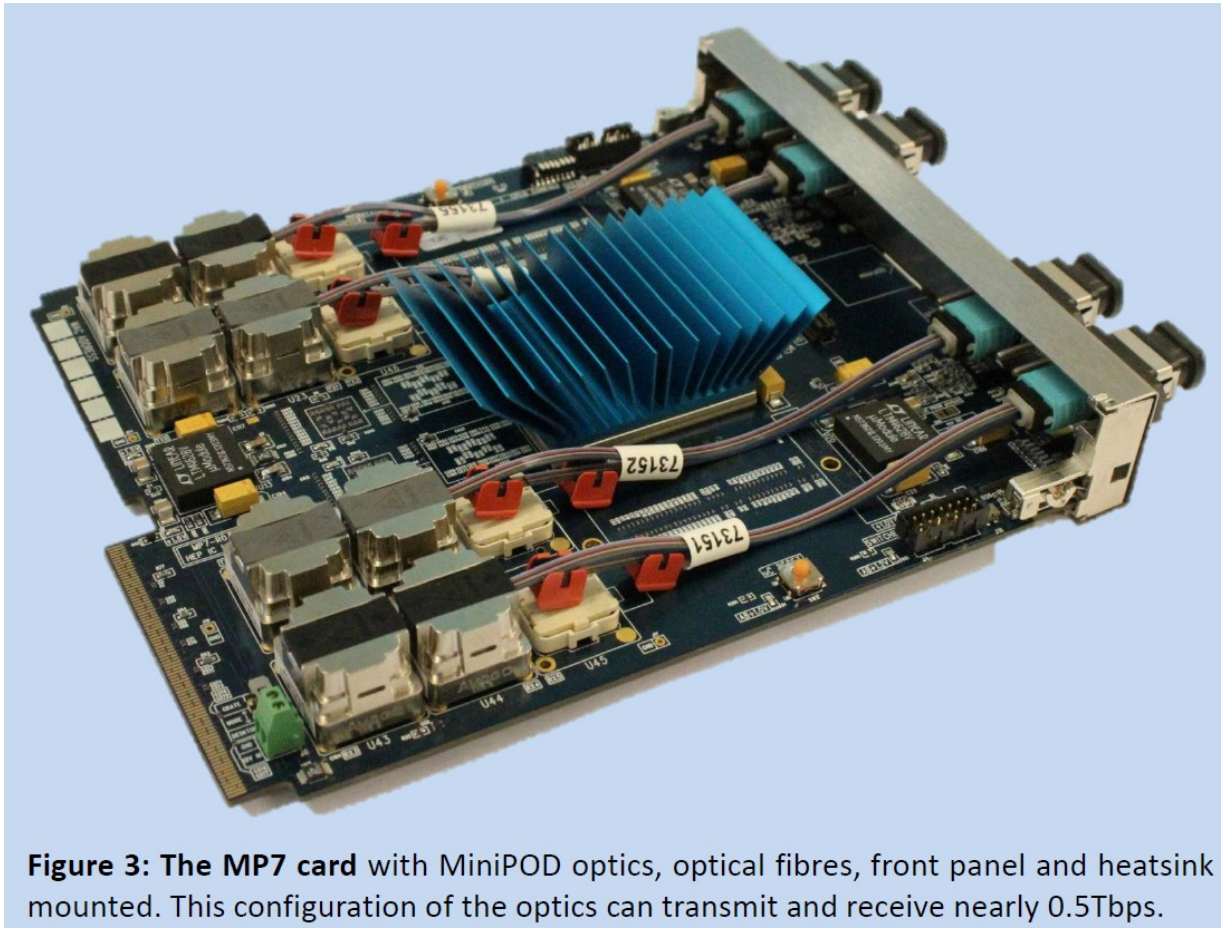
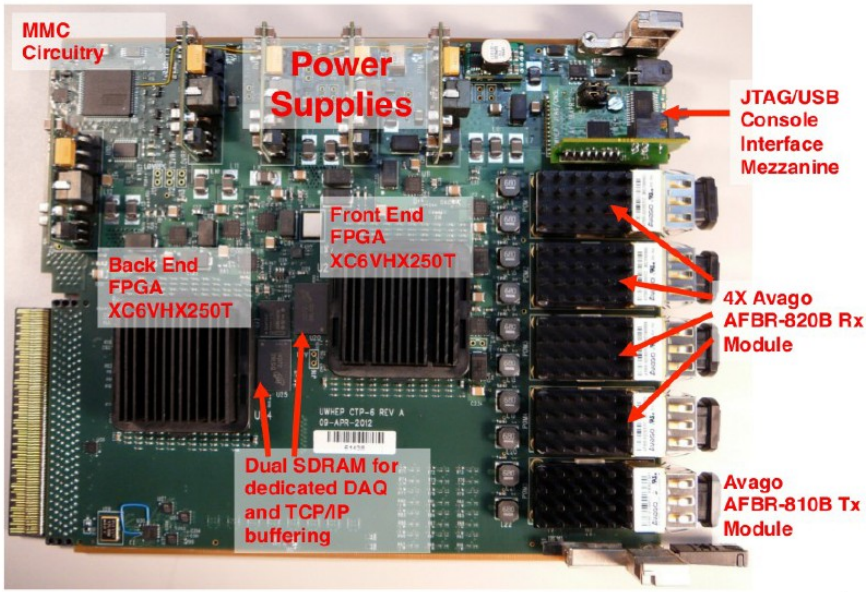


Figure 3: The MP7 card with MiniPOD optics, optical fibres, front panel and heatsink mounted. This configuration of the optics can transmit and receive nearly 0.5Tbps.

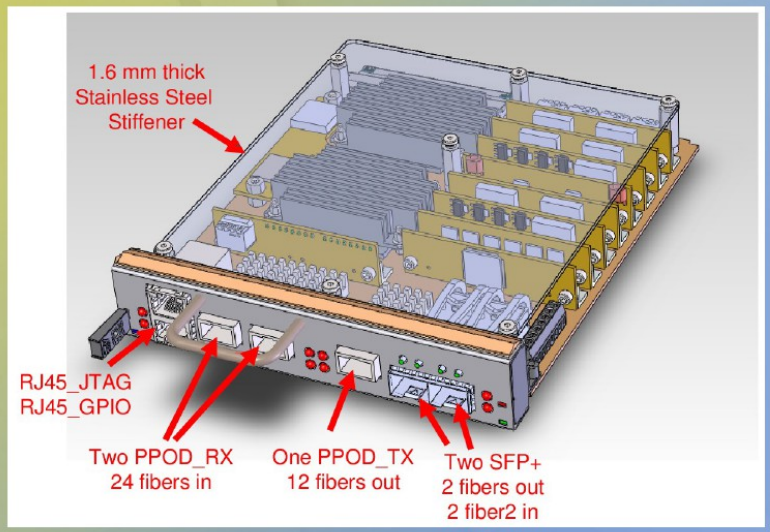
Imperial College Trigger Card

CMS

Wisconsin Calorimeter Trigger Processor (CTP) Virtex-6 Prototype Board



U. Minnesota – HCAL uHTR



2012-09-19 E. Hazen -- TWEPP 2012 8

ATLAS

Goals and status of the ATLAS VME Replacement Working Group

Markus Joos, CERN

Based on slides prepared by Guy Perrot, LAPP

19/09/2012

Approach

- **A 1 day meeting including the other LHC experiments has been organized in July**
  https://indico.cern.ch/conferenceDisplay.py?confId=196590
- **A questionnaire had been prepared and presentations were to give answers to it**
- **The analysis of this questionnaire showed that ATLAS sub-systems were all driving for ATCA**
  - There seems to be no need for uTCA
  - But there will be AMCs at the level of the ATCA blades
- **Possible common elements are being identified**
- **A list of points to solve is being defined**
- **Solutions and / or recommendations will be proposed**

Possible Common Elements (1)

- **System Manager (Software layer to manage shelves)**
  - Custom code (integrated into DCS) based on ipmitool / OpenIPMI?
- **ATCA shelf** (14 slots to fit in 19 inches Frames)
  - Backplane
    - Full mesh and radial IPM links
    - May use some fabric links for TTC distribution
  - Vertical airflow (to be compatible with existing infrastructure)
- **Shelf manager**
  - COTS component
  - Follow recommendation of shelf manufacturer
- **IPMC (mezzanine and S/W framework)**
  - LAPP IPMC design (already foreseen by LHC-b)
- **MMC (mezzanine and S/W framework)**
  - DESY/CPPM/CERN design whenever needed (AMC)
- **Power supply**

Possible Common Elements (2)

- **Blades**
  - Do we want to recommend commercial blades?
    - AMC Carrier blade
      - For what AMC format and fat pipe-protocol?
    - Switch blade
      - Most likely ATLAS ATCA blades will use Ethernet on both base and fabric interface
    - CPU blade (so far: Only one potential user in the ATLAS community)
  - Do we want to standardize some generic community built blades?
    - Carrier blade
    - Switch blade (e.g. including TTC distribution)
- **Tools for blade / system development and diagnostics**
  - E.g. IPMC tester S/W

Journée xTCA
École électronique IN2P3 2012

Thèmes abordés

Tutoriaux

- xTCA (Jean-Pierre Cachemiche)
  http://www.in2p3.fr/actions/formation/Numerique12/Technologies%20xTCA.pdf

- xTCA for Physics (Jorge Sousa – IPFN)
  http://www.in2p3.fr/actions/formation/Numerique12/Jorge_Sousa_xTCA%20Extensions%20for%20Physics.pdf

Retours d'expériences IPMI

- Implantation d'un système xTCA (Jean-Pierre Cachemiche)
  http://www.in2p3.fr/actions/formation/Numerique12/xTCA_retour_experience.pdf

- IPMI et retour d'expérience du LAPP (Nicolas Letendre)
  http://www.in2p3.fr/actions/formation/Numerique12/IPMI_et_retour_d_experience_du_LAPP_N_Letendre.pdf