ANR SPLAM: nouveaux ASUs

Réunion technique
LAPP
Jan. 16th, 2013

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Outline

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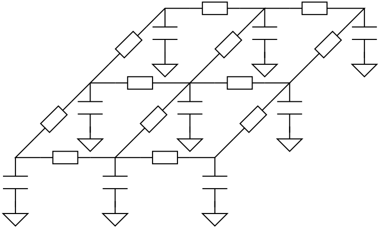
What is a resistive layer?

A resistive layer is a resistive coating which produce a distributed R-C network.



The resistivity is given in $\Omega/\square$: $R = \frac{\rho \cdot l}{h \cdot L}$ with $L = l \rightarrow R = f(h)$
Common values in PCB manufacturing : 100 $k\Omega/\square$ to 10 $M\Omega/\square$.
The capacitance is a function of the dielectric material and its thickness: $C = \varepsilon_0 \cdot \varepsilon_r \frac{A}{d}$

Orders of magnitude

Resistivity

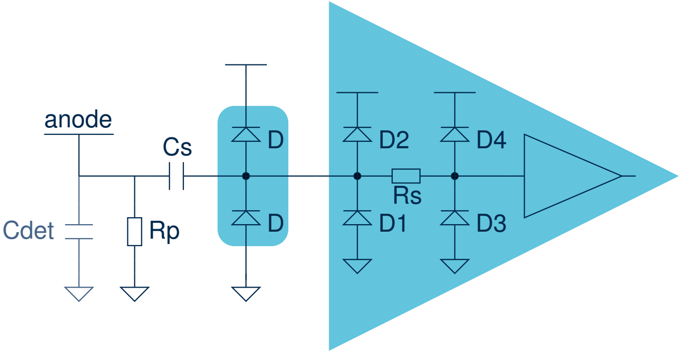
Layer thickness: 17 to 35 μm.
Common values in PCB manufacturing: 100 kΩ/□, 1 MΩ/□ and 10 MΩ/□.

Capacitance

Common values for 1 cm^2 anode :

Material	**Thickness**	**Capacitance**
Kapton	12.5 μm	240 pF
FR4	50 μm	80 pF
Photoresist	25 μm	100 pF
AriCH_4	128 μm	20 pF (measured)

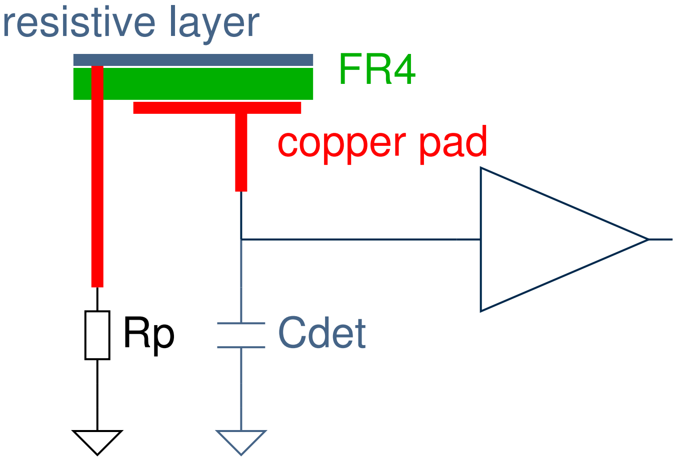
Reminder: current protection



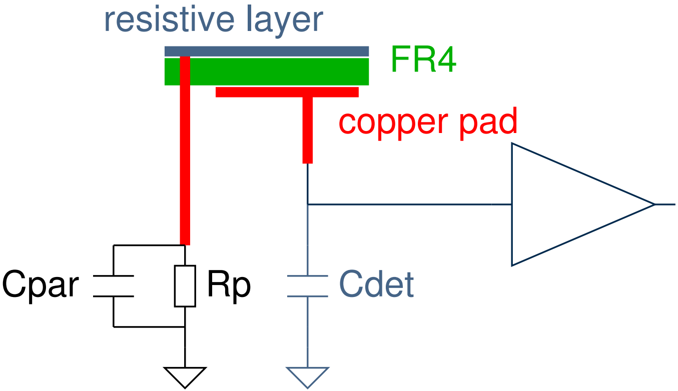
Rp=1 MΩ, Rs=10 Ω, Cs=470 pF, D are ON-Semiconductor NUP 4114, Dx are integrated fast diodes.

Proposition #1

Add a protective layer on the pad à la MAMMA. Implementation studied by Alex, Cyril, Renaud and Rui, presented the 10/01/2012.



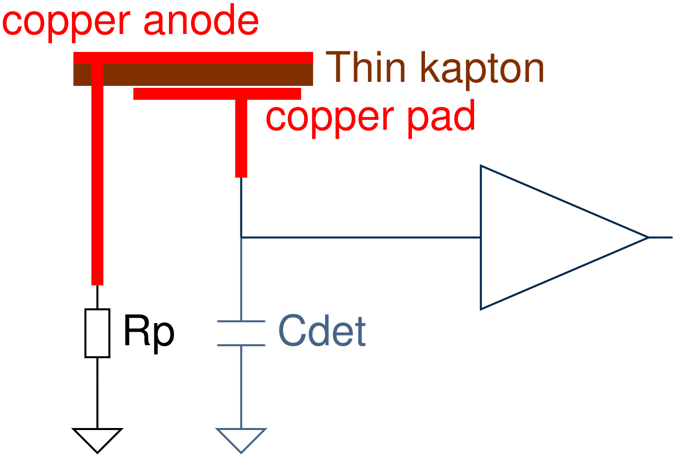
Proposition #1



The myth: the parasitic capacitor ! For a 100 µm ∅ via with 50 µm insulation (worst case !) C_{par}<0.5 pF. Mesh pillar over the via to ensure regular field (anyway, the via is grounded and not necessary over the R layer).

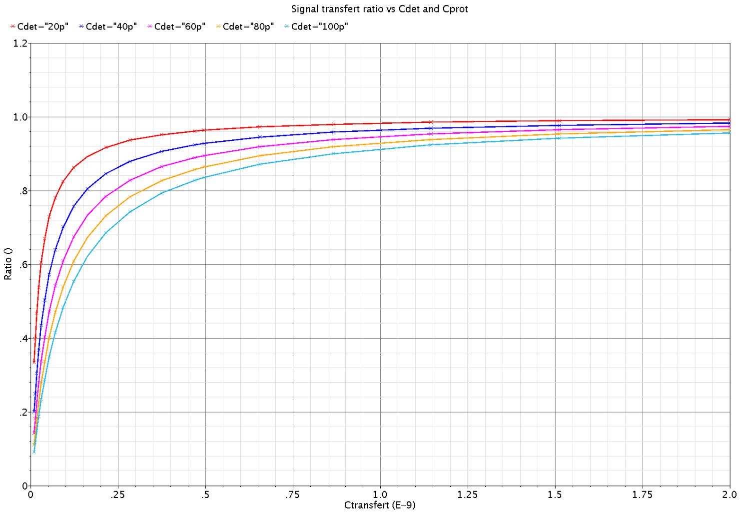
Proposition #2

Perform a pure capacitive readout. *cf.* R&D with BC16T.

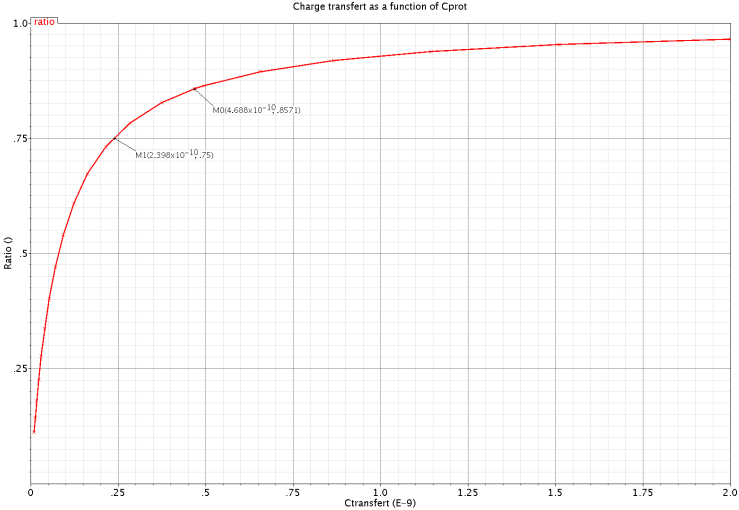


Unrealistic without ceramic-loaded films (loss of signal too important).
Expensive and film not easy to stock up (need license agreement...).

Charge vs Cs vs Cdet



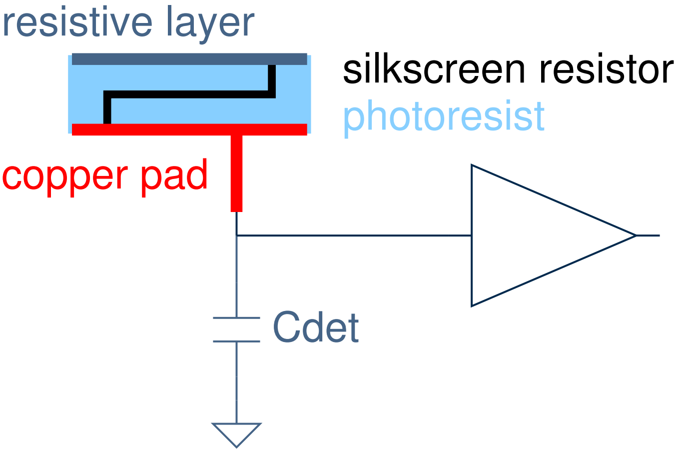
Charge vs Cs



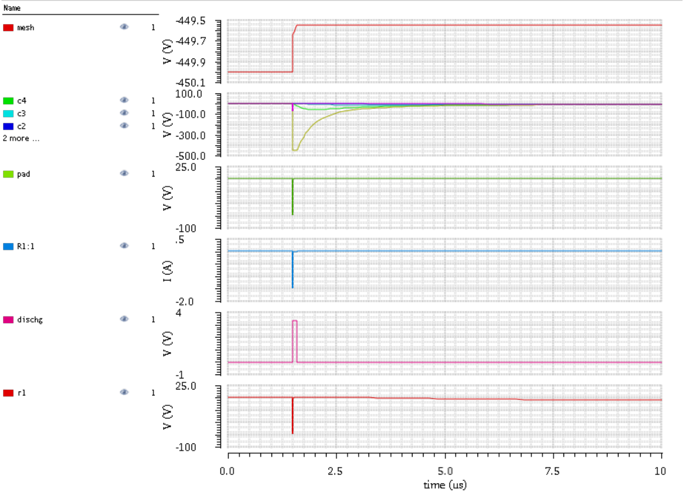
Charge transfert as a function of Cprot
ratio
M0(4.688x10^-10,.8571)
M1(2.398x10^-10,.75)
Ratio ()
Ctransfert (E-9)
1.0
.75
.5
.25
0
.25
.5
.75
1.0
1.25
1.5
1.75
2.0

Proposition 3

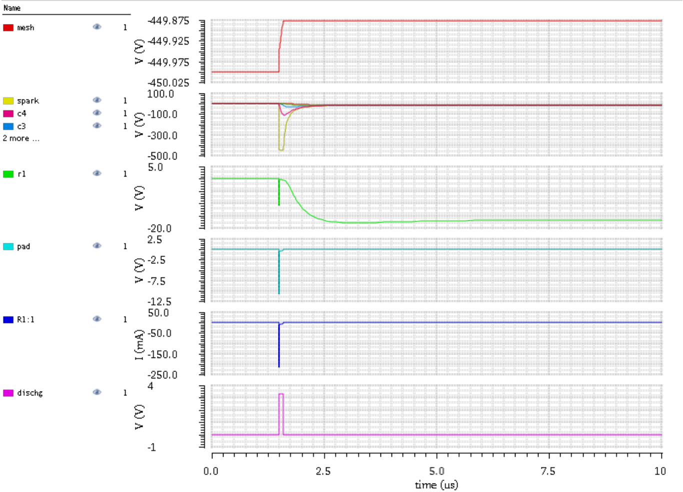
À la COMPASS: same as #1, but R layer is discharged via FE.



Simulation of #1



Simulation of #3



Pro and con

Simulation results very similar, but for both case, R and C must be tuned.

Solution Mamma		**Solution COMPASS**	
pro	con	pro	con
should work	sophisticated vias	easy	dead time
K at 0V possible			noisy?

Mamma (32x48) already designed by Alex (2217E + 1200E tool + postprocess: 2100 CHF/pièce + 600 CHF tool)
Possible to test via connection (different configuration) for 1700 CHF (all included)
Compass possible with existing ASU (postprocess: 4000 CHF for 2 boards)

Big vs small

Small

- Small prototype may help to test via connection for 1st solution, but there is another way, quickest and less expensive.
- Risk to be dominated by edge effect $\rightarrow$ if small proto are choosen, perhaps 16x16 is much better than 8x8.

Full size

- All ASU design already done $\rightarrow$ quickest and separate potential problems (same routing, etc)
- No new interdif (design time + pcb cost + new tools for cabling)
- No software nor firmware modification
- Result can be compared directly and immediately to square meter ASUs
- More than 300 MICROROC remaining.

Outline

Simulations

Well engaged, but we need to extract parameters from a prototype!. Then only we'll be able to ensure accuracy of simulations. Values are at the moment "orders of magnitude", mix of theory and rough measurement : we'll use resistive prototype to extract some values.

Protections tests

Jérôme has successfully tested a first batch of the new silicon protective structures (diode+MOS). The comparison with the reference protection has not been done yet, because the reference structure does not work yet... Investigation on the way!

Funds

Allocated by ANR (excluding Jérôme's contract): 51 500 €
Bonus from Arves Industries : 7 564 €
Total : 59 064 €
Remaining : 43 271 €

Outline

Conclusions

- According to me, both solutions (MAMMA and COMPASS) are appealing and both should be tested
- Do not forget that we want to build large detector *in fine*
- Jerôme's contract ends this year : big prototype are quicker to build, and the cost is not so much higher
- Big prototype will help us to refine modelling.