Upgrading the ATLAS Tile Calorimeter Electronics

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(for the ATLAS Tile Calorimeter System)

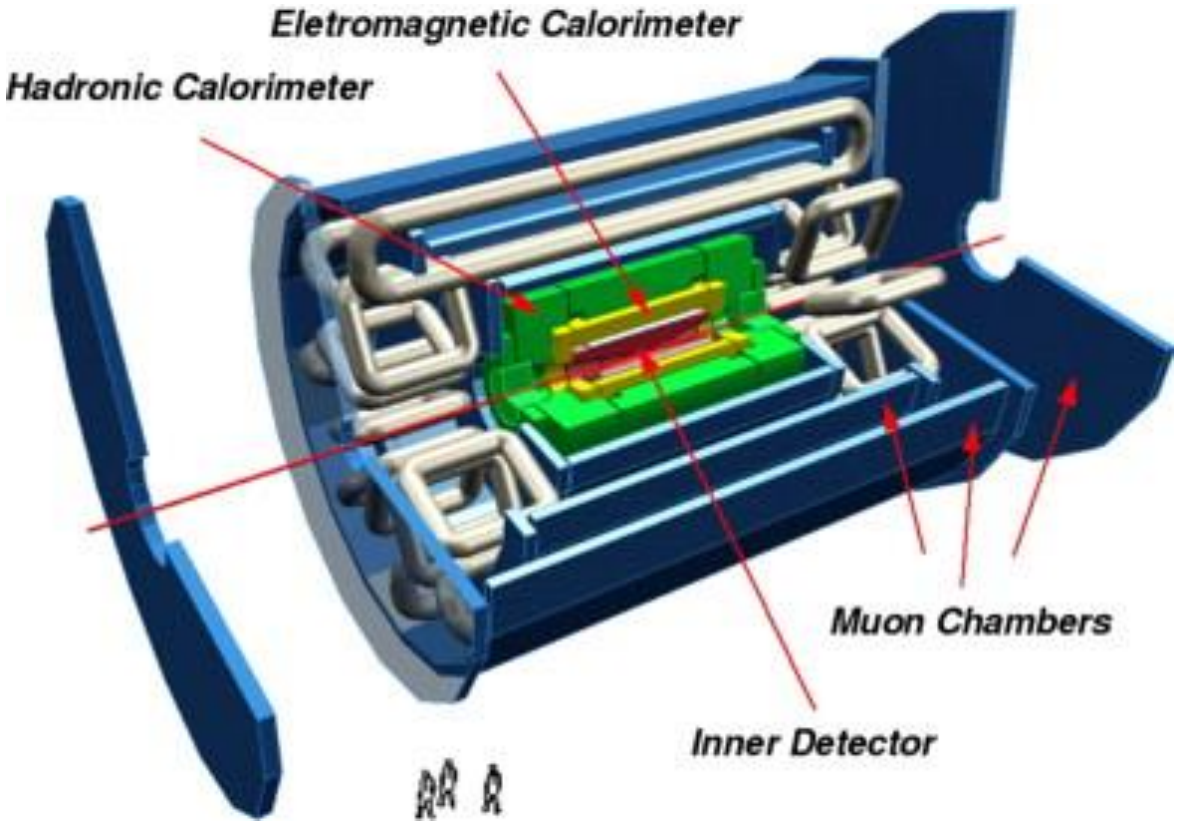
With special thanks to Christian Bohm and Alberto Valero Biot
For creating some excellent graphics

- Overview
- Front-end electronics
- Off-detector electronics
- Other R&D
- Schedule

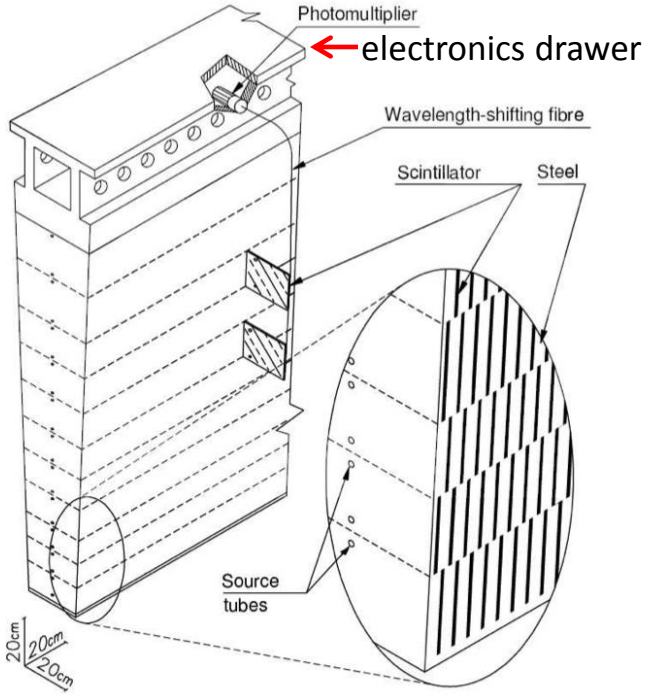
The LHC Upgrade Phases

- Completed Run-1: 2010-2013
  - $\sqrt{s}$ =7,8 TeV, luminosity L up to 8×10^{33} $cm^{-2}s^{-1}$
  - 50 ns bunch spacing … typically 30 interactions/crossing in 2012
- Phase-0 after Long Shutdown 1 (2013-14)$\rightarrow$ *nominal lumi*
  - increase $\sqrt{s}$ to 14 TeV (maybe 13.5), $L=1\times10^{34}$ $cm^{-2}s^{-1}$
  - bunch spacing 25 ns so that fewer interactions/crossing
- Phase-1 after LS2 (2018) $\rightarrow$ *ultimate lumi*
  - $L=2\times10^{34}$ $cm^{-2}s^{-1}$
- Phase-2 after LS3 (~2022) $\rightarrow$ *high lumi*
  - $L_{max}=(5\text{-}7)\times10^{34}$ $cm^{-2}s^{-1}$
  - experiments won't be able to handle that $\Rightarrow$luminosity levelling
    - Goal: no more than 200 interactions per crossing

The ATLAS Detector

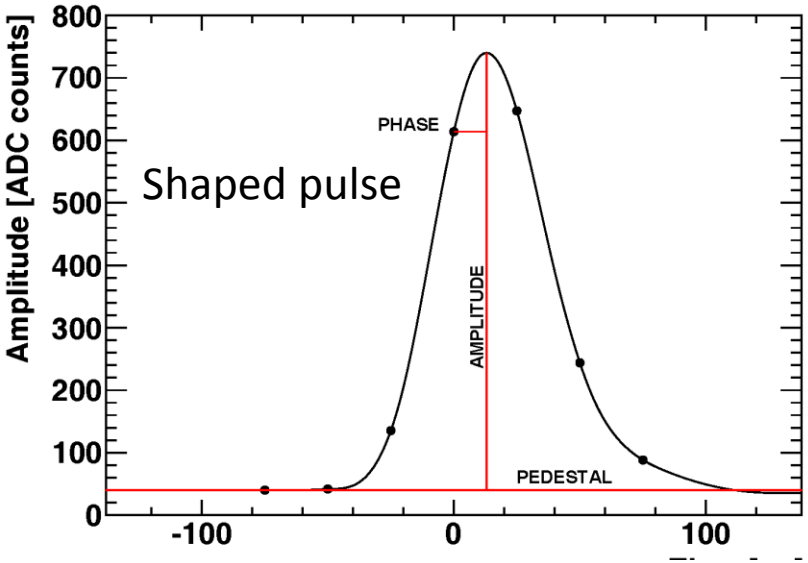


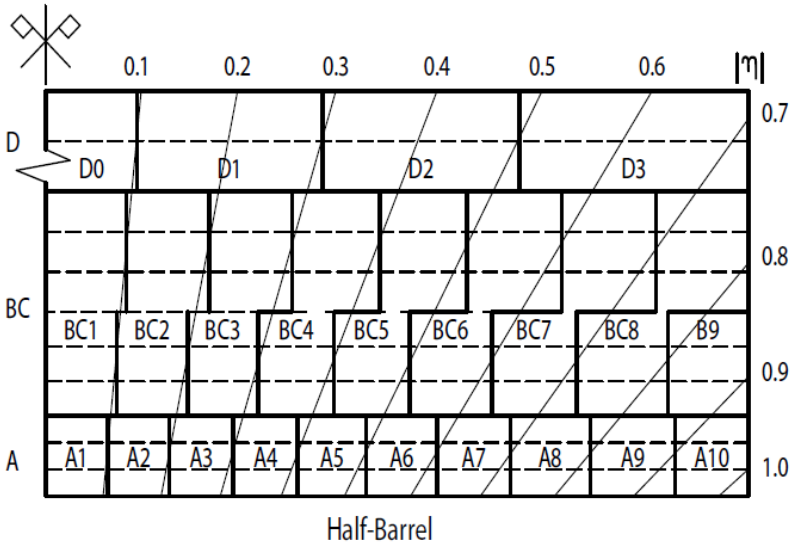
One Tile Wedge:



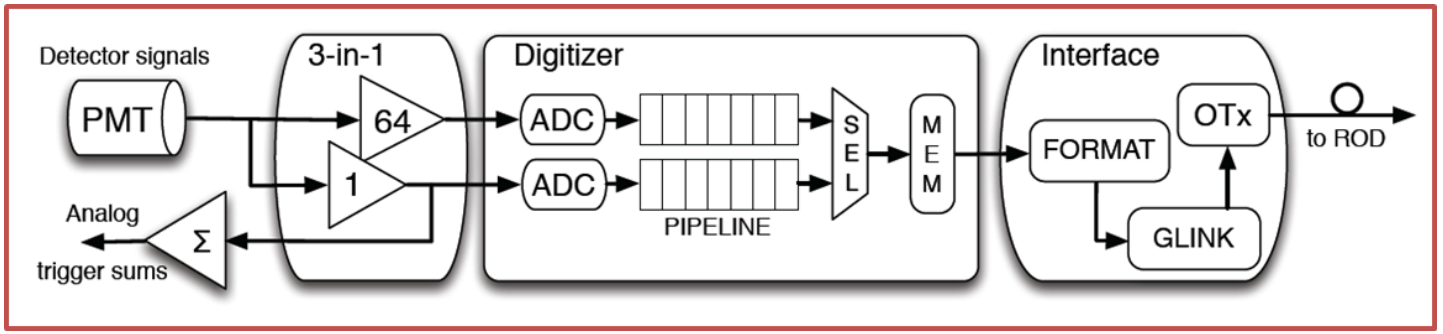
The Tile Calorimeter

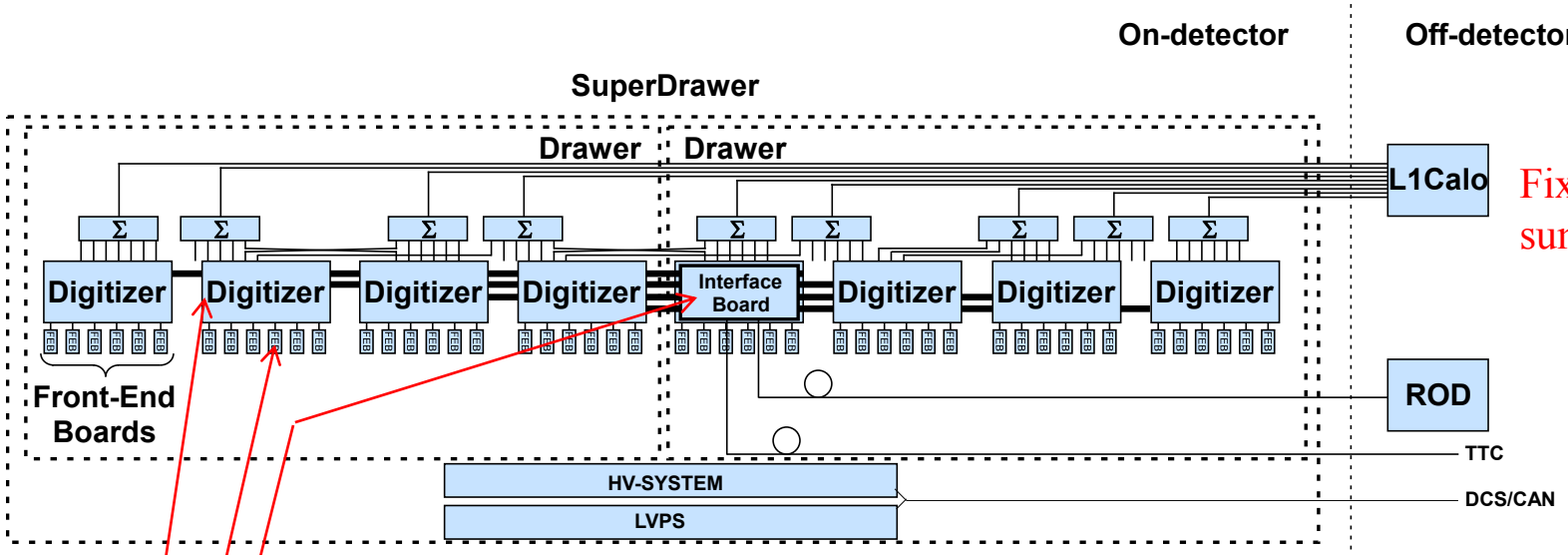
- Tile calorimeter
  - Digitize three radial layers (λ_{int} =1.5, 4.1 & 1.8)
  - e/h = 1.3 - 1.6
  - η covered by approximately constant Δη to 1.7
  - Δη X Δφ=0.1 X 0.1 (0.2 X 0.1 in outermost layer).
  - $22X_0$ -$33X_0$ in the barrel
  - Excellent hadronic energy resolution overall: 60%/√E
- Tower structure
  - 64 wedges in azimuth
  - 4 types of cell define towers in rapidity
  - analog trigger sum formed on-detector
- Data pipeline:
  - digitized data for all channels kept in rotary buffer
  - 16 bits achieved by two gain ranges
  - 7 samples of all channels sent off-detector to ReadOutDriver if there is a L1 trigger
  - ROD does the digital signal processing:
    - fits 25ns samples to template to get energy
    - zero suppresses





The Present System





Fixed analog sum to trigger

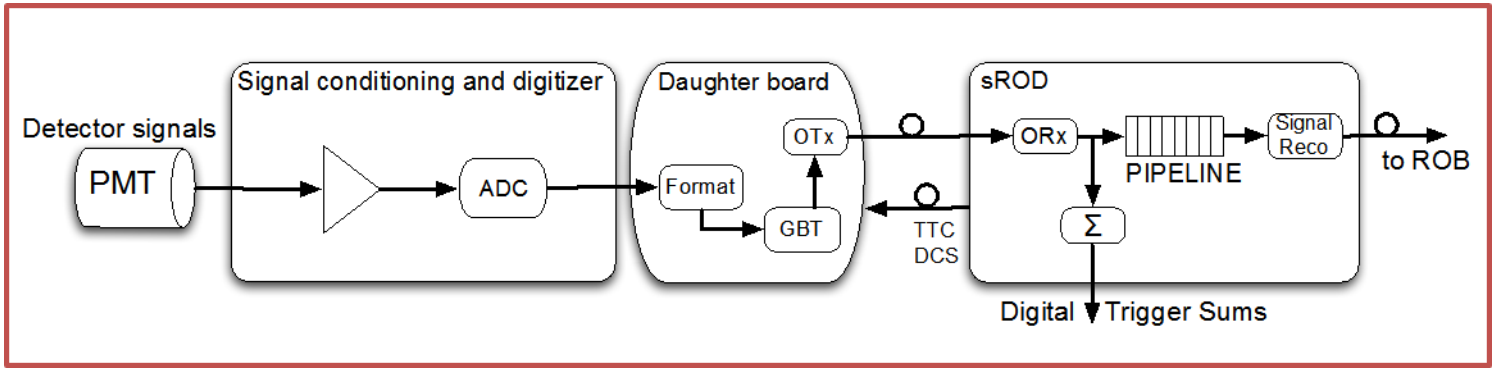
- Mother Board: LV, controls, base for PCBs with specialized functions:
- FEB: shape and amplify PMT signals, analog trigger
- Digitizer: ADCs, data pipeline
- Interface Board: off-detector data transmission and TTC receiver

The Issues Driving an Upgrade

- Important to address HL-LHC rate, radiation, error correction, and trigger
  - Better radiation tolerance
  - No analog trigger; all signals sent to USA15 via fast fiber
  - Local Point Of Load LV regulators with redundancy
  - Minimize number of connectors
  - No availability of parts for current system
- Architecture of upgraded system emphasizes reliability:
  - **Main Board** has LV/controls section and high-bandwidth mezzanine
  - Serialization plus GBT in the ~ 10 GHz mezzanine **Daughter Board**
  - Parallel Optics Device (POD) fiberoptics for now; studying modulators too
- Additional redundancy by **independent readout of the 2 PMTs** attached to each calorimeter cell. Duplicating the fibers to further improve redundancy and in general avoid single point failures.
- Redundancy in power supplies – 10v power distribution with local POL regulators
- Also looking at possibility of improved mechanics (smaller drawers ~75cm, <25kg) to allow access with shorter ATLAS opening and easy access/manipulations
- Replacing all LV on-detector electronics – all HV on-detector electronics – LVPS

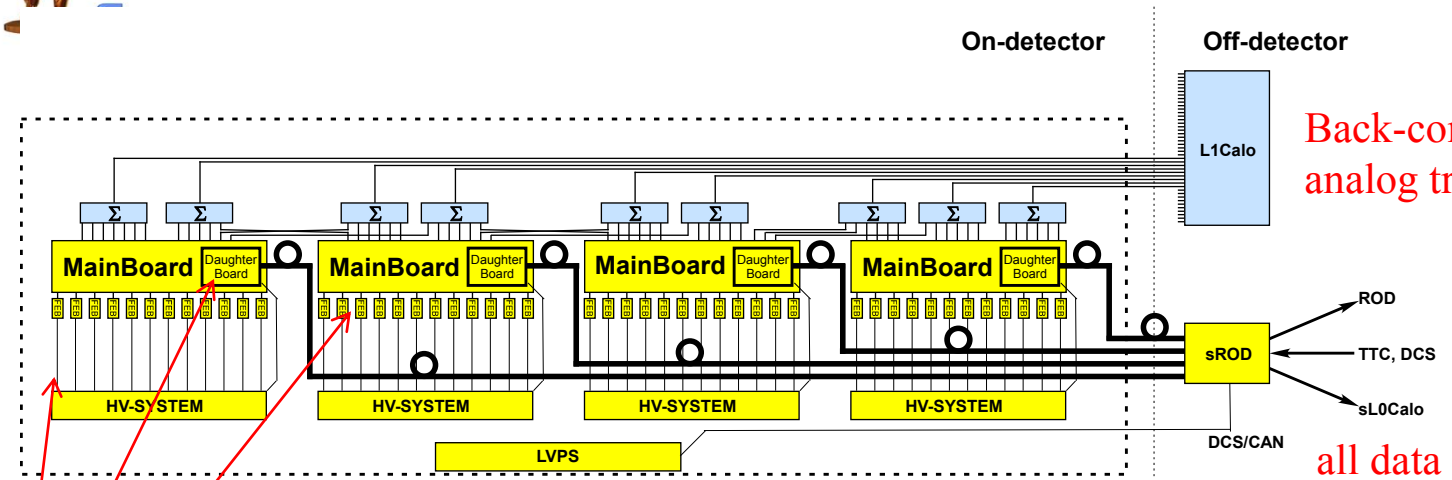
The Phase-2 Tile Upgrade in Brief

- For LHC Phase-2 a major change: send all data to L1CALO
  - high speed optical communications permit a lower noise, reconfigurable trigger
  - lower noise, radiation hard components
  - chance to simplify and address old problems: fewer voltages and connectors
- We need complete redesign of on&off-detector electronics
  - Front-End Card: considering redesign of current shaper or ASIC options
  - Main Board: does signal routing, digitization, controls
  - Daughter Board does the high-bandwidth tasks: serialization, optical communications



- Such extensive redesign needs testing
  - Demonstrator: insert 1 new drawer in 2014

The Demonstrator Features



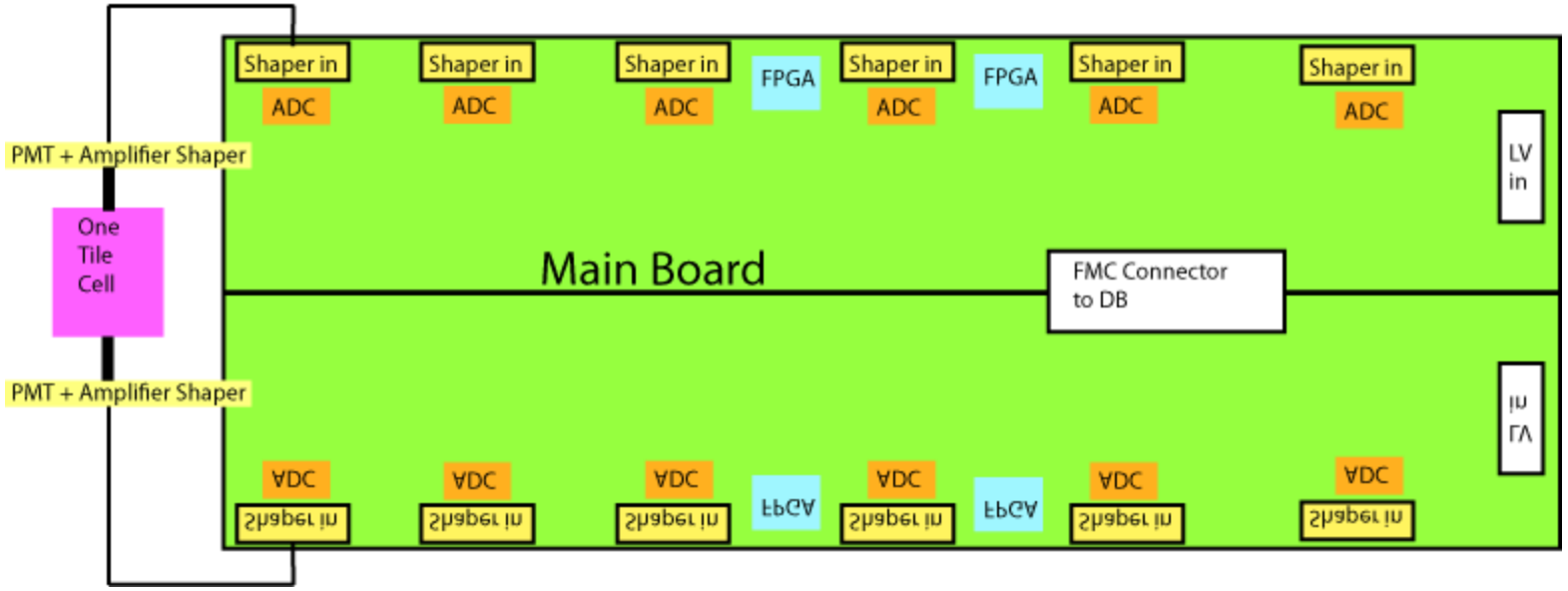
Back-compatible analog trigger sum

all data sent to new sROD; forms trigger for studies

- high speed DB: serializes, error encodes, sends/transmits optical signals
- MB has ADCs, LV distribution, controls
  - has analog sum cards compatible with current system
- new Front End Boards shape/amplify PMT signals
  - also charge injection and Cs integrator calibrations
  - *Alternative* FEBs under development: FE-ASIC ,QIE
    - possibly lower noise, incorporates ADC, lower-cost
    - not ready for 2014 and can't provide analog trigger

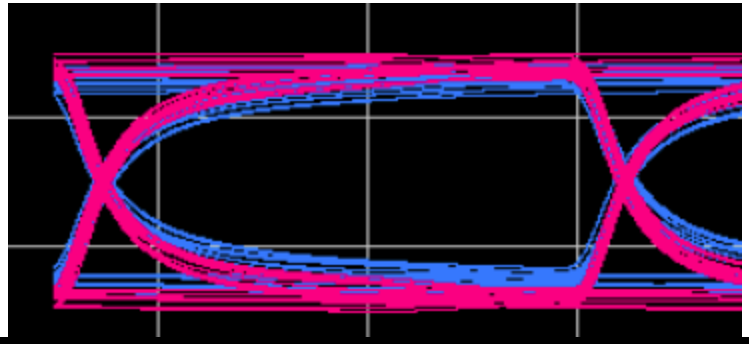
The Main Board

- This PCB is the backbone of the drawer architecture
  - receives amplifier/shaper signals
  - distributes LV
  - manages controls and calibrations
- Each MB receives 12 PMT signals
  - redundant architecture: each side of PCB has half of the fibers from each tile cell
  - separate LV supply on each side of MB preserves data in case of LV malfunction
- Fast data pipeline on highspeed DaughterBoard connected by 400 pin FMC



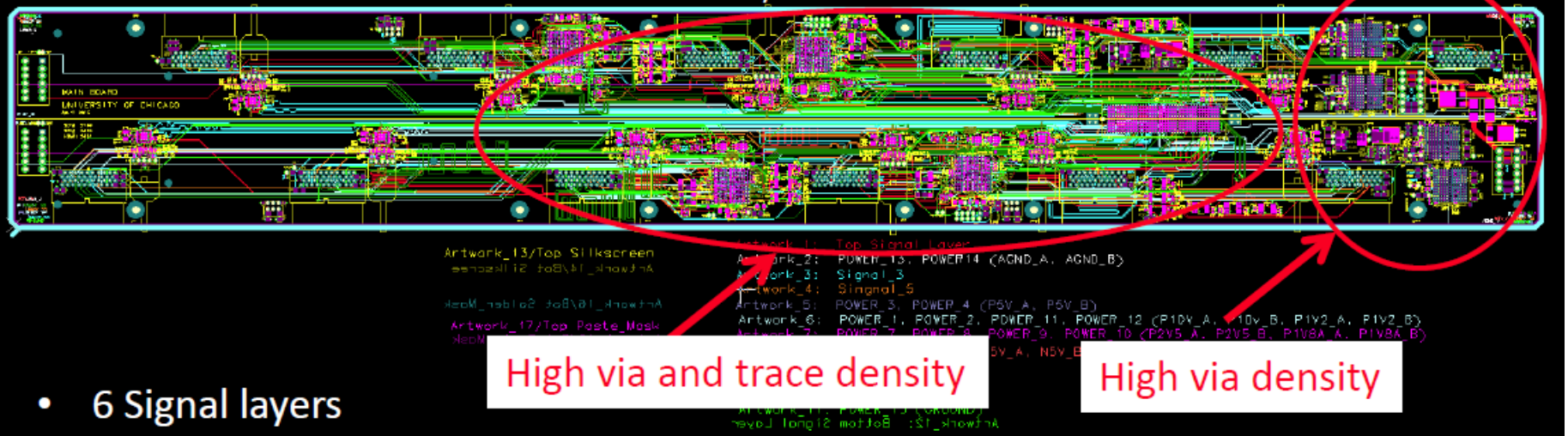
Main Board: Geometry Challenge

- 50 cm in length presents challenges: crosstalk, delay line timing, ball-grid stability
- 14 layer board with 3 ground planes
- simulations give good performance



Complexity and Challenges:

- High speed: (640 Mbps)
- Max. trace length: (20 inches)
- All routes are same direction routes
- Crosstalk consideration: (parallel and tandem)
- Mixed signals (low noise analog and high speed digital)
- Equal timing high speed traces
- Current rate constraints
- Swish-cheesed power planes (via usage limitation)
- Many other constraints



- 6 Signal layers
- 8 Power layers including 3 redundant ground layers (continuous solid plane) for signal integrity and tandem crosstalk reduction

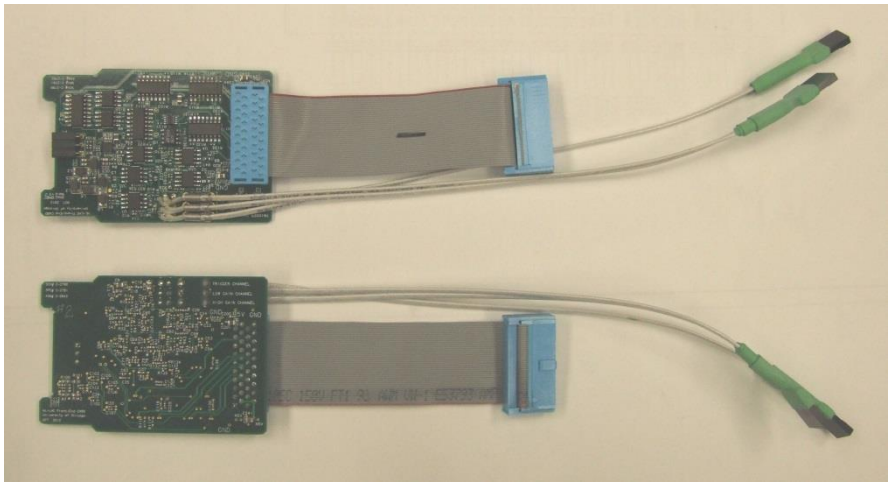
The 3 FEB Alternatives

- 3 different possibilities for shaping, digitization and radiation tolerance
  - Discrete component version is remake of a well-proven design; 12-bit ADC requires only 2 ranges to be calibrated
  - the two ASICS benefit from probable radiation tolerance of small-feature size and fewer components
    - Trade-off: lower voltage requires 3 or 4 ranges; unipolar
    - Need to decide on active shaping or direct integration of PMT

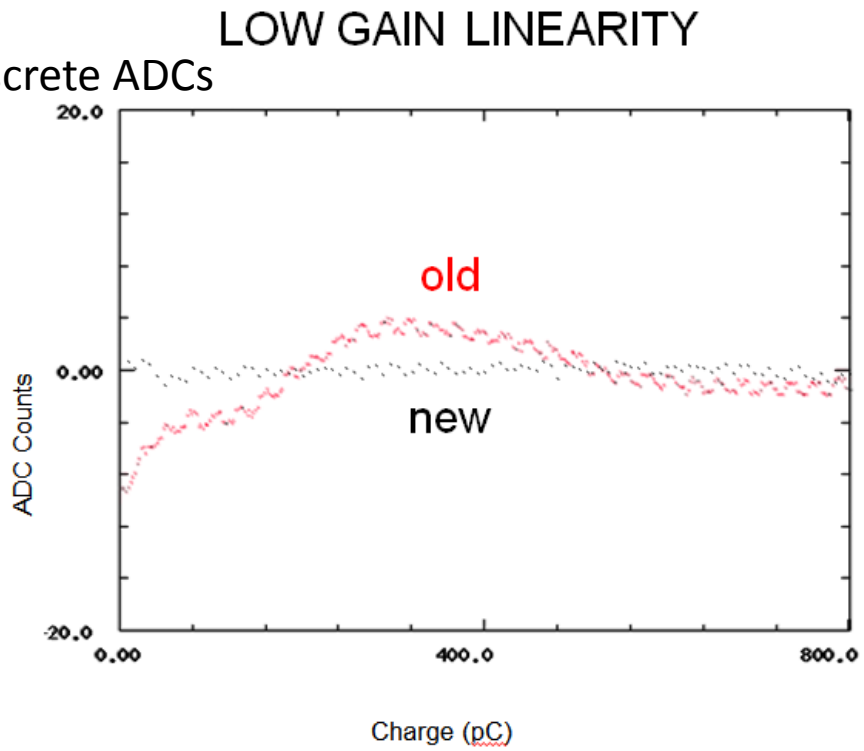
- We are designing 3 Main Board variants to receive the 3 FEB signals
  - High-bandwidth daughterboard is the same for all 3 variants

- Summary of the developments:
  - Discrete component version has been built, gives good performance, and has been found to meet radiation tolerance only for ionizing radiation
  - New version of QIE being designed jointly by ATLAS and CMS
    - Received version-2 from foundry …now testing
  - FATALIC ASIC is a 3-stage current conveyor variant on a chip designed for LHCb; have tested version 1,2 protypes, now on version 3

Amplifier Option 1: New 3-in-1 card

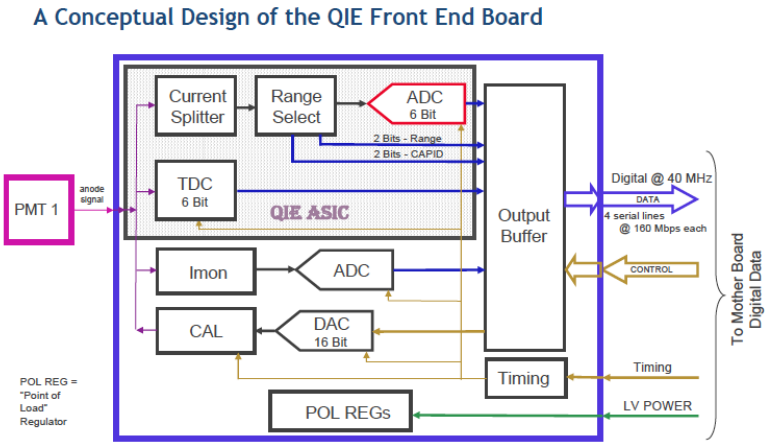


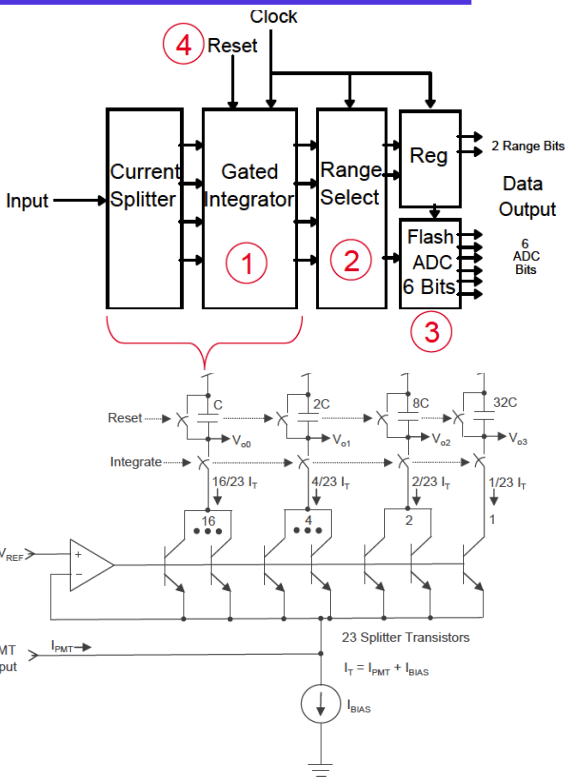
- Improved version of the present design
  - COT discrete components
  - Improved functionality - Better linearity
- 3 main functions:
  - High and low gain analog outputs
  - Charge injection calibration
  - Integrator to read out Cs calibration data
- Digitization in MainBoard with independent discrete ADCs
- STATUS:
  - Prototypes built and tested
  - Radiation tolerance successfully tested

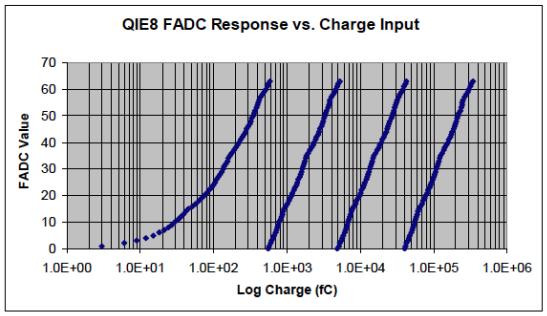


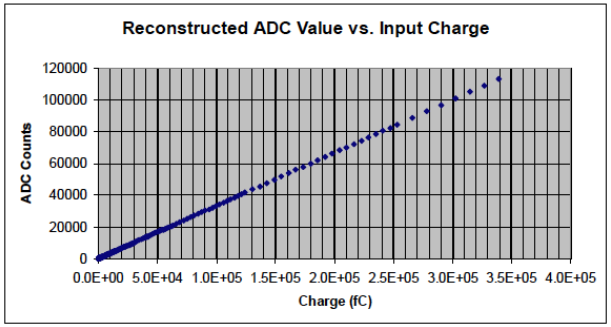
Amplifier Option 2: QIE

- charge integrator
  - 4 clock cycles to acquire the data
- Data Output : 10 bits encodes a 17-bit dynamic range
  - 6-bit ADC value, 2 bits range (4 ranges), 2 bits CAPID
- Version 10.5 received this month, under evaluation
  - fully-functional, including data drivers and TDC
- PLANS:
  - First tests with QIE at CERN lab in late summer, 2013
  - Beam tests at CERN in 2015; Maybe at FNAL in 2014







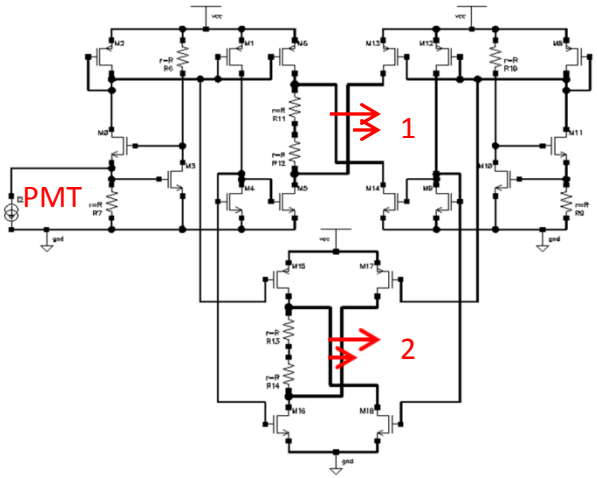


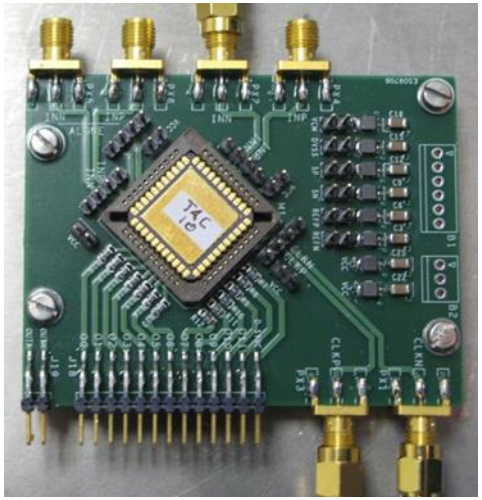
Amplifier Option 3: FATALIC CHIP

FATALIC: Front-end for Atlas Tile cAL Integrated Circuit
TACTIC: Twelve bits AdC for s-atlas Tilecal Integrated Circuit

- Based on the **FATALIC** chip family + TACTIC ADC
  - Current conveyor concept
- IBM 130 nm technology. Shaping, 3 gain ranges (1, 8, 64)
- First prototypes (FATALIC 1/2) tested
- Version FATALIC 3 being tested.
- Validation of the current conveyor concept.
- Promising "digital integrator" for the Cesium calibration
- **TACTIC**: Include 12-bit pipeline ADC@40 MHz
  - Best resolution and speed.
- **STATUS:**
  - First tests of FATALIC already done in the lab at CERN
  - Production of TACTIC chip is ongoing. First units delivered early December
  - Next step: before putting inside FATALIC→ "3in1" card with TACTIC next to FATALIC.

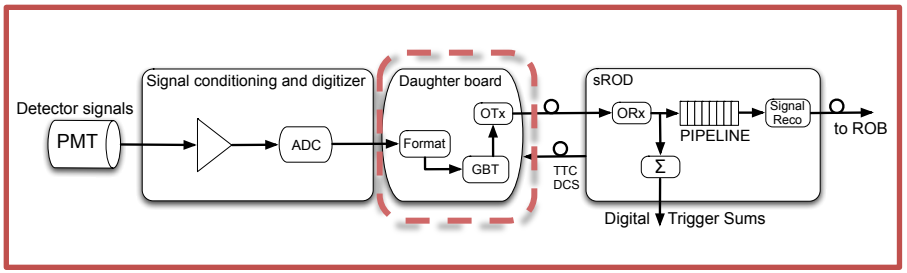
2-stage current conveyor





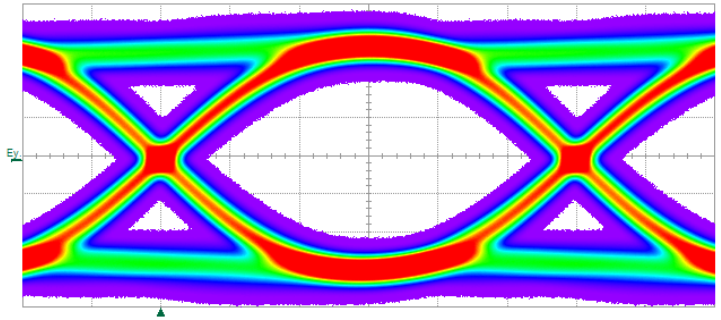
First TACTIC chips from January 2013

Daughter board: High Bandwidth

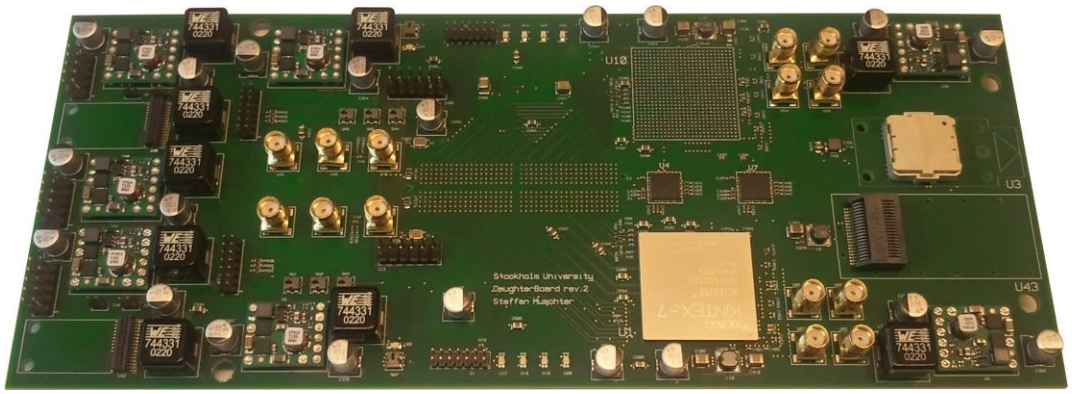


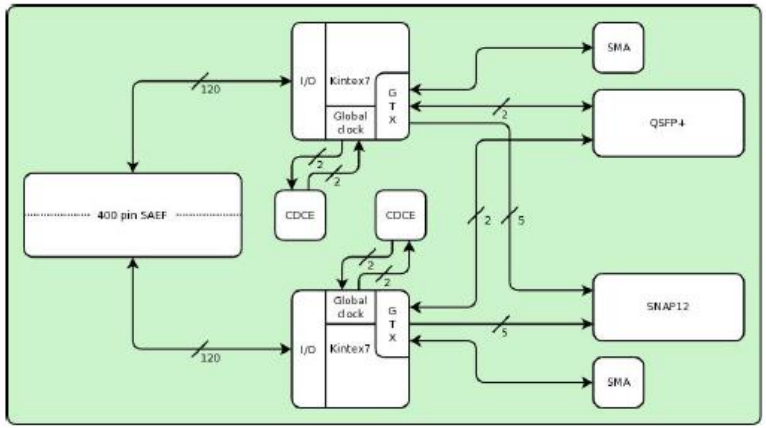
High speed system on mezzanine PCB preserving 2-fold redundancy

- Kintex 7 FPGAs
- 400 pin FMC connector to Main Board
- Evaluation of different optical links.
- Clock recovery unit + additional clock inputs



- STATUS.
  - Second prototype being evaluated.
    - GTX transmission at 5 Gbps and 10 Gbps
    - BER better than 10^{-13} at 10 Gbps
  - 2nd quarter 2013: submission of an almost final demonstrator version





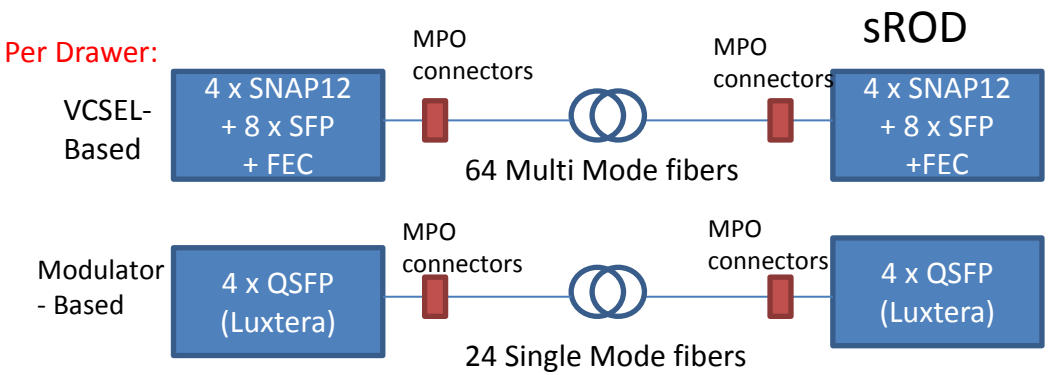
Optical links: vcsel *vs* modulators

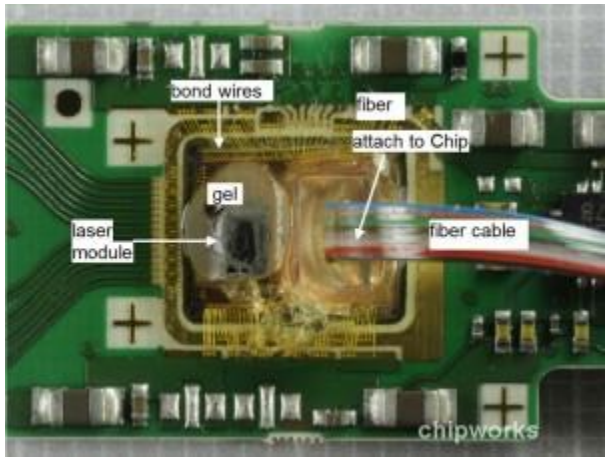
- New studies of QSFP+ transceivers based on modulators (Mach-Zehnder interferometers)
  Can operate above 40 Gb/s (4x10) with bit error rates (BER) less than 10^{-18}
  - Radiation hard proved. No SEU observed : TID of 64 krad, fluence of 8 x 10^{11} p/cm^2
- Directly modulated lasers (including VCSELs)
  - Have been qualified at ~10 Gb/s per link but with BER ~10^{-12}
  - Increasing bandwidth increases problems
  - Use Multi Mode fibers
  - Commercial VCSEL arrays (SNAP12) have shown Single Event Effects (SEE) at ~10^{10} p/cm^2.
  - Luxtera chips are made with 130 nm SOI CMOS which *should* be very radiation hard
- Both approaches being evaluated in the demonstrator system.
  - Less fibers vs lower clock frequency.
- Radiation tests underway

Per link @ 10 Gb/s

10^{-18} BER =1 error in ~1000 days !

10^{-12} BER = ~ 900 errors per day

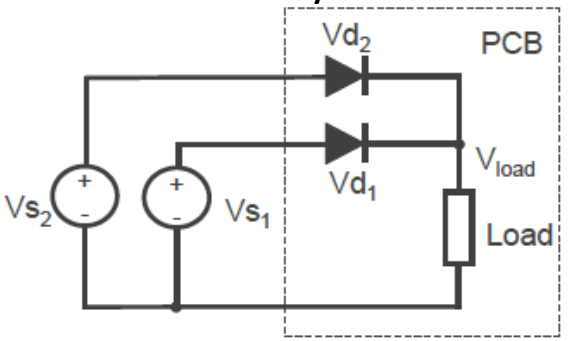


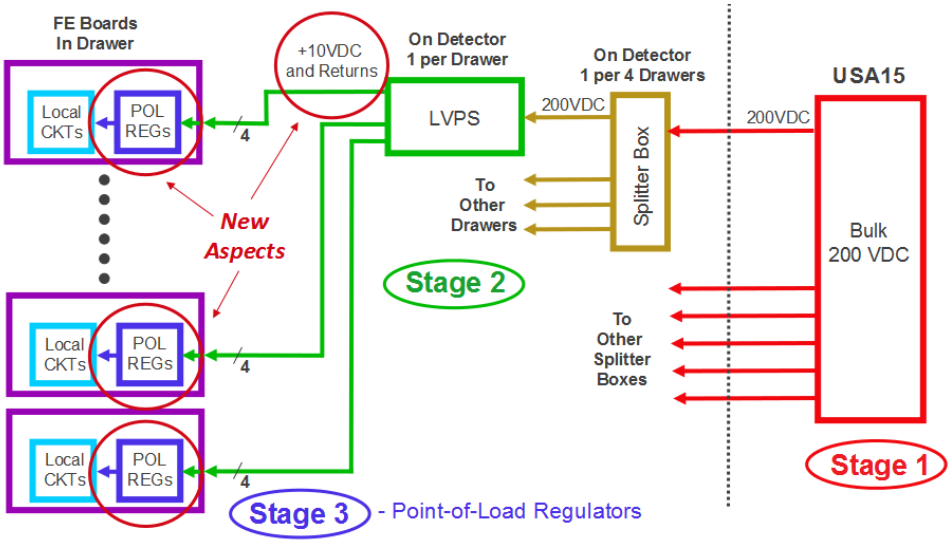


Front-end- LVPS

- **3 stage power distribution system design:**
  - **Stage 1 – bulk 200V in USA15 (off-detector)**
  - **Stage 2 – LVPS boxes on-dectector.** New design
    - +10V only
    - Tight regulation not important. POL does the final regulation
    - Advocating balanced loads
  - **Stage 3 – Point-of-Load regulators on MB, DB cards**
    - Several developments in progress for positive voltage regulator
    - Maybe CERN POL regulator will work even for negative voltages → provide just +10V from LVPS box and generate +/- voltages in the POL.

Redundancy





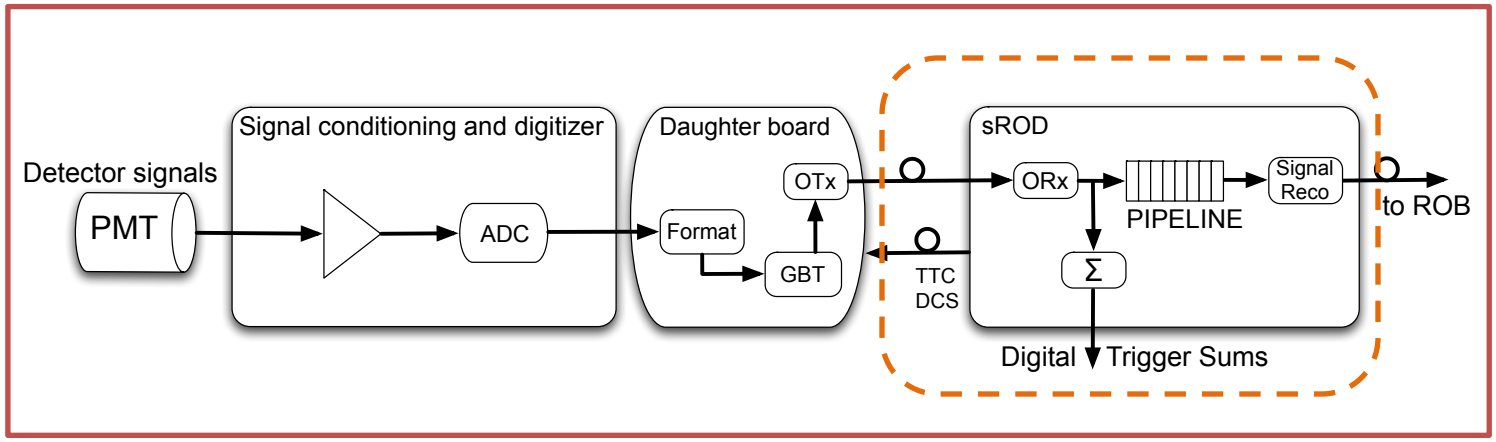
Phase II – Impact on Back-end

Move some FE functionalities off detector:

- Increase ROD input bandwidth by 100
- Output to DAQ after L1 unchanged
- New output to L1/L0 Calo

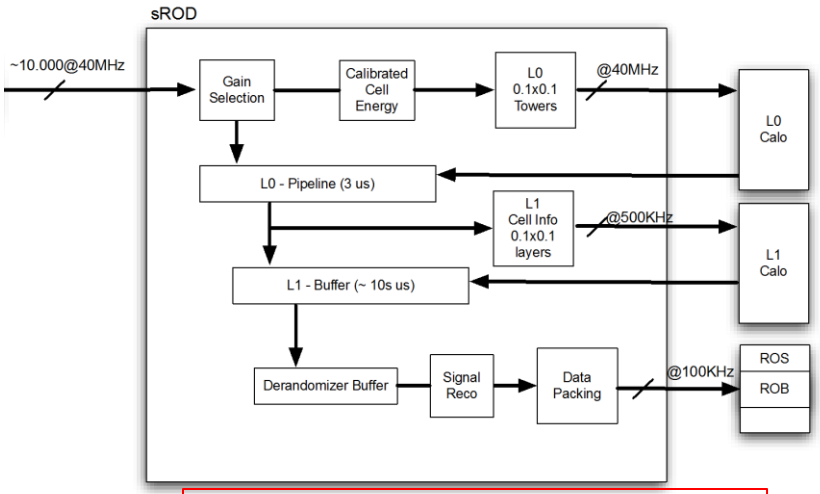
- sROD functionalities:
  - **Pipeline memories & derandomizers**
  - **L1/L0Calo PP and Interface**
  - Signal reconstruction, L2 algorithms
  - Interface with DAQ
  - **DCS/ TTC to FE**

	Present	Upgrade
BandWidth	~ 165 Gbps	~20 Tbps
Nr. fibers	256	8192
Fiber BW	640 Mbps	10 Gbps
Nr. RODs	32	32?
ROD Crates	4	4
Input BW/ROD	5 Gbps	625 Gpbs
Out BW/ROD $_{DAQ}$	2,56 Gbps	10 Gbps

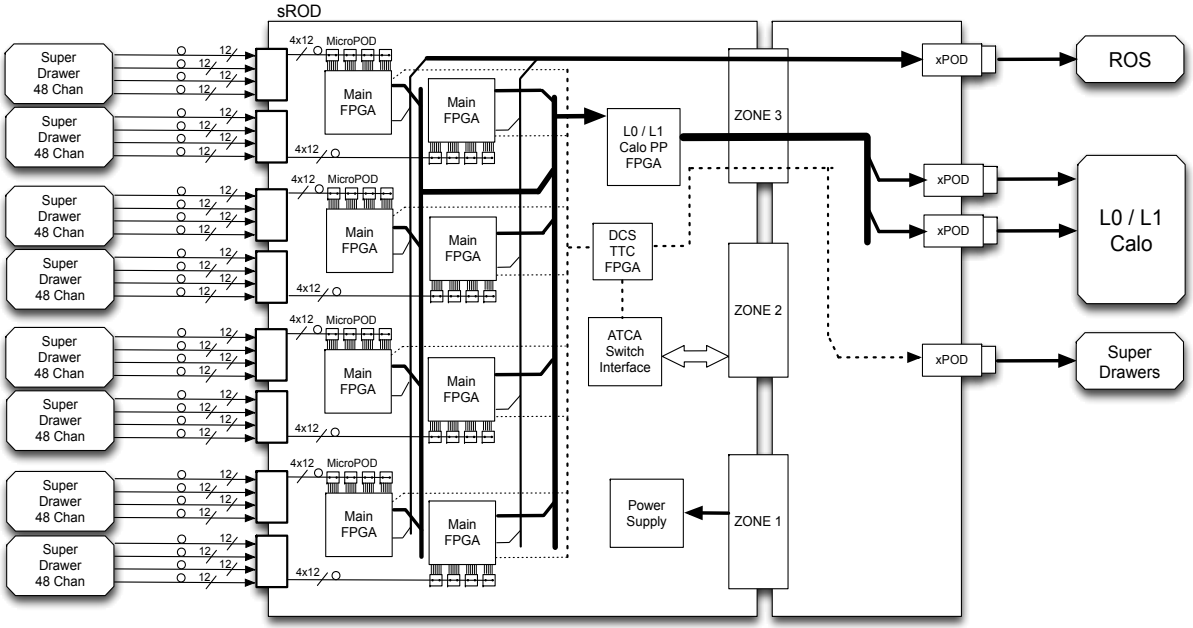


sROD module for Phase-II

- The sROD "system" will absorb some front-end functionalities:
  - Pipeline(s), BCid, L1/0 PP, DCS/TTC distribution
- The plan is to keep present partitioning in terms of:
  - Number of SD processed by each sROD (8) and crates.
  - Feasible already with present technologies.
- TTC partitions will depend on mapping of SD to sROD
  - Two TTC partitions if positive/negative eta to different sROD
  - 0.4×0.4 L0/L1 trigger regions per sROD (with full digital TTs)



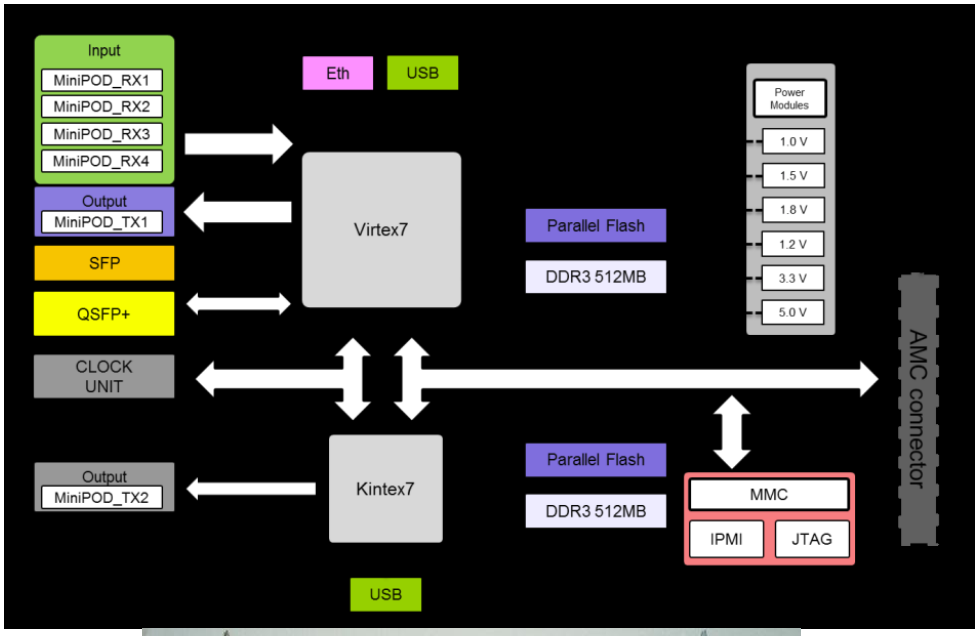
Note new trigger format: old L1calo split into L0 (fast) and L1' streams

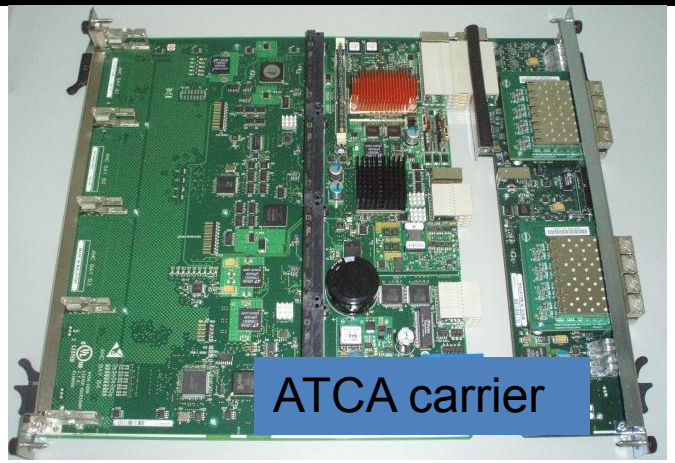


- Ongoing study of algorithms for BCID identification and energy reconstruction @ 40 MHz:
  - De-convolution algorithm implemented in FPGAs
  - Dependent on the front-end option used

sROD Demo Board Under Construction

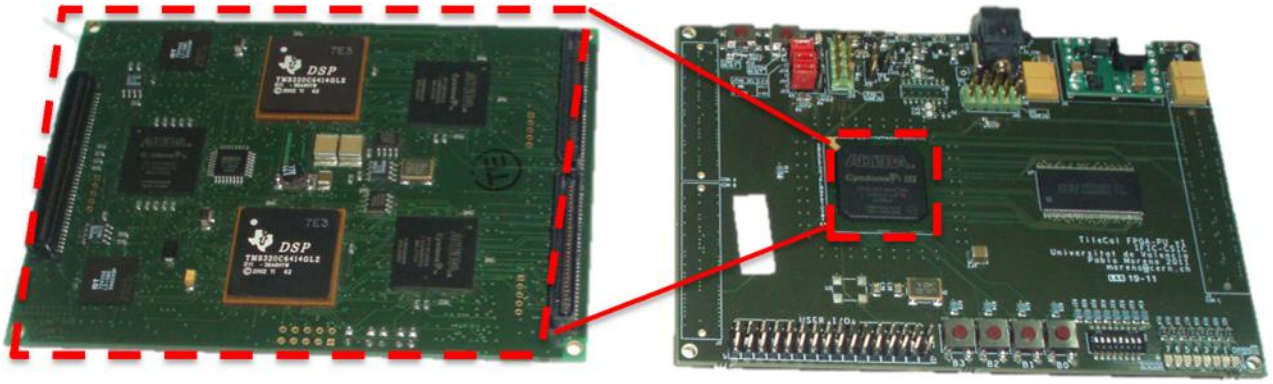
- AMC standard compliant
  - Double mid-size AMC (180.6x 148.5 mm)
  - Can be plugged in a ATCA carrier or in a uTCAplatform
- Processing Units:
  - 1 Xilinx Virtex7 FPGA:
    - XC7VX485T-2FFG1558 (48 GTX)
  - 1 Xilinx Kintex7 FPGA:
    - XC7K480T-2FFG901 (24 GTX)
- Memories:
  - DDR3 SDRAM
  - Flash memories
  - EEPROM
- Communications
  - USB interface
  - Ethernet Port (10/100/1000)
- Parallel optics
  - 4 x Avago RX MiniPODs(12 x 10Gbps)
  - 1 x QSFP+ module
  - 2 x AvagoTX MiniPOD(12 x 10Gbps)
  - 1 x SFP connector





Other R&D Underway

- HV System and PMT Bases
  - Problem of high currents in forward region requires new active bases
  - Study of HV distribution system redesign underway
    - Studying radiation tolerance of opto-isolators
- Evaluation of Digital Filtering algorithms in FPGA
  - Higher processing power that present system allow us to consider more sophisticated algorithms to deal with higher PU

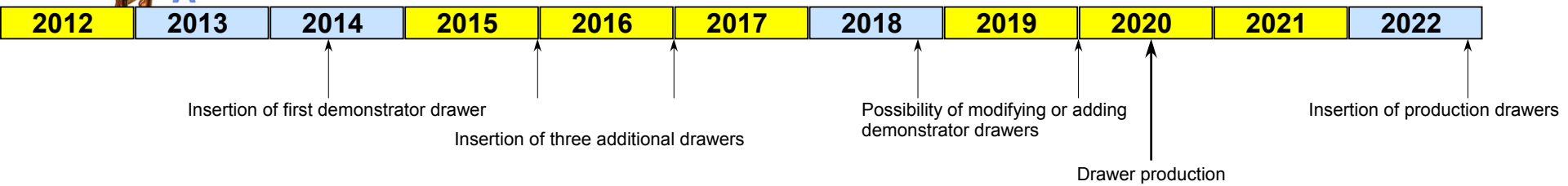


Assessing Performance and Radiation Tolerance

- We need a more rigorous study of simulation of alternative timing structures and luminosity leveling to understand the Tilecal baseline and effect of pileup
  - Influences shaping time or indicates non-shaped direct integration
- Radiation tolerance, error recovery, and SEU have been studied for components in a number of facilities:
  - Hospital proton accelerators, reactors, ANL APS beam dump, ANL electron linac, BNL Cs source
    - Potential new FNAL facility in meson beamline could simulate LH-LHC cavern
- Biggest challenge: beam tests of full Tilecal wedge
  - Much was learned … and fixed … for the current calorimeter

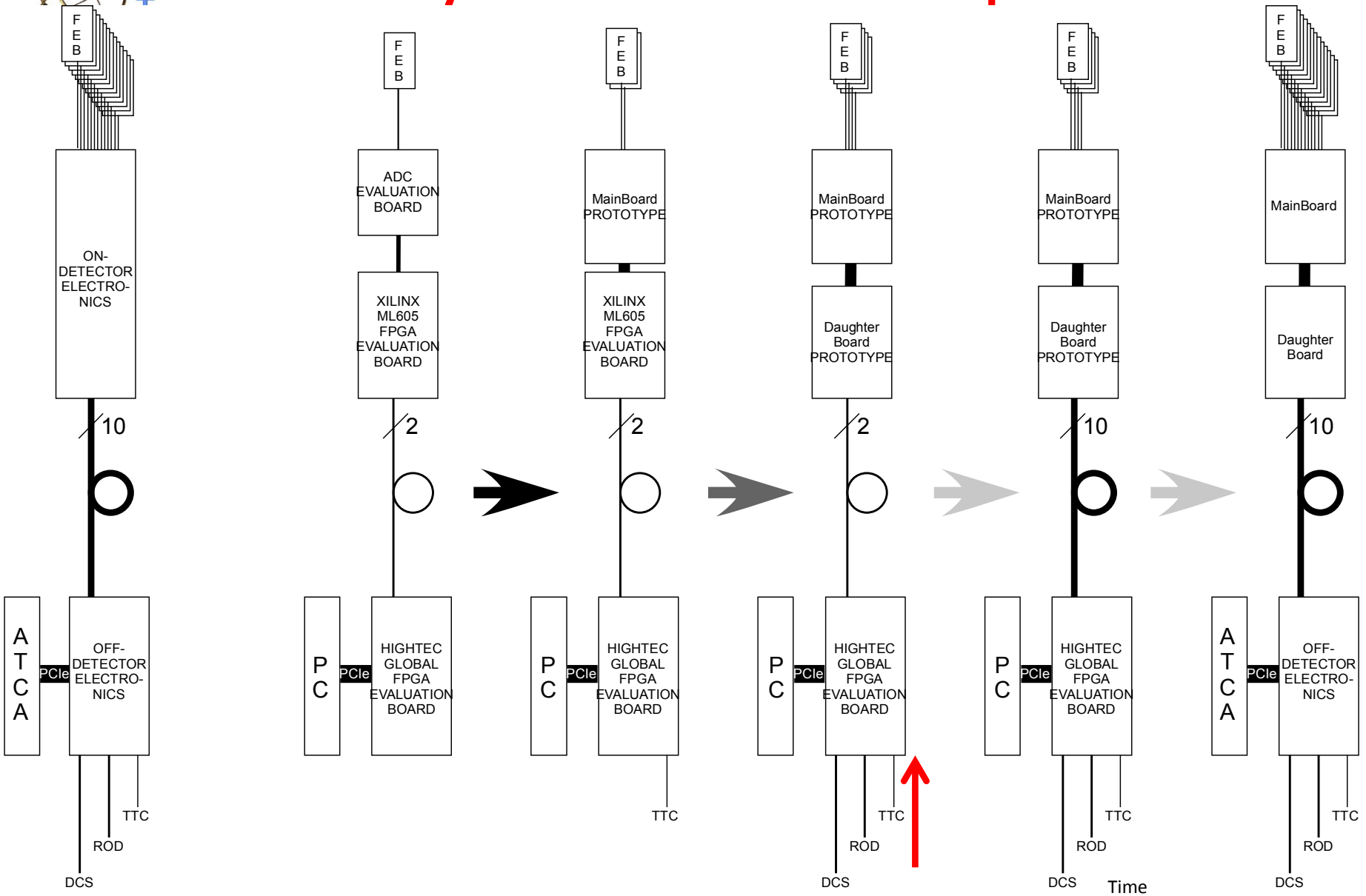
Only through this chain of simulations and tests can we confidently decide on the FEB design and communications package.

Demonstrator Phases



- LS1 (by June 2014)
  - install and test one wedge using discrete-component front-end board
    - commercial point-of-load regulators
    - SNAP-12 or QSFP optical communication
    - current HV distribution system
  - sROD developed for testing of opt. comm.
- 2015-17: beam testing of FEB options (discrete, ASIC)
- Winter shutdowns 2015/16, 16/17
  - insert additional wedge with ASIC option(s)
    - with POL regulation
    - possibly with modulator optical communications
- LS2: replace wedge with final prototype
- 2020: need to begin Phase-II production

Summary of Incremental Development



We are here

Time
Completeness
Effort
Cost

Future system

Summary and Conclusions

- TileCal upgrade goals and architecture are well defined
- Designs and prototypes of each task are on schedule
- Solutions have been found for a DEMONSTRATOR installation in LS1
- Some critical Phase-2 components and options still under development:
  - Point of Load regulators
  - ASIC integrated amplifier/shaper/digitizer alternatives
  - Optical modulators
  - HV distribution
  - Phase-2 Back-end electronics