UNIVERSITAT DE BARCELONA

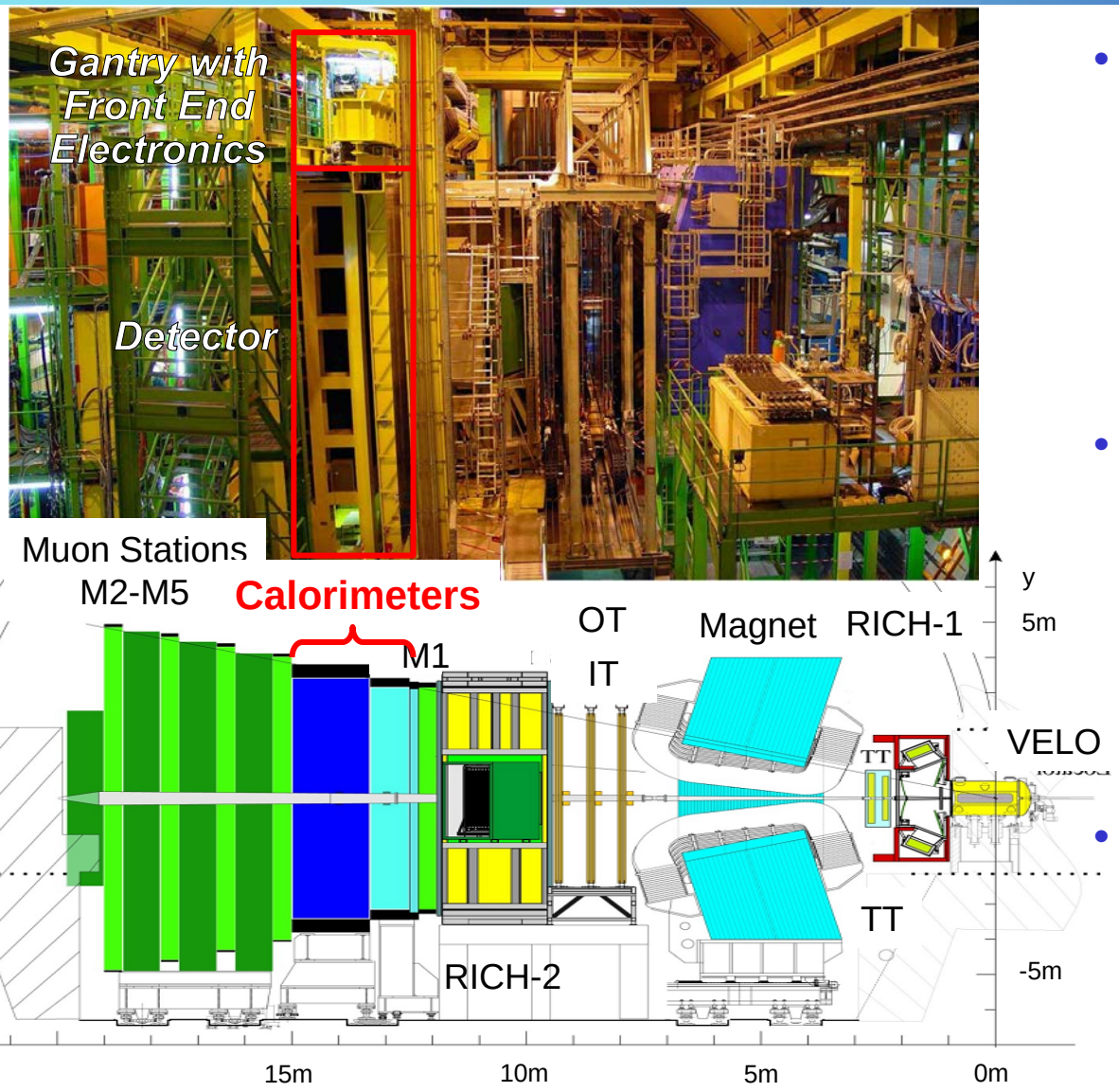
LHCb Calorimeter Upgrade Electronics

E. Picatoste (Universitat de Barcelona)

On behalf of the LHCb group

CHEF 2013 – 22-25th April 2013 – Paris

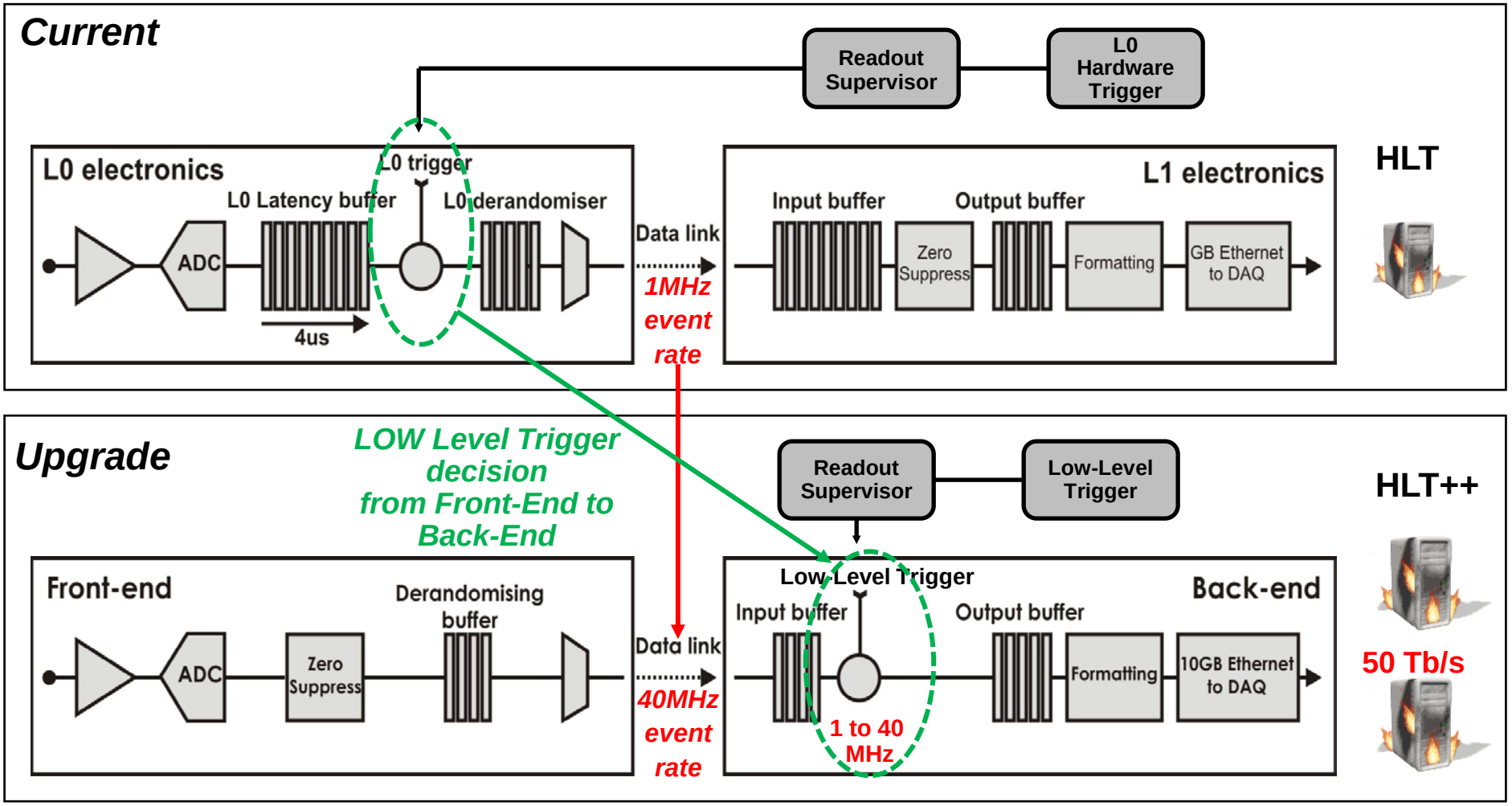
LHCb Upgrade



- Statistical improvement if:
  - Increase of data rate from 1 to 5fb^{-1}/year
  - Increase luminosity to 2x10^{33} cm^{-2}s^{-1}
  - Increase trigger efficiencies
- Current L0 trigger limited by electronics ⇒upgrade:
  - Trigger in software
  - Use data from every bunch crossing
  - Upgrade electronics and DAQ
- Scheduled for the long LHC shutdown in 2018.

More details on "LHCb Calorimeter upgrade": talk of Yu. Guz, this conference

Upgrade Architecture



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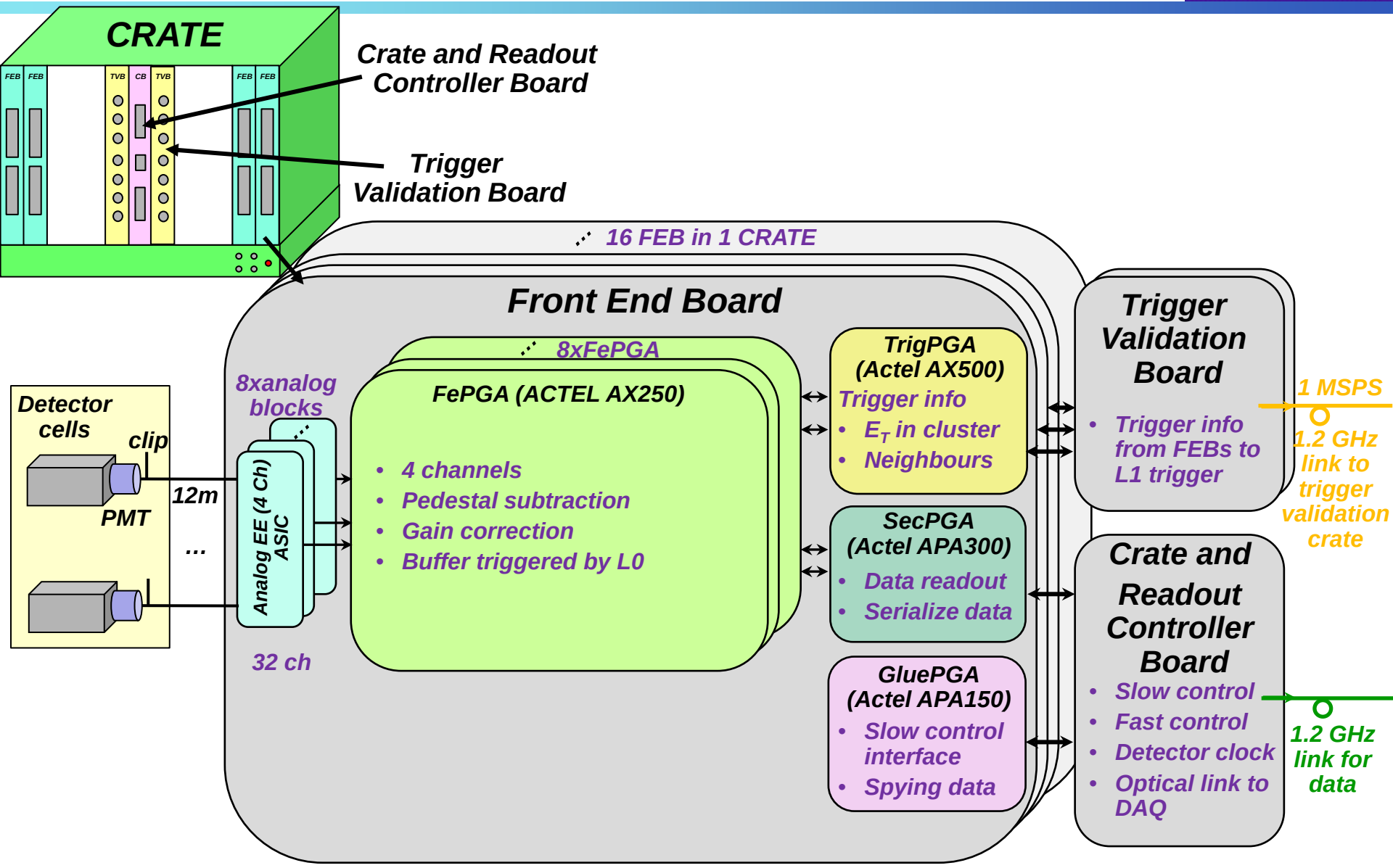
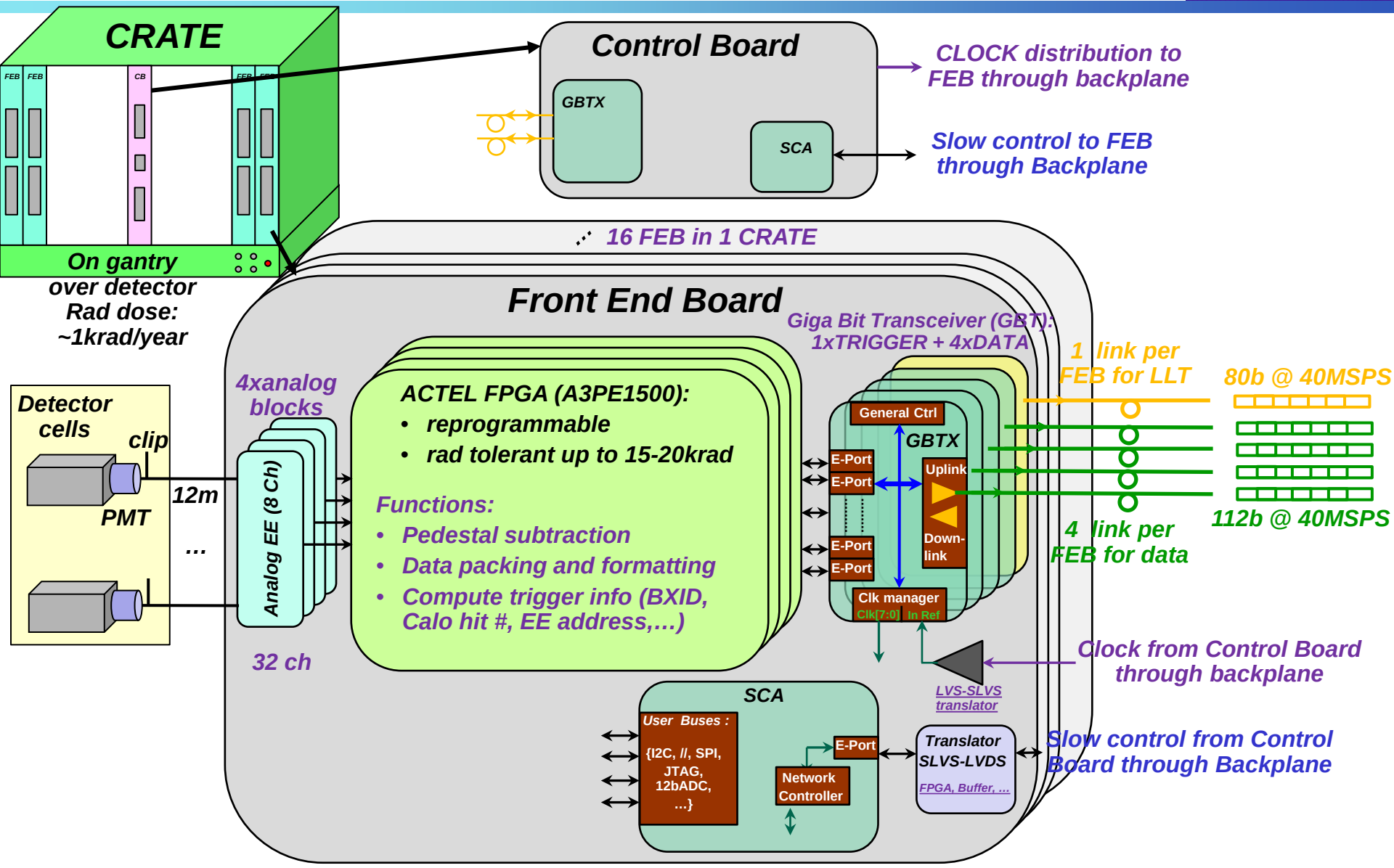
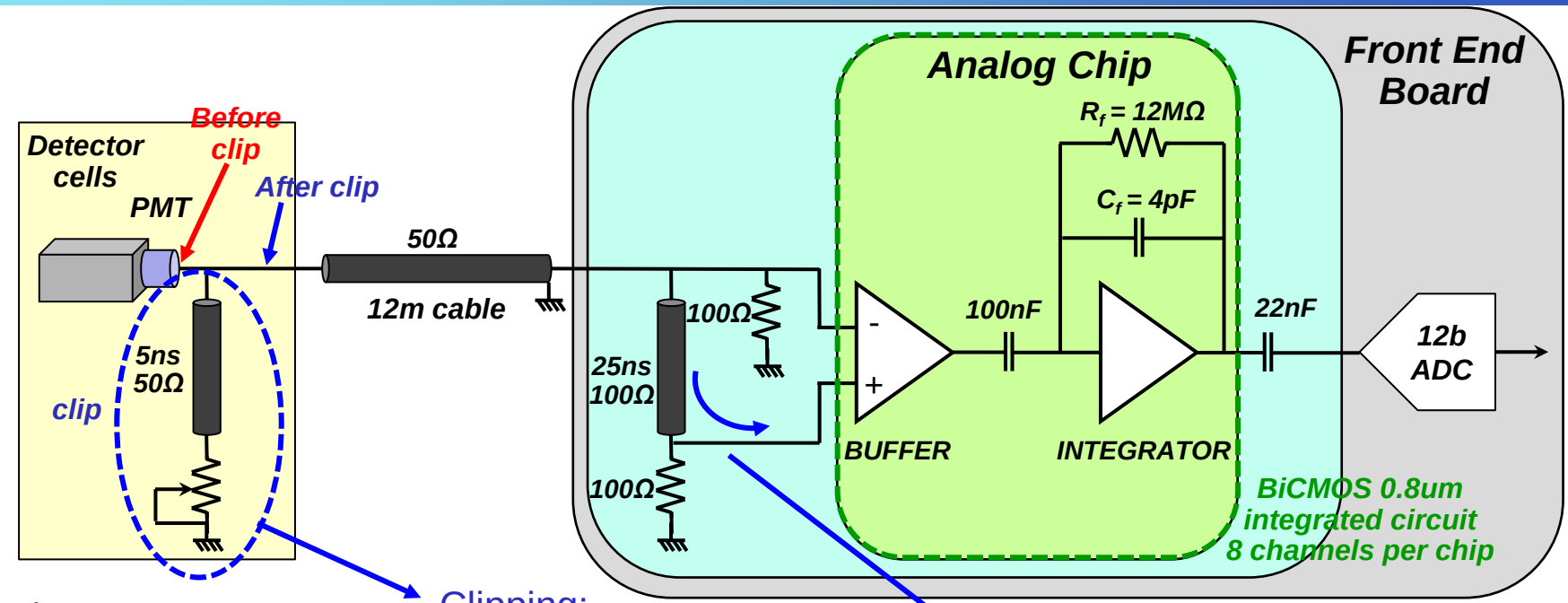
Current Front-End Electronics



Upgrade Front-End Electronics



Current Analog Signal Processing



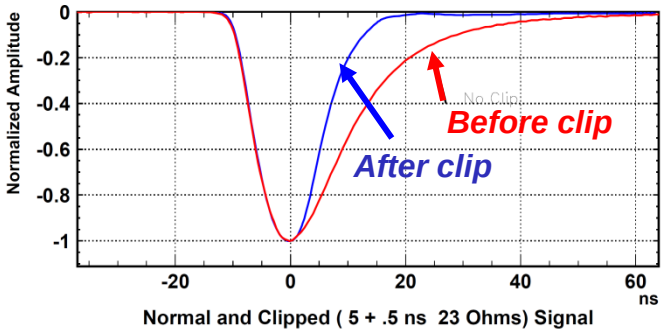
Specifications:

- Pulse shaping in 25ns
- Spill over < 1% after 25ns
- Integrator plateau: 4ns
- Linearity < 1%
- Rise time ~ 5 ns

Clipping:

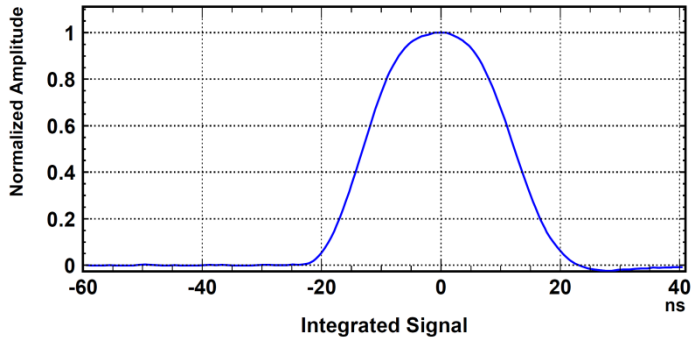
⇒ Reduce signal tail

⇒ Reduce spill over

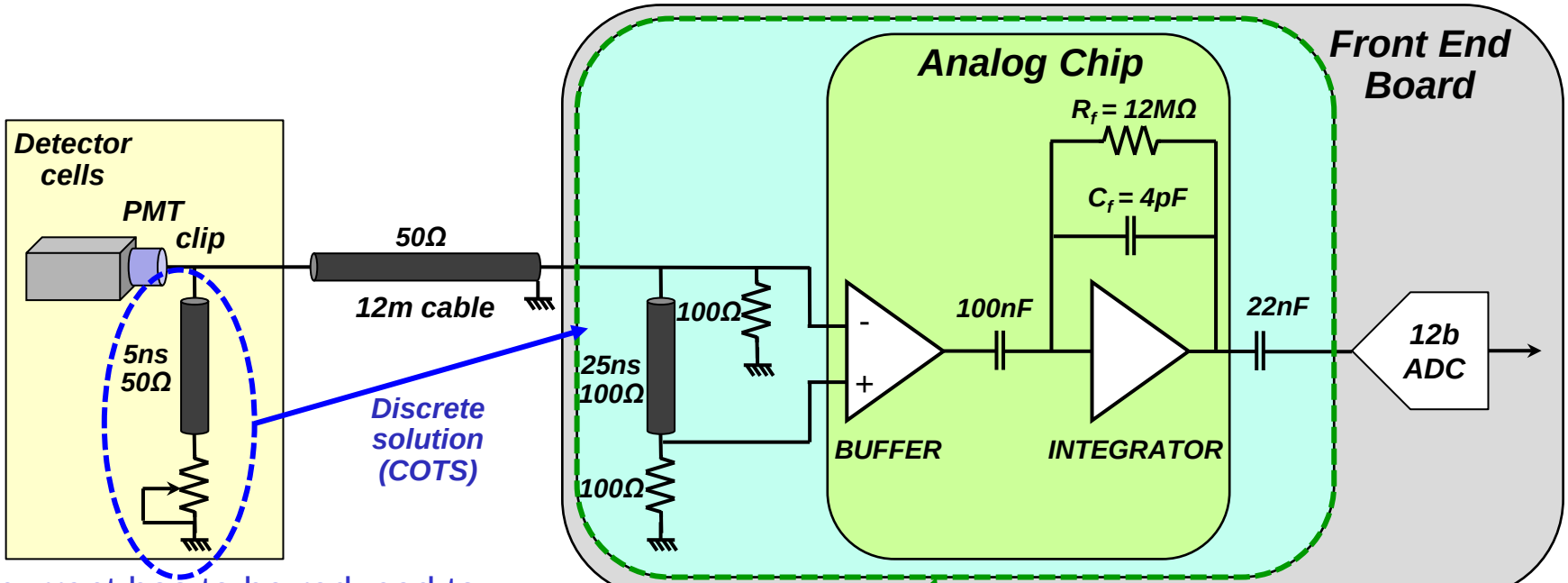


Integrator discharge:

Clipped signal + delayed negative clipped signal



Analog Electronics Upgrade Motivation



PMT current has to be reduced to increase lifetime

⇒ FE electronics gain has to be increased correspondingly

– BUT FE noise should not be increased in the operation!

Noise < 1 ADC Count

– For 12 bit DR, input referred noise <1nV/sqrt(Hz)

⇒ Termination resistor at input generates too much noise

Solutions:

– New ASIC
  - ✓ Increased gain
  - ✓ Active cooled termination

– Discrete solution: Components Out-of-The-Shelf (COTS)
  - ✓ 2/3 of the signal are lost by clipping
  - ✓ Remove clipping at the PM base (detector)
  - ✓ Perform clipping after amplification in FE using delay lines

ASIC Channel Architecture

Very difficult to integrate in ASIC HQ analog delay lines

↓

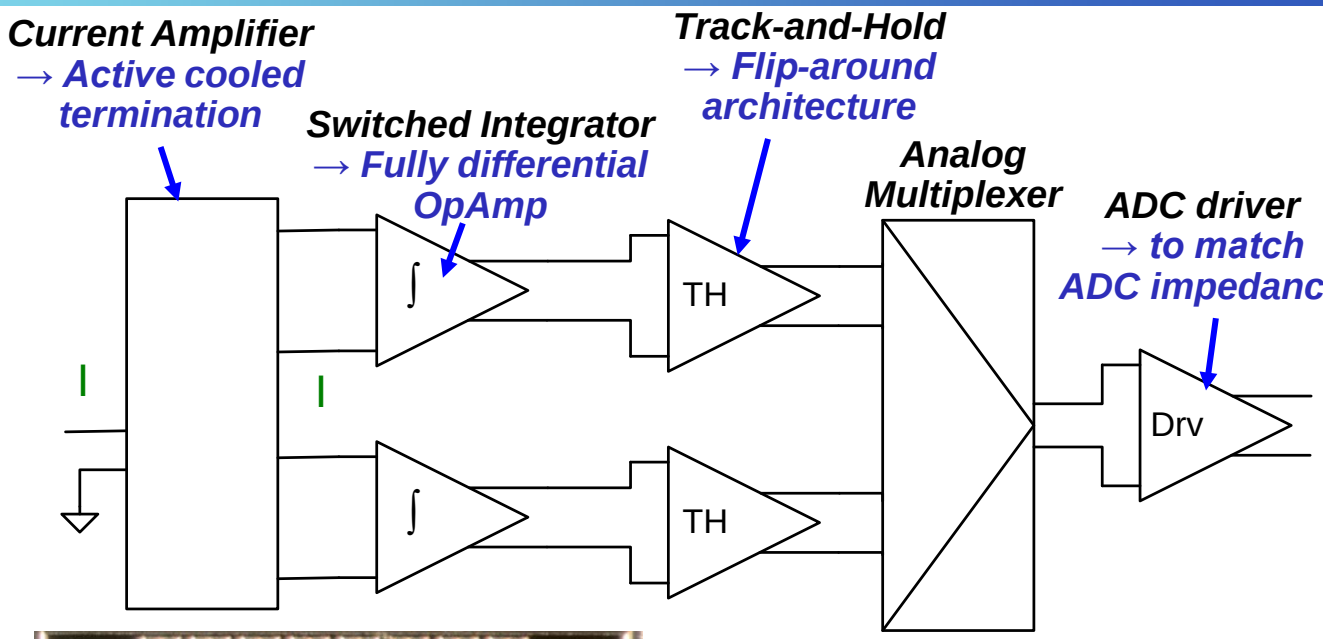
*2 switched alternated paths**

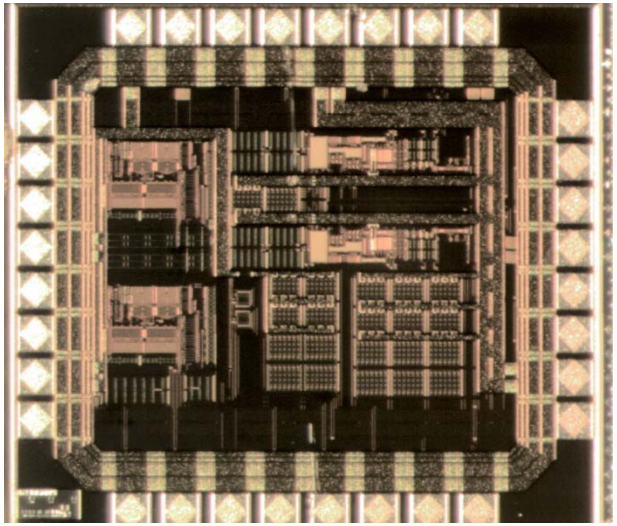
↓

Switching noise!

↓

Fully diferential ASAP





Two prototypes already designed and tested:

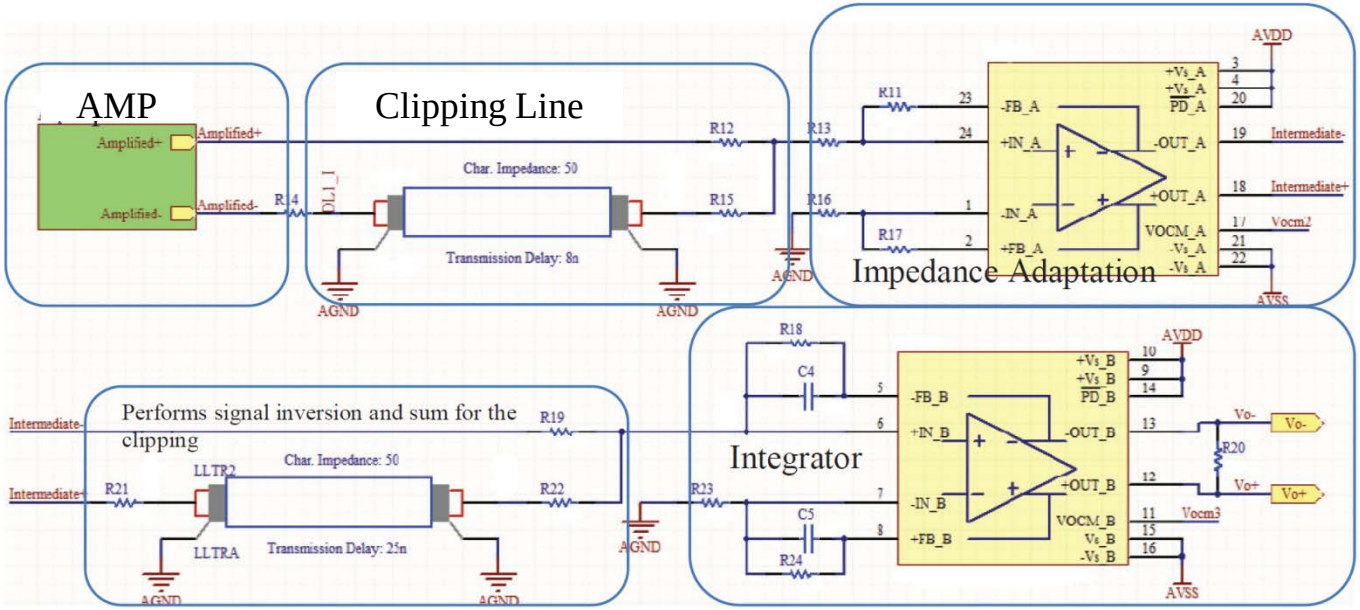
- Preamp + integrator
- Preamp + integrator + TH

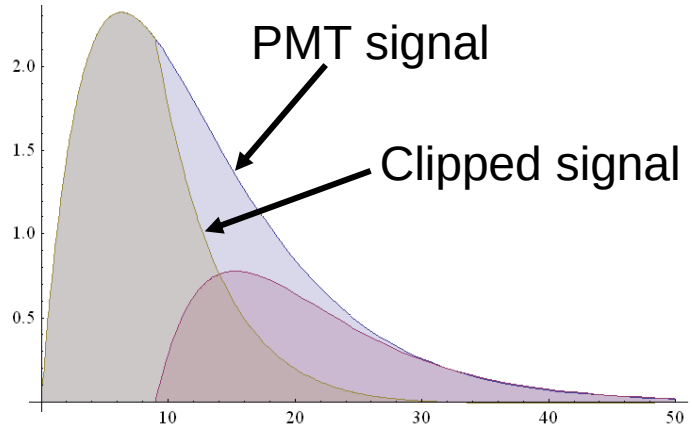
Technology:

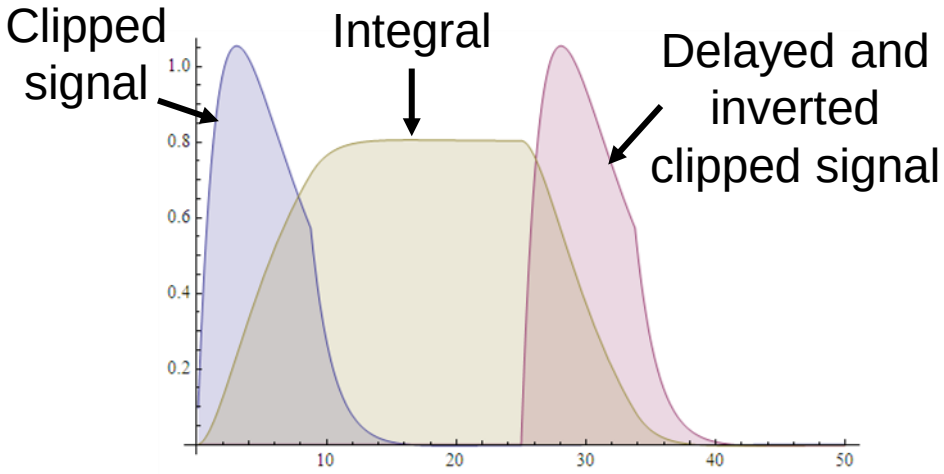
- SiGe BiCMOS 0.35um AMS

** Used successfully in LHCb PS/SPD Calo*

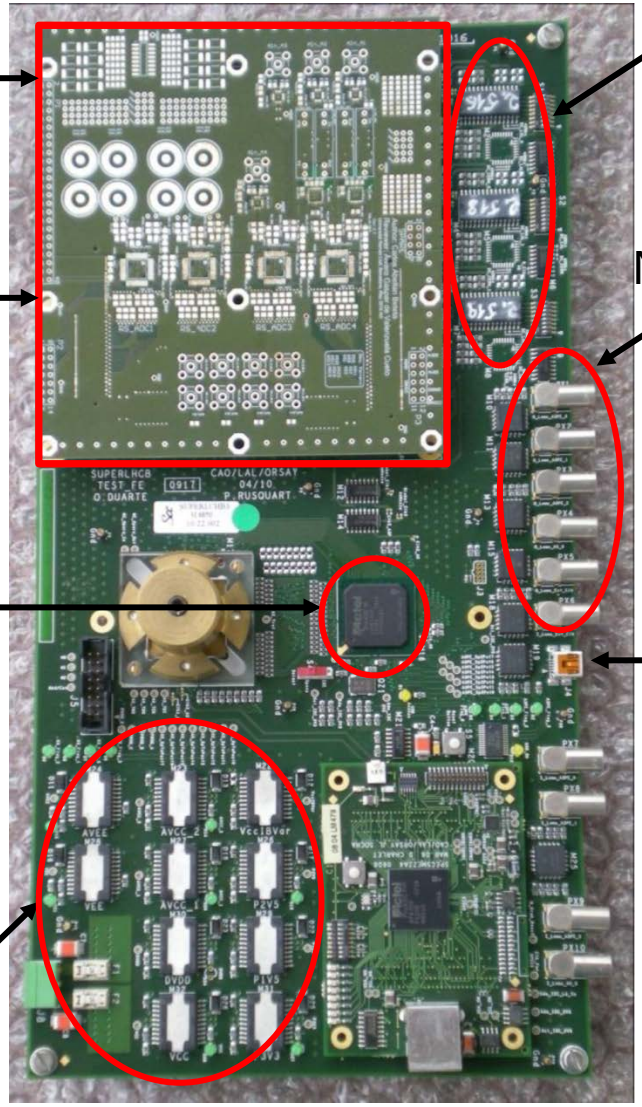
COTS Channel Architecture







Front End Board Prototype Tests



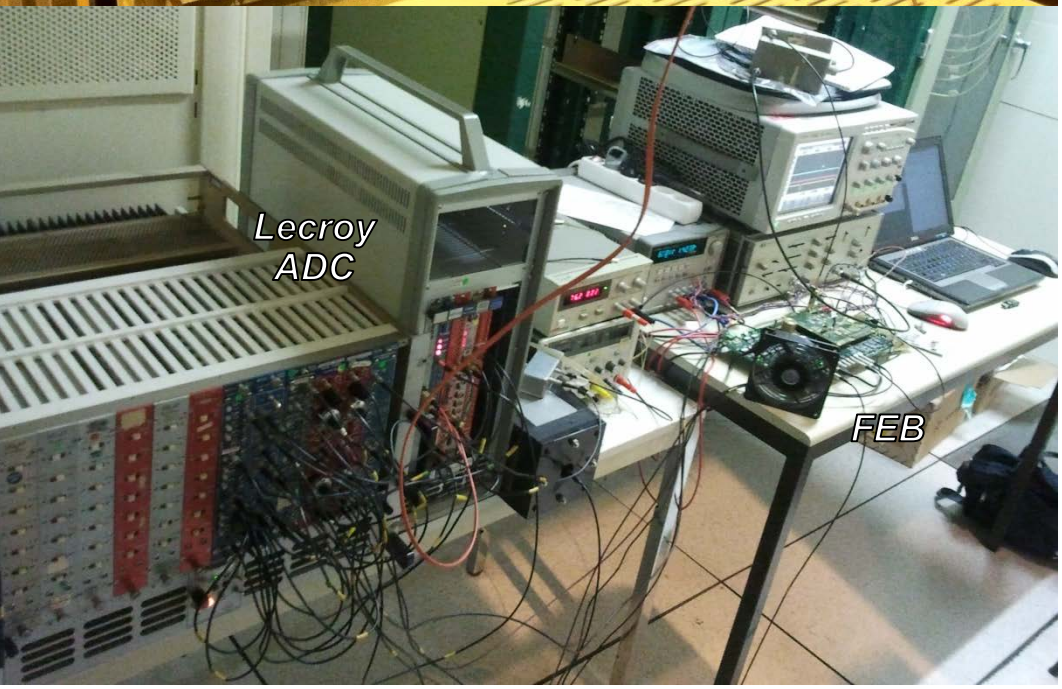
Verilog blocks:

- USB and control board
- General functionality
- DAQ

- Tests:
  - Linearity
  - Noise
  - Integral plateau
  - Spill over

Test Beam Measurements (Nov. 2012)

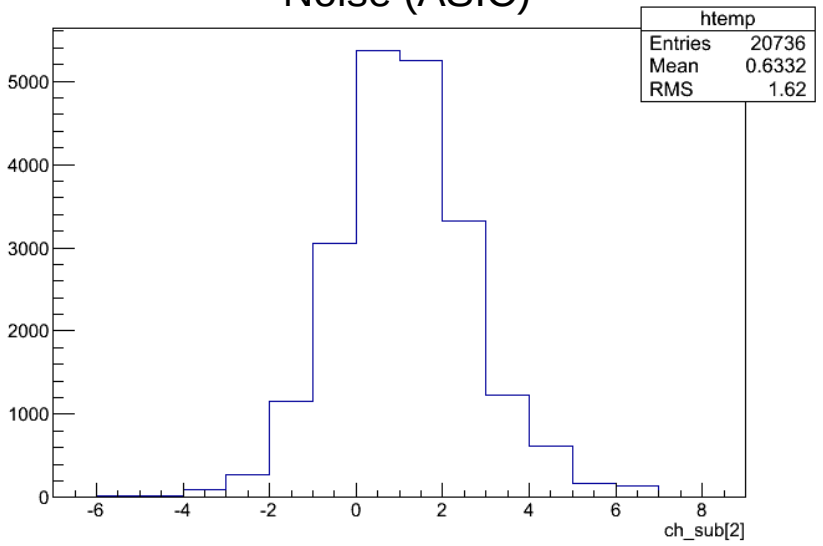
ECAL channel+PMT+same 12m cable



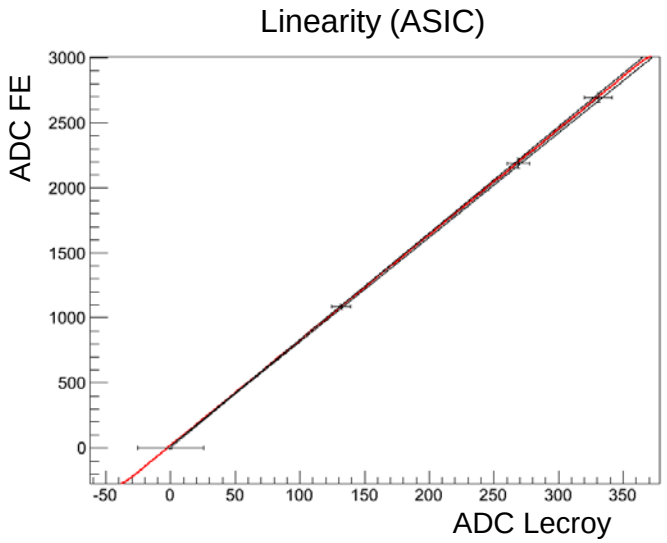
- Used e- of 50 to 125GeV
- Measurements:
  - Noise after pedestal subtraction: ~1.6 ADC (ASIC) and ~2.6 ADC (COTS)

    → Contribution of 10-15% due to the use of a “T” to distribute the signal

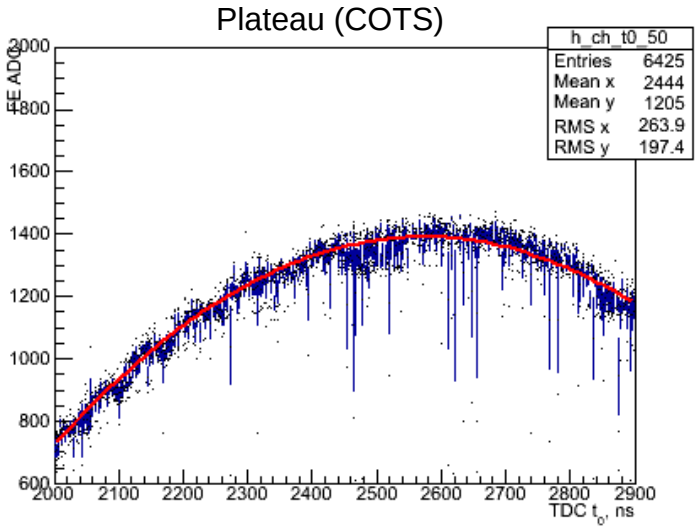
Noise (ASIC)

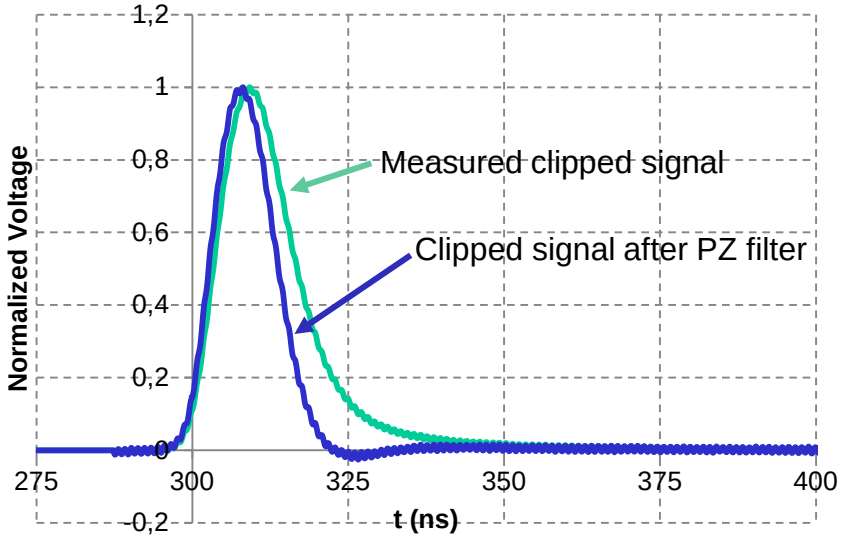


Test Beam Measurements (Nov. 2012)



- Measurements (cont'd):
  - Linearity better than 1%
  - Integral plateau ~1.6% at ±2ns (ASIC) and <1% (COTS)
  - Spill over of ~8% in following sample (ASIC)
- Pulse width underestimated (due to cable and clipping effects):
  - Affects plateau and spill over
  - ⇒ Pole-zero filter proposed for final version of ASIC/COTS



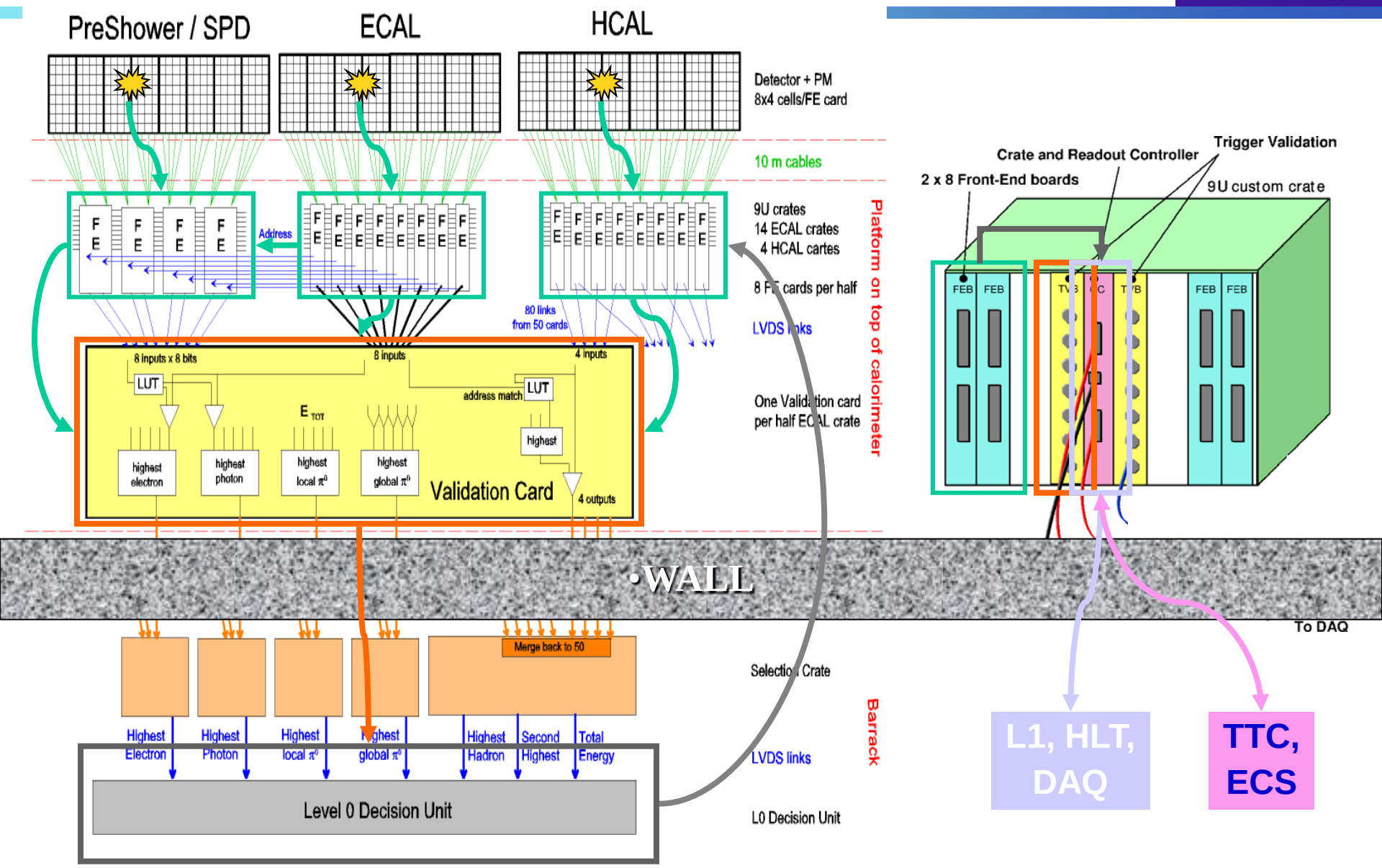


Summary

- Upgrade architecture with new Front-End electronics board
  - 40MHz readout
  - Re-use FE crate
  - Actel FPGA reprogrammable A3PE family
- Analog shaping electronics: two solutions
  - ASIC:
    - cooled input termination for reduced noise
    - 2 interleaved channels and switched integrators: no deadtime
    - Full 4 channel ASIC to be sent in June 2013
  - Discrete elements (COTS):
    - Clipping removed from PMT base and installed in the FEB: increase in signal
    - Definitive version scheduled by end of May 2013
  - Final decision before September 2013
- Prototypes tested both at lab and at a test beam
- Radiation qualification tests foreseen
- Technical Design Report (TDR): September 2013

Back up

Current Trigger and Readout Architecture



Upgrade Architecture