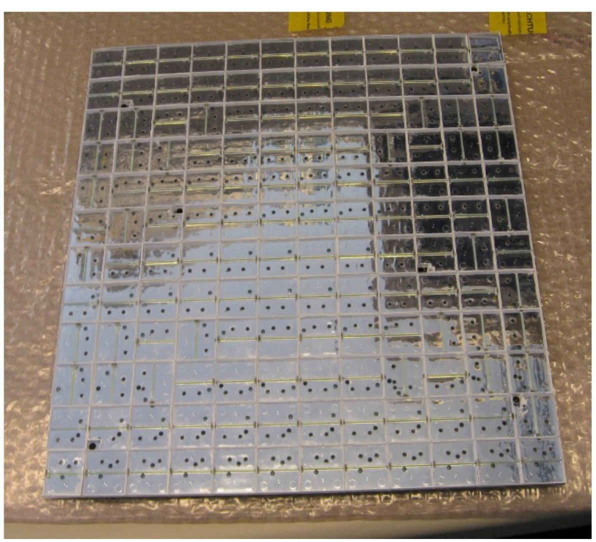
Towards hadronic shower timing with CALICE Analog Hadron Calorimeter

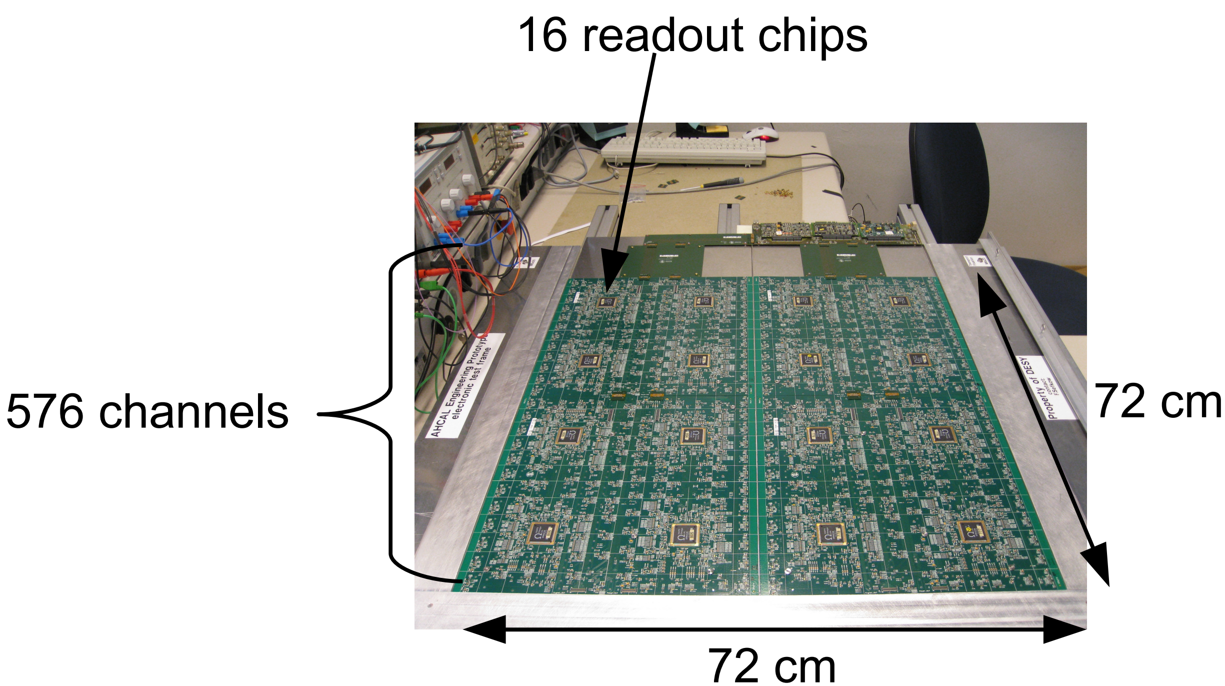
Marco Ramilli
on behalf of
the CALICE Collaboration

CHEF 2013 - Paris, 23/04/2013

Overview

- 2006 – 2011: first generation of AHCAL prototype
- 2011 – ongoing: second generation of AHCAL prototype
- Physics motivation
- Commissioning of the first layer
- Summary and Outlook



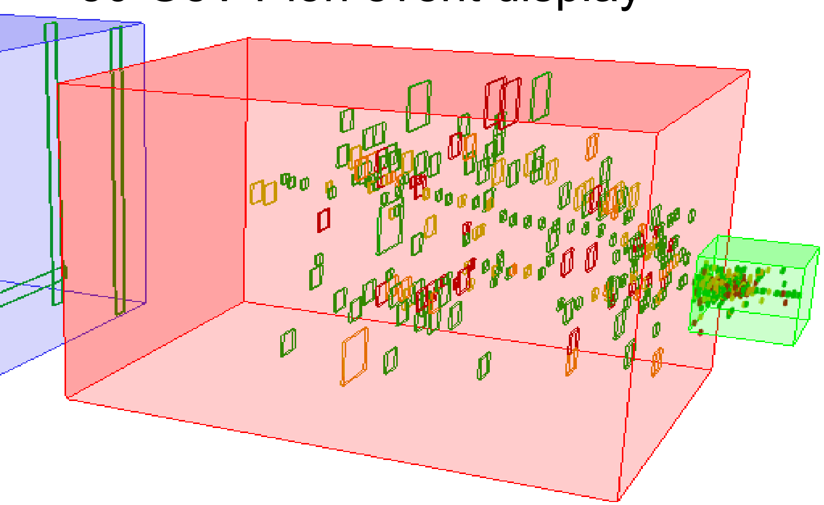


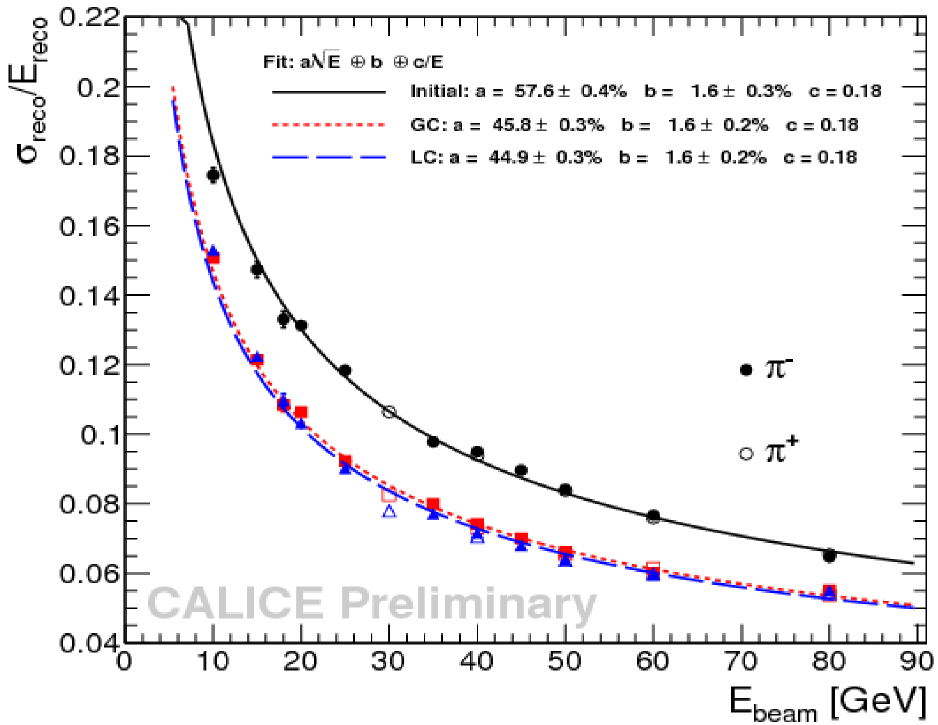
Highly granular calorimeters

highly granular calorimeter prototypes for **particle-flow**

First generation prototype:
- Physics proof of principle
- Energy measurement

50 GeV Pion event display





- Measurements of shower **spatial** development:
  - First hard interaction point
  - Track multiplicity
  - Radial/longitudinal development
- Possibility of **validation for GEANT4** physics lists
  - Transition region (4 GeV – 25 GeV)

More details in talk from M. Chadeeva

A second generation AHCAL prototype

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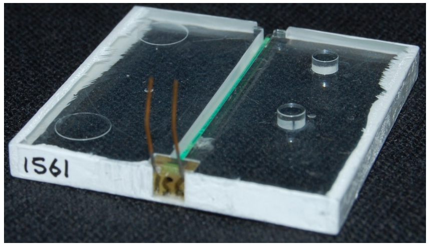
Second generation prototype:
•Scalable technology
•**Integrated readout electronics**

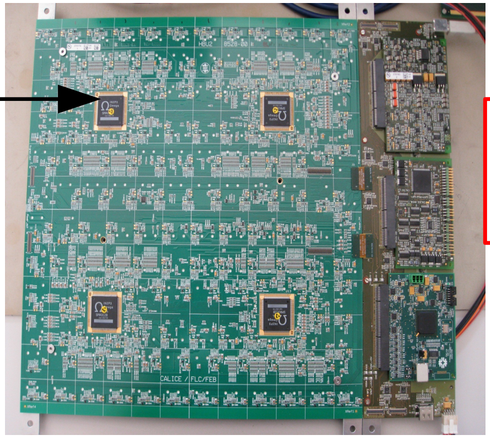


3 cm x 3 cm x 0.3 cm

•Plastic scintillator
•WLS fiber
•Green sensitive SiPM

144 tiles mounted on each **HCAL Base Unit** (HBU)

Read out chips (SPIROC2b)
• 36 channels/chip
• One threshold discriminator per channel
• one ADC per channel
• one TDC per channel
• Low power consumption (25 μW/channel)



More details in talk from K. Krueger

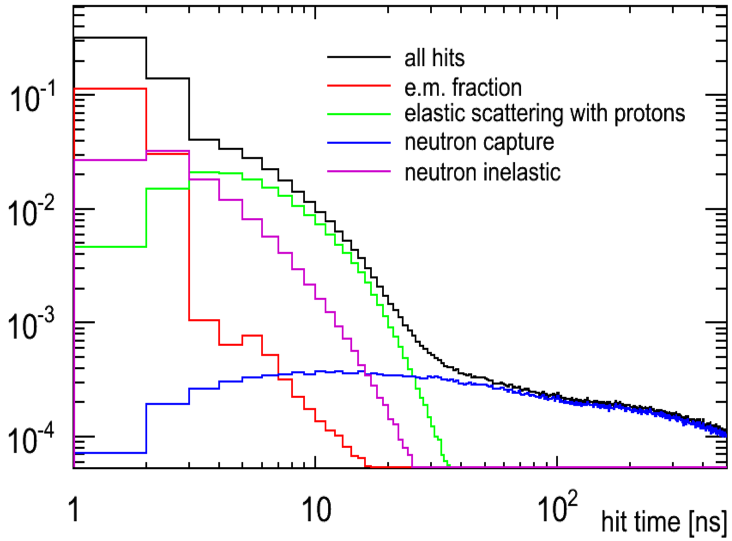
4 HBUs assembled together to form a layer

Technological motivation: test integrated readout electronics

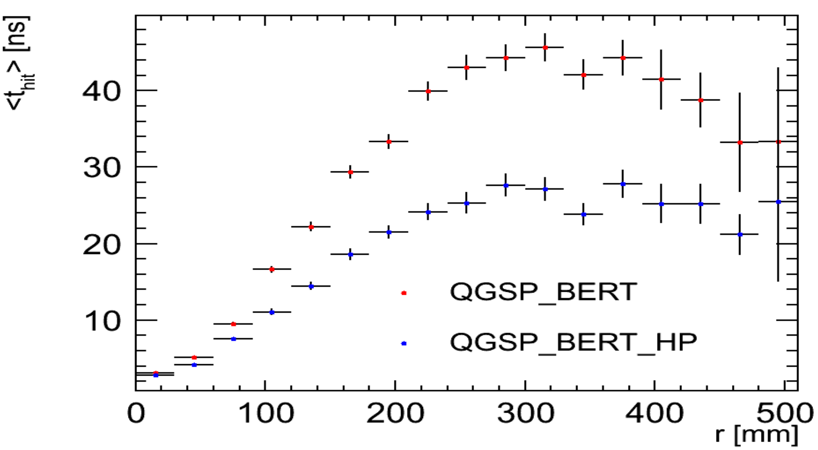
CALICE Calorimeter for ILC

Hadronic shower timing

180 GeV π- QGSP_BERT_HP



180 GeV π-



First timing experiment in CALICE (T3B)
- One dimensional: row of 15 detectors
- Picosecond resolution (not scalable)

see talk from F. Simon

provided first check of Physics Lists timing

Late neutron component in hadronic showers:
Impact on Particle Flow Algorithm
- Estimate effect of pile-up (CLIC)
- Improve shower reconstruction with time cuts

Second generation AHCAL:
- Nanosecond resolution scalable technology
- One layer (soon: multi-layer prototype)

- Test of the time-stamping capabilities
- Apply shower reconstruction algorithm } multi-layer
- Estimate impact of late component

The readout chip

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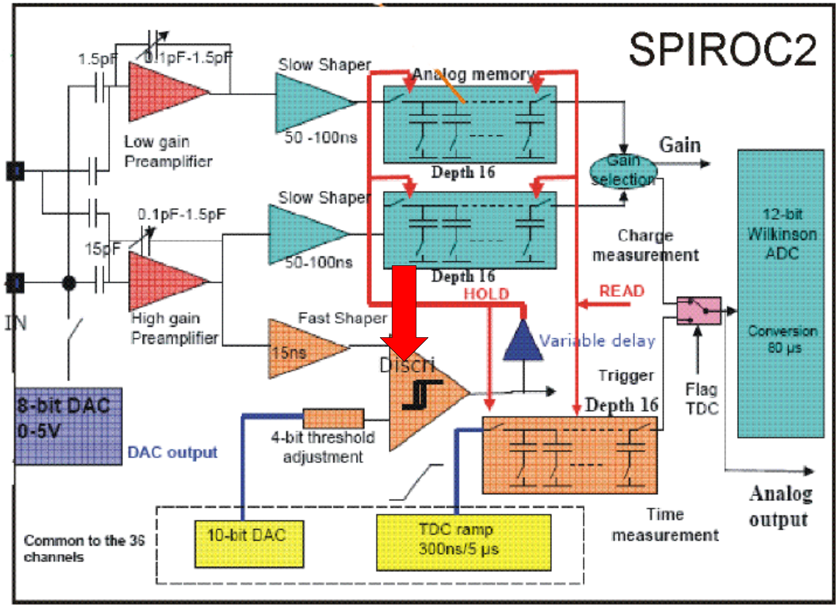
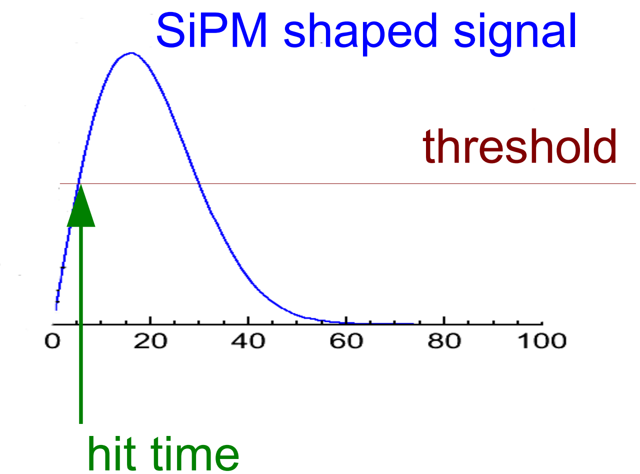
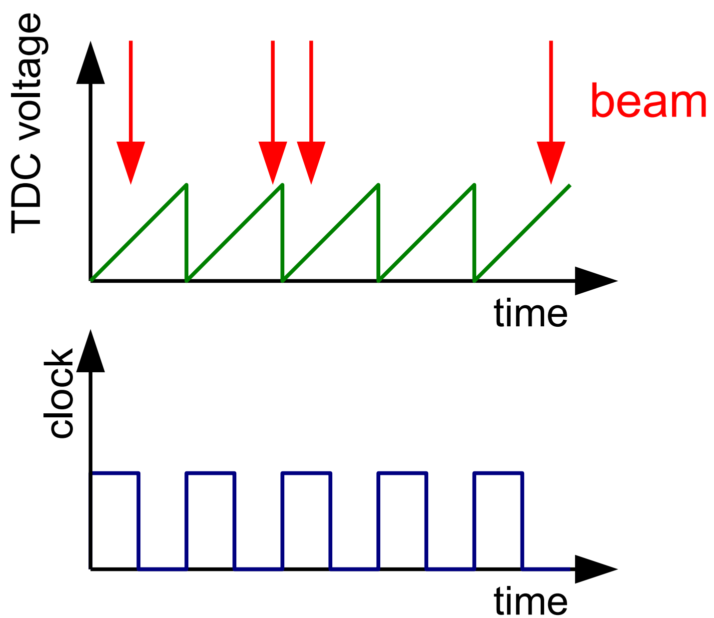
Autotrigger:
a) Cell hit is given by signal passing threshold
b) Cell hit time is the time of signal passing threshold



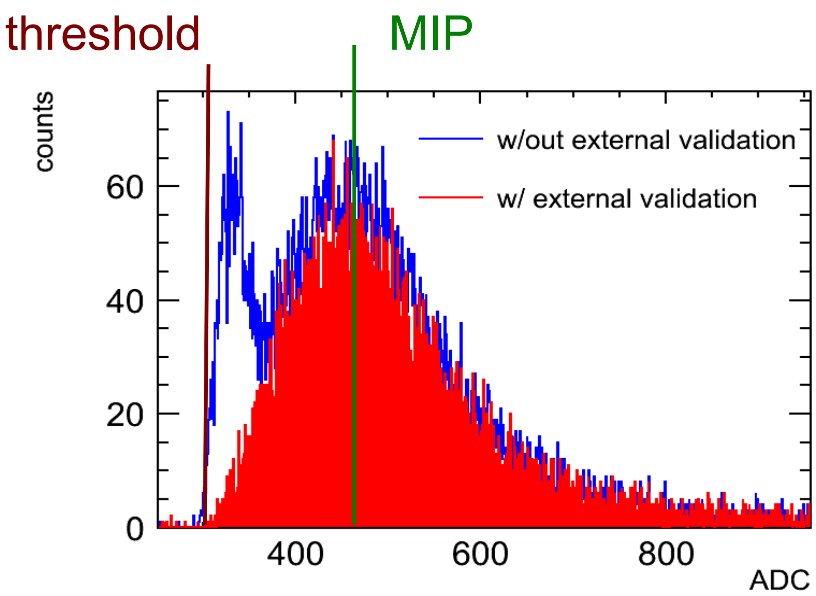




The readout chip has been optimized for LC operation
• Clock synchronized with beam
Not synchronized in test beam operation
External signal from scintillators to provide:
1) absolute time reference
2) event validation

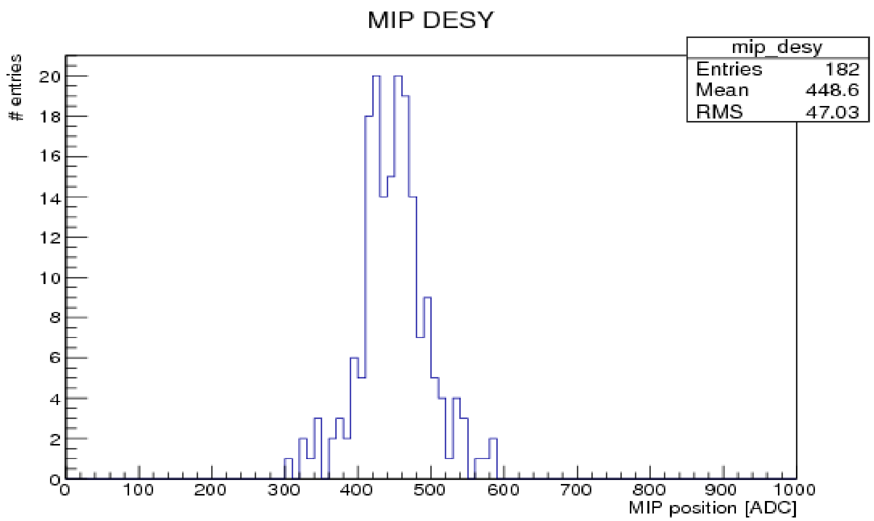
Threshold calibration

DESY test beam: 3 GeV e- **on individual tiles**



- Individual threshold adjustment
- Test for the event validation

Spread of the MIP most probable value ~ 10%
This value includes:
- Individual SiPM bias adjustment
- SiPM gain equalization via pre-amplifiers HBU mounted



TDC calibration

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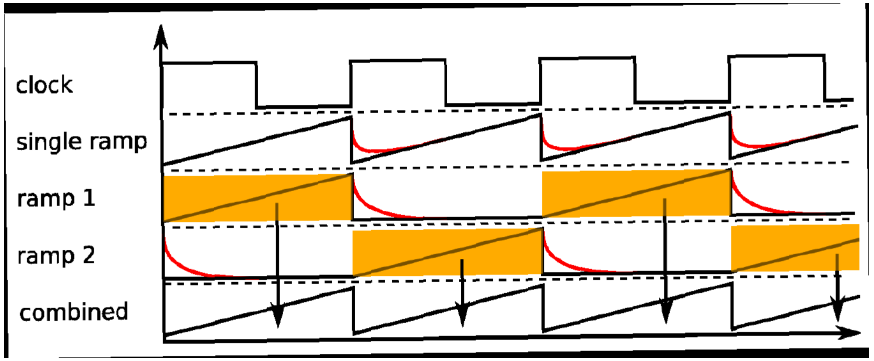
Time stamping:

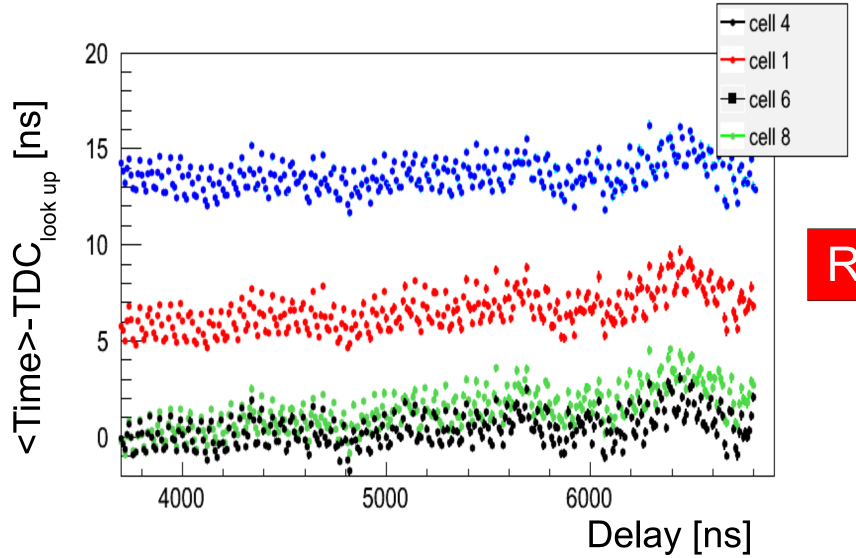
a) 2 multiplexed voltage ramps per chip (adj. length)
- 5 µs long

b) voltage value at hit is stored in memory cell
- 5 µs/4096 bins ~ **1.2 ns/bin**



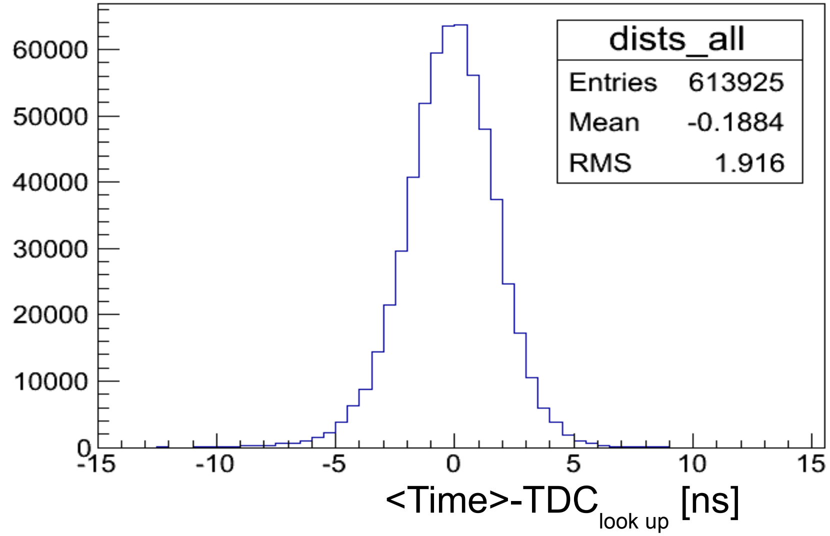
Ramp calibration (charge injection with a pulser): time [ns] = *f*(TDC) + *offset*

each memory cell has a different offset



Rescaling

Single channel spread **~ 2 ns**



To be done for 16 x 36 x16 = 9216 memory cells: calibration still ongoing!

CERN test beam

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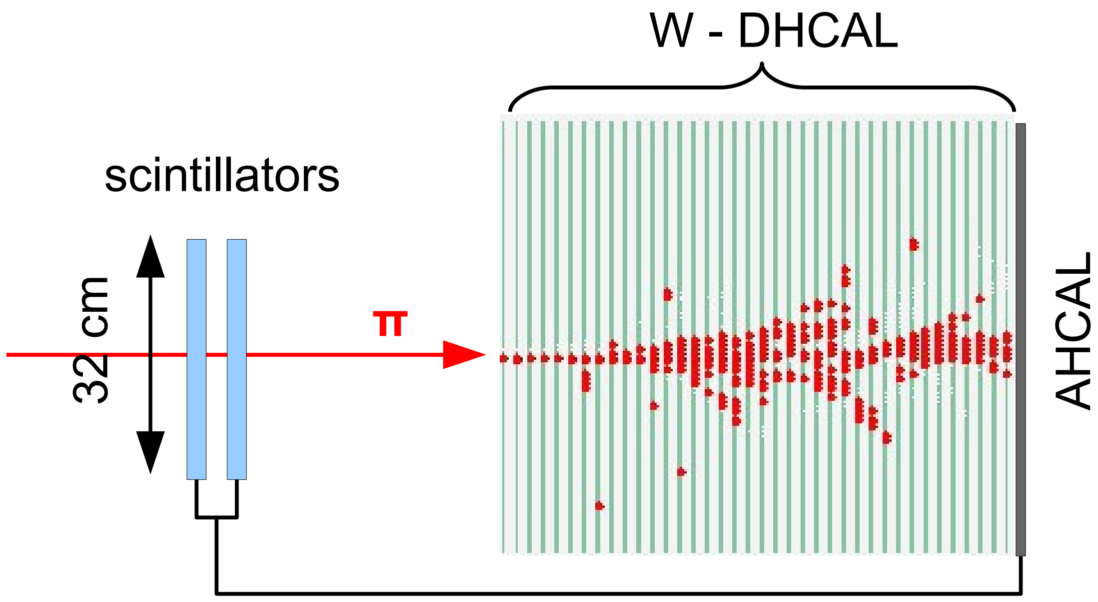

Test beam at CERN SPS:

- Experiments set in conditioned tent: stable temperature conditions
- Muon runs for further MIP calibration
- Pion runs
  - at 50 GeV and 180 GeV
- Trigger scintillators in coincidence
  - into two AHCAL channels for absolute time reference

CERN data

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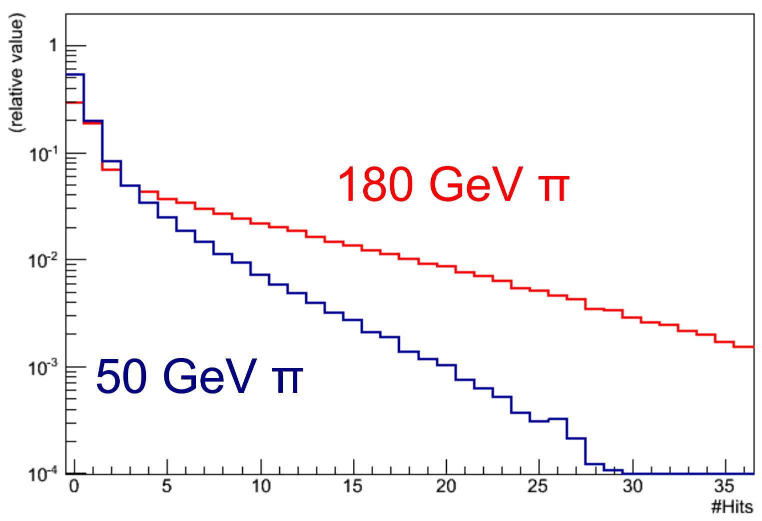
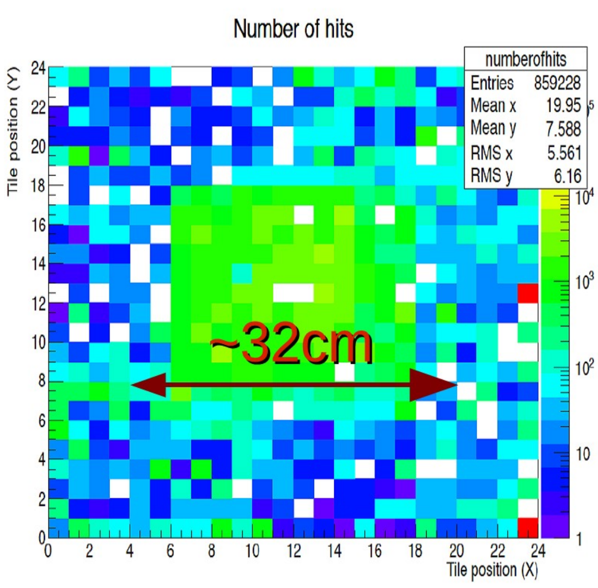
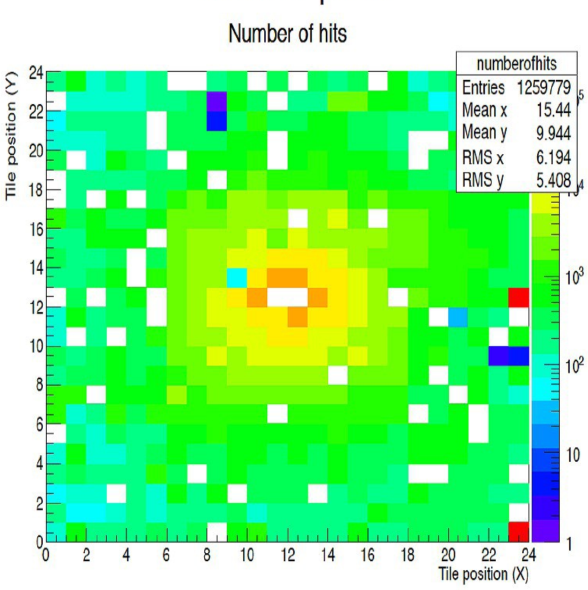
- More than 400k muons
- Pion event reconstruction finalized:
  - 420k pion events reconstructed at 180 GeV
  - 86k pion events reconstructed at 50 GeV
- MIP calibration ongoing
- TDC calibration still ongoing

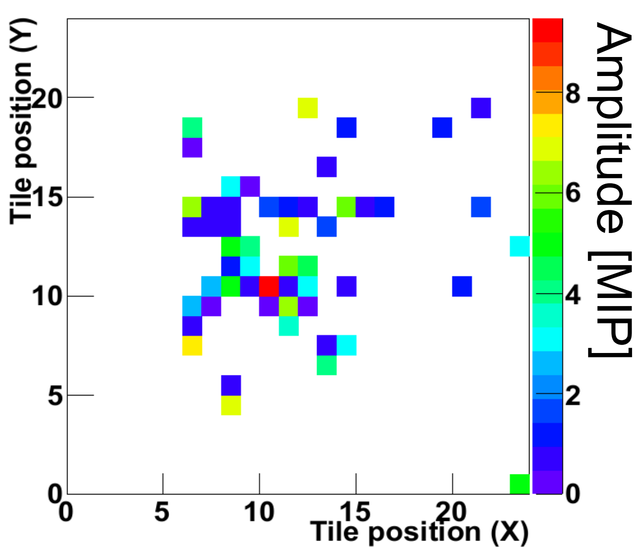


180 GeV muons



180 GeV pions





Calorimeter for ILC

CERN data quality

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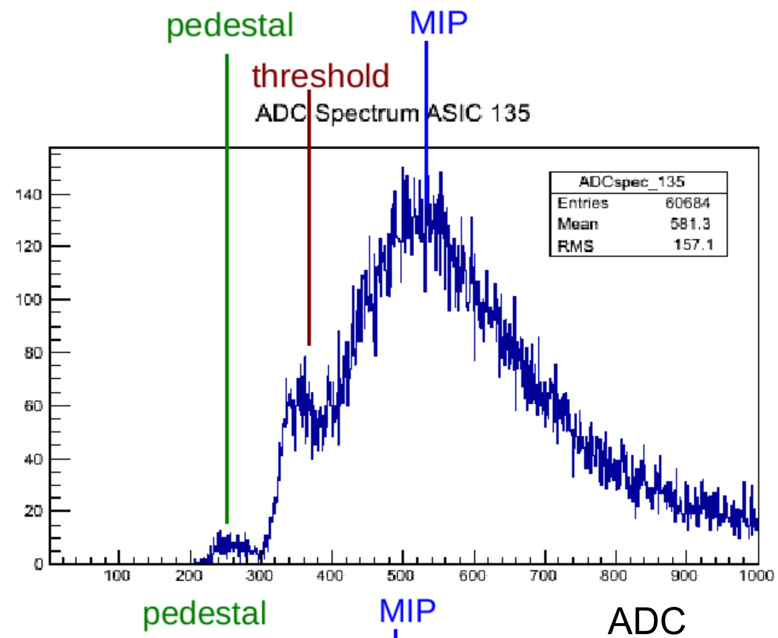
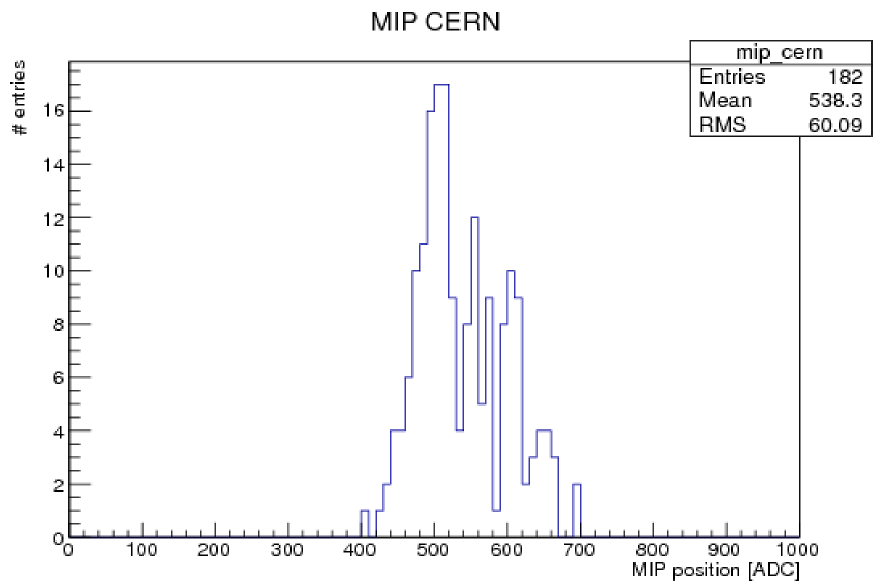
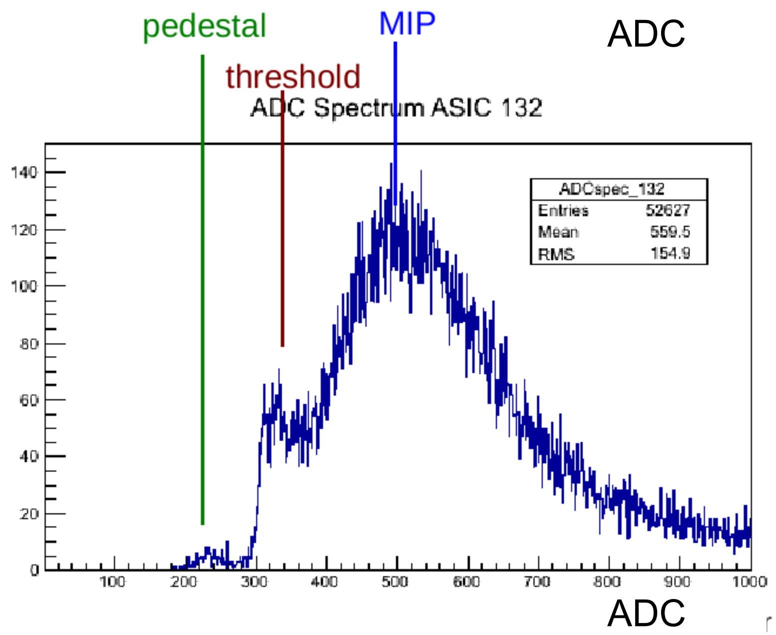
<u>Muon data</u>
cross-check of threshold calibration:

- Homogeneity of MIP positions
- Successful test for external validation:
  - ➔ Threshold < 0.5 MIP
  - ➔ Noise < 50 Hz/HBU (up to 700 Hz/HBU w/out validation)
  - ➔ Beam rate 1 – 50 Hz
- Noise peak due to inefficiency of external validation
  - ➔ Known feature of the readout chip
  - ➔ Fixed in following versions





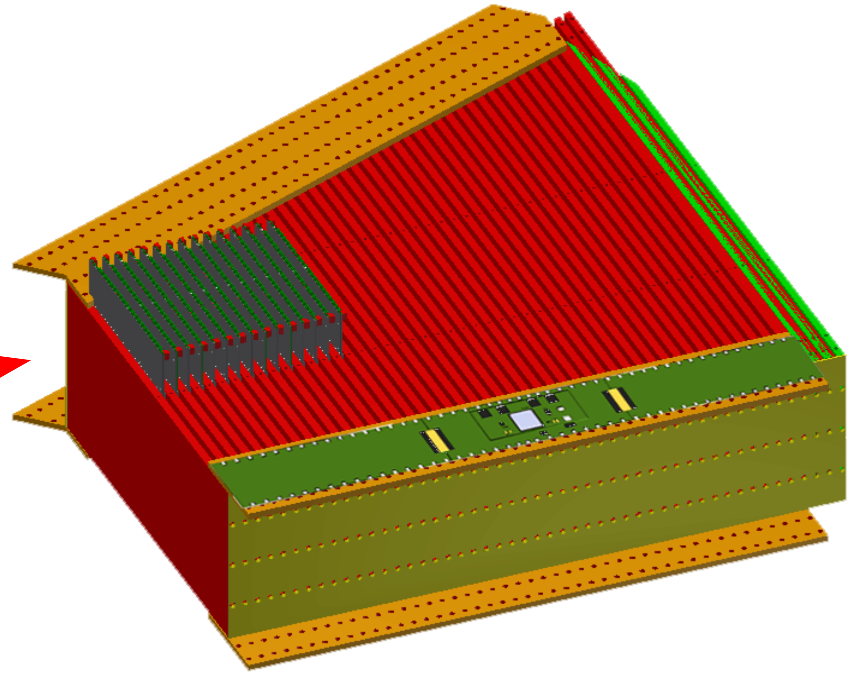


Upcoming test beam

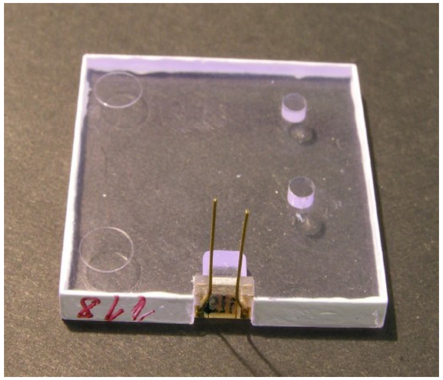
Next test beam:
- Two weeks in June 2013
- DESY electron beam line 22
- 2 – 6 GeV electrons

Multi-layer setup:
- Commissioning and test:
  - → New Front End electronics
  - → New DAQ
- New tile prototypes
  - → New solutions for simplification
  - → Mass production

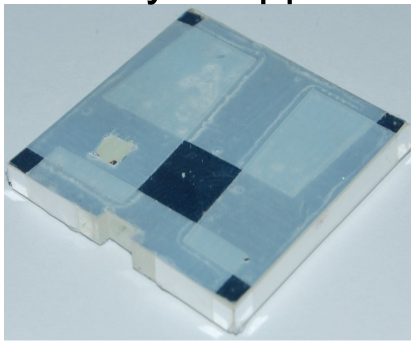
electron beam



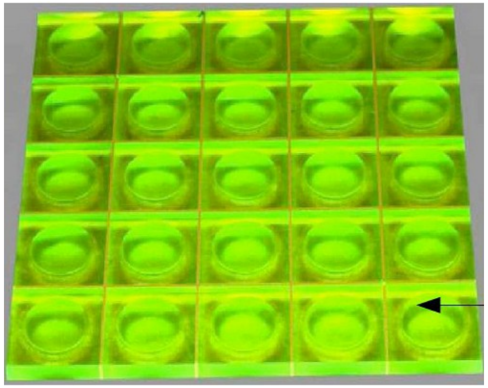
ITEP
w/out fiber



UniHH
fully wrapped



NIU “megatile”



Conclusions

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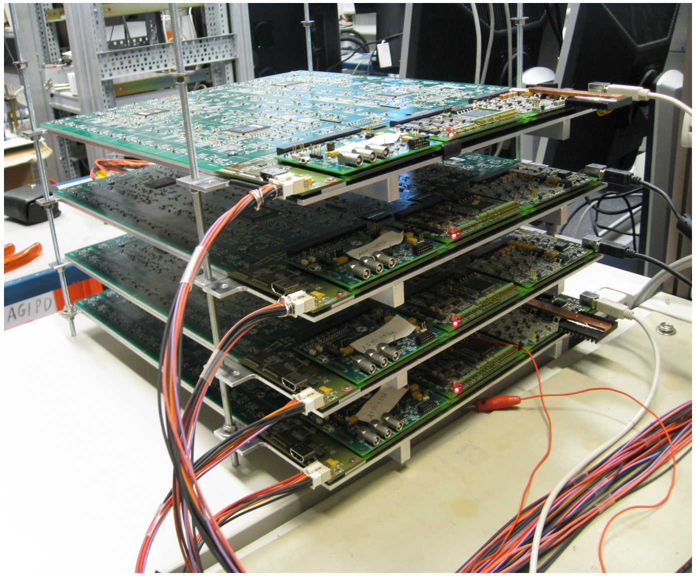
- One layer of new AHCAL prototype successfully commissioned:
  - Integrated readout electronics
  - Time stamping capabilities (main physics goal)
- Extensive calibration procedure
  - Full understanding of the electronics
- Hadronic test beam campaign at CERN SPS
  - Data analysis just starting

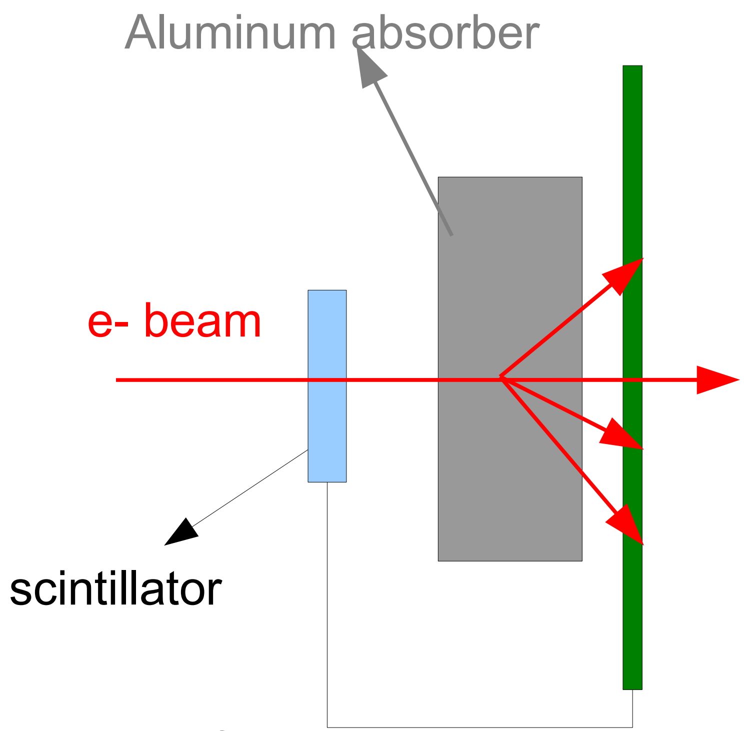


Outlook:

- Commissioning of a multi-layer prototype
  - Focus on DAQ development
- First test at DESY test beam in June 2013
- Total of 20 HBUs envisaged for 2014
  - Bring multi-layer prototype in hadronic test beam

Backup Slides

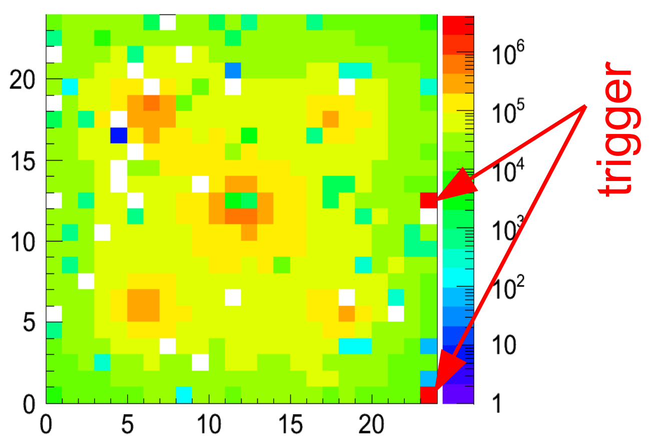
TDC calibration at DESY test beam

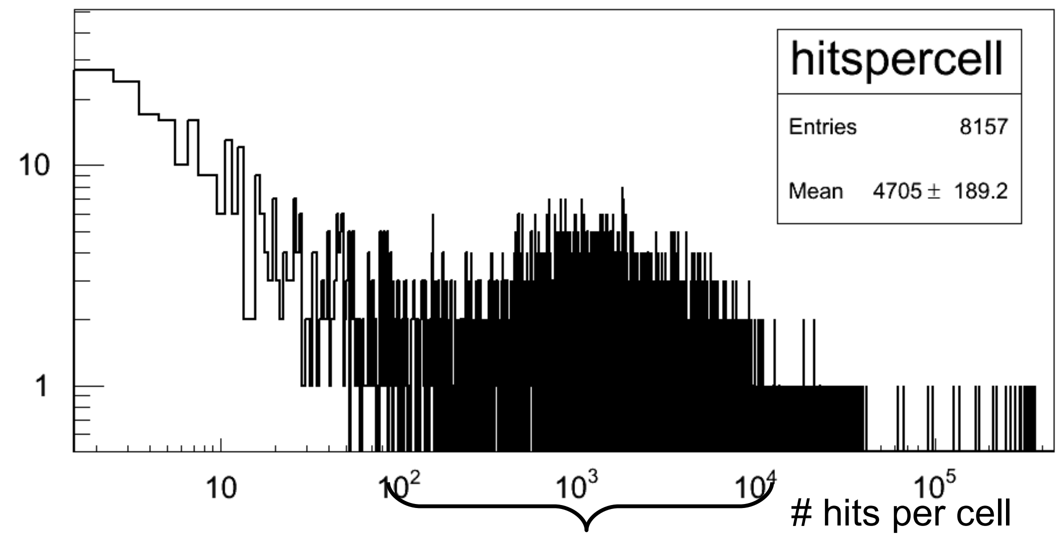


HBU in DESY electron test beam:

- Aluminum absorber (R_M ~ 4.4 cm)
- Wide, “instantaneous” EM showers
- Each shower hits several cells simultaneously
- Two channels replaced with external trigger from scintillator for absolute time reference
- chip clock not synchronous with the beam
- We cover the whole TDC ramp range

Hitmap of all the runs combined





89% of memory cells has at least 100 hits

TDC ramp accuracy

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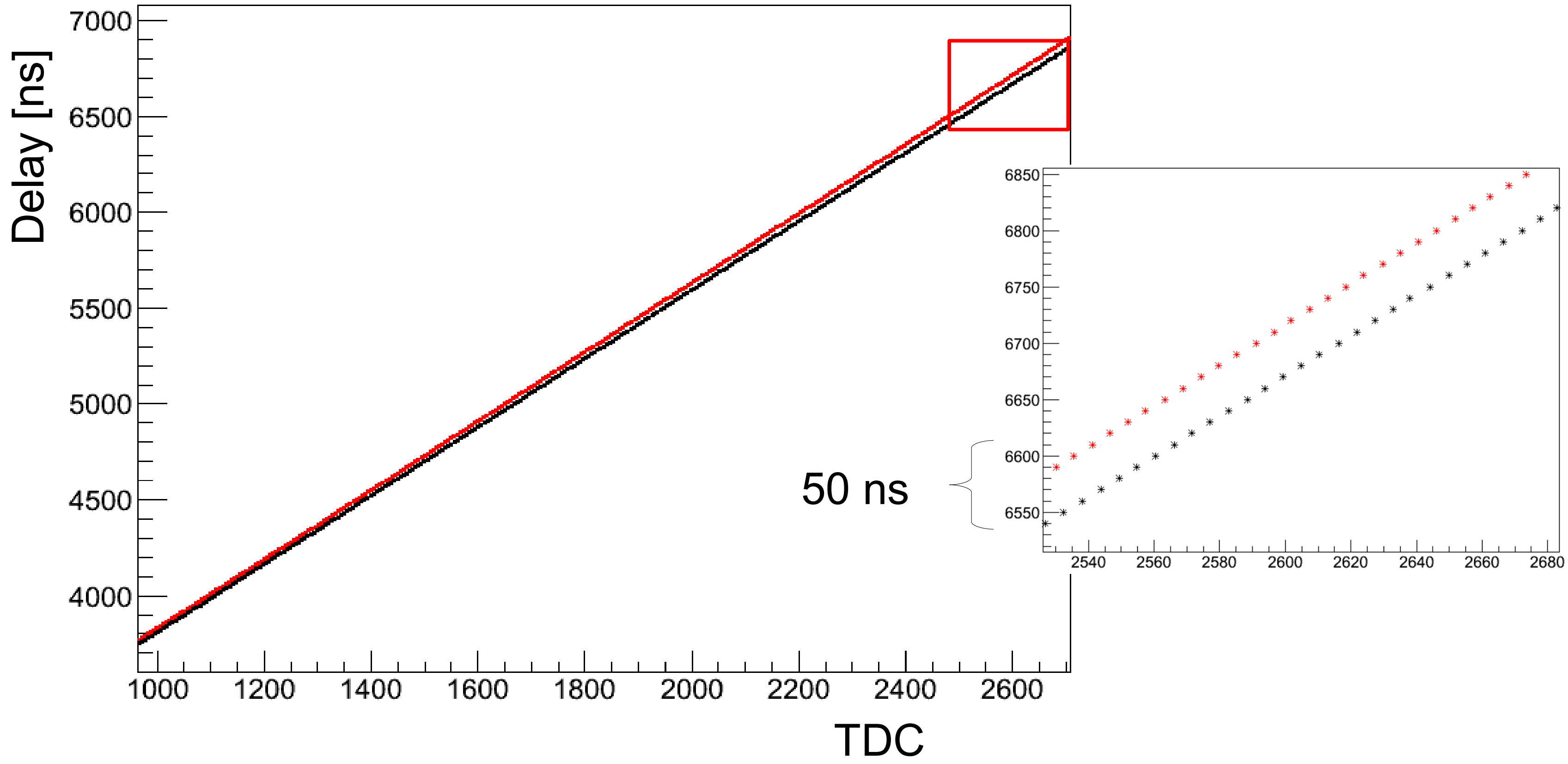
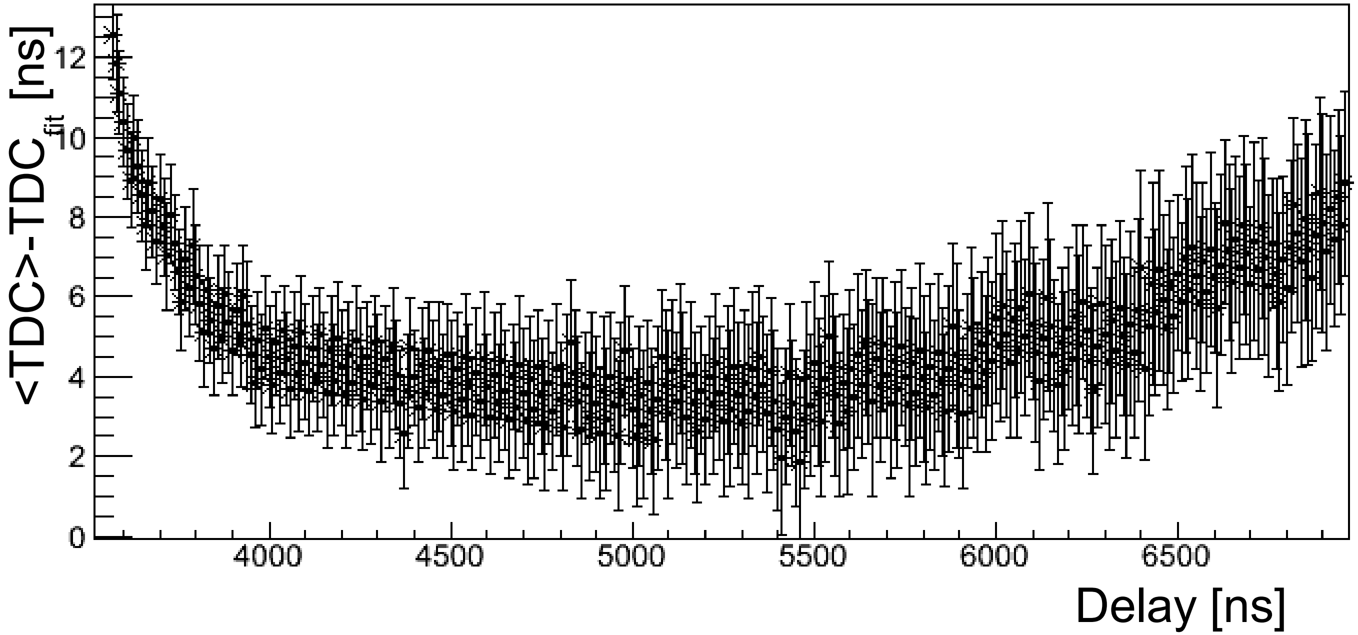


The two multiplexed ramps are not equal to a level of ~ 1%
Still not enough: deviation corresponds to a difference of tens of ns

TDC ramp linearity

Linear ramp approximation:

time [ns] = *slope* x TDC + *offset*



Linear approximation still not good enough:
Residuals up to 10 ns between real data and fit
Instead of fit function:
Look up table of data points for interpolation

New tile prototypes

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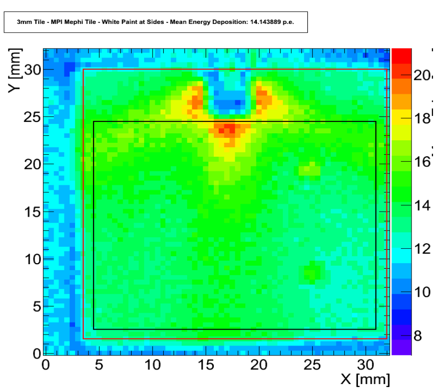
Reduce the spread in tile performances:

- Remove wavelength-shifting fiber
  - ➔ Use blue sensitive SiPM
- Enhance tile uniformity (Light Yield uniformity)
- Enhance SiPM performances uniformity
  - ➔ SiPM mass production
  - ➔ Ensure calibration portability

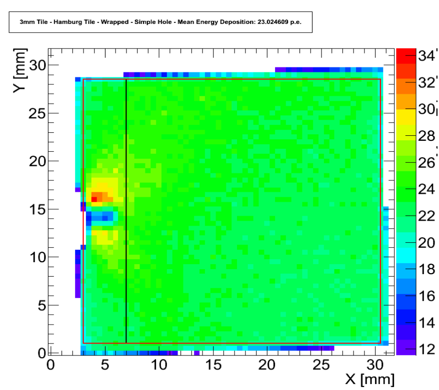
	CPTA	**Ketek**
Gain [e-]	0.7 x 10^6 to 2 x10^6	0.8 x10^6
PDE [%]	n.a.	30 (at λ= 420 nm)
DCR (at 0.5 p.e.)	1 Mcps	1 Mcps
Cross-talk [%]	~ 1%	10 %
Recovery [ns]	80	50
Breakdown [V]	28	26
dV_{BD}/dT [mV/K]	20	23
Area	1 mm x 1 mm	1.2 mm x 1.2 mm
N of pixels	798	2300

ITEP tile



[p.e.]

UniHH tile



[p.e.]

Light Yield scan (same SiPM as reference)

	ITEP	UniHH
Mean LY [p.e.]	14	23
10% deviation area	76 %	91 %