

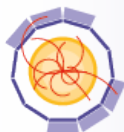


R&D for a highly granular SiW ECAL and analysis of beam test data

Thibault Frisson (LAL, Orsay)
on behalf of the CALICE collaboration



CALIIMAX-HEP
2010 BLANC
0429 01



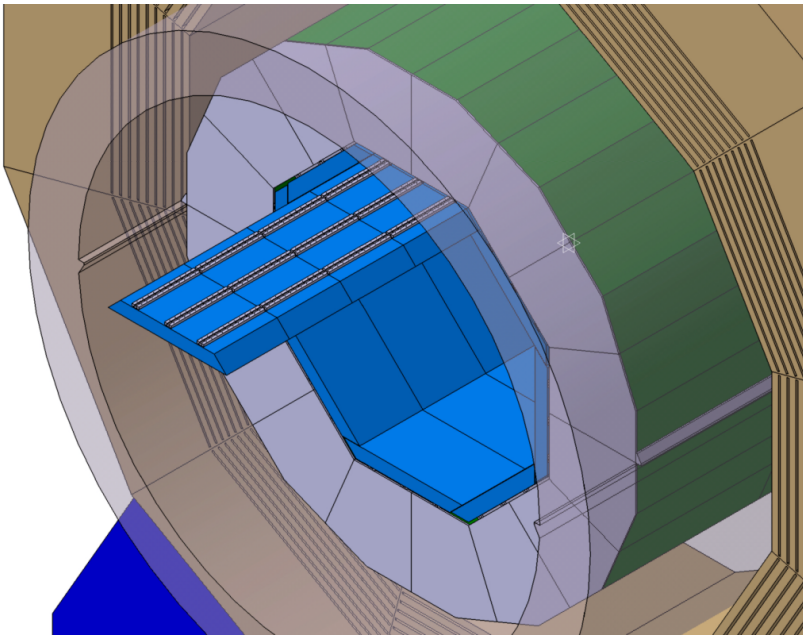
AIDA

Advanced European Infrastructures
for Detectors at Accelerators

SiW ECAL for a future LC detector

SiW ECAL is one of the proposal for future LC detectors

➔ Optimized for Particle Flow Algorithm



The SiW ECAL in the ILD Detector
(presented by Daniel Jeans)

Basic Requirements:

- Extreme high granularity
- Compact and hermetic

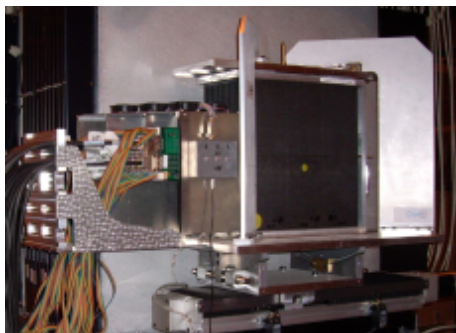
Basic Choices:

- Tungsten as absorber material
 - $X_0=3.5\text{mm}$, $R_M=9\text{mm}$, $\lambda_I=96\text{mm}$
 - Narrow showers
 - Assures compact design
- Silicon as active material
 - Support compact design
 - Allows for pixelisation
 - Large signal/noise ratio

Physics Prototype

Proof of principle

2003 - 2011



JINST 3, 2008

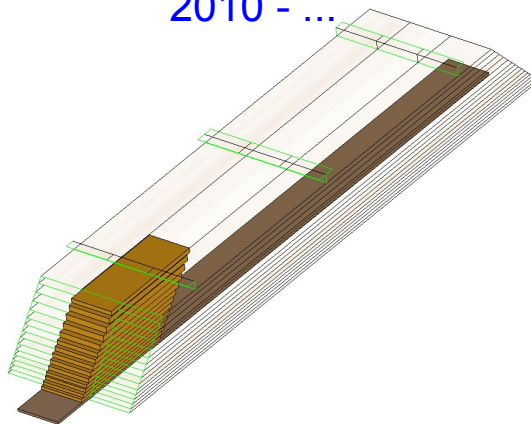
Number of channels : **9720**

Weight : **~ 200 Kg**

Technological Prototype

Engineering challenges

2010 - ...

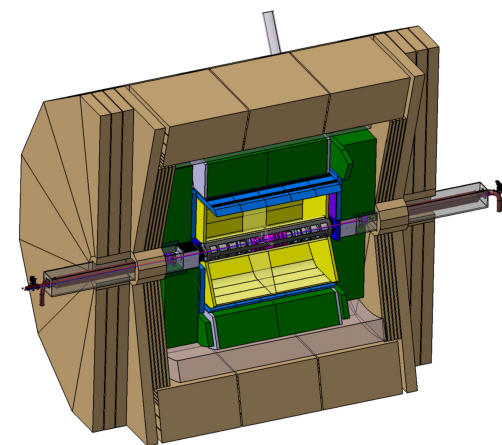


TDR EUDET-Report-2009-01

Number of channels : **45360**

Weight : **~ 700 Kg**

LC detector



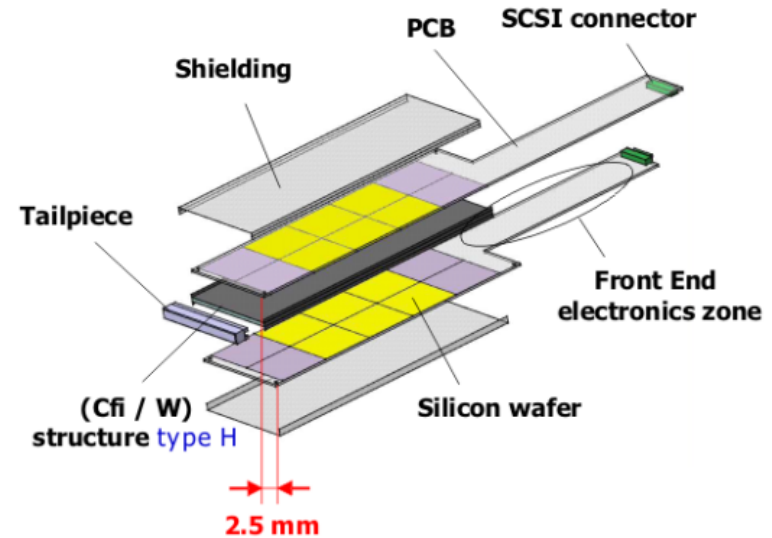
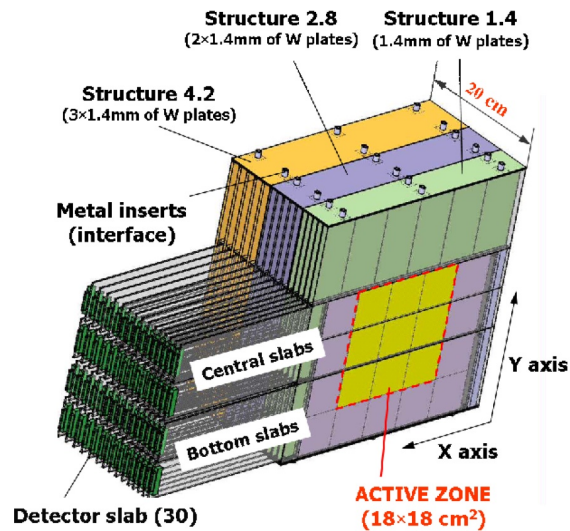
DBD for ILC
CDR for CLIC

ECAL :

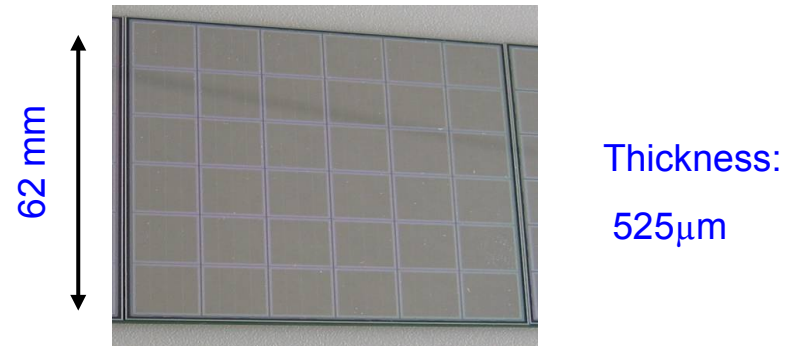
Channels : **~ 100 10⁶**

Total Weight : **~ 130 t**

Physics prototype



6x6 PIN Diode Matrix – **1 x 1 cm²**



Carbon-fibre mechanical structure

30 layers of tungsten: 24 X_0 , 1 λ_1

10k channels

S/N ~ 8

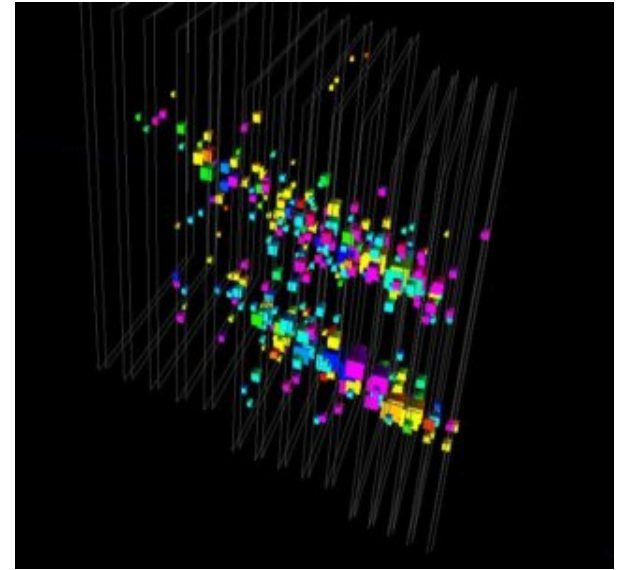
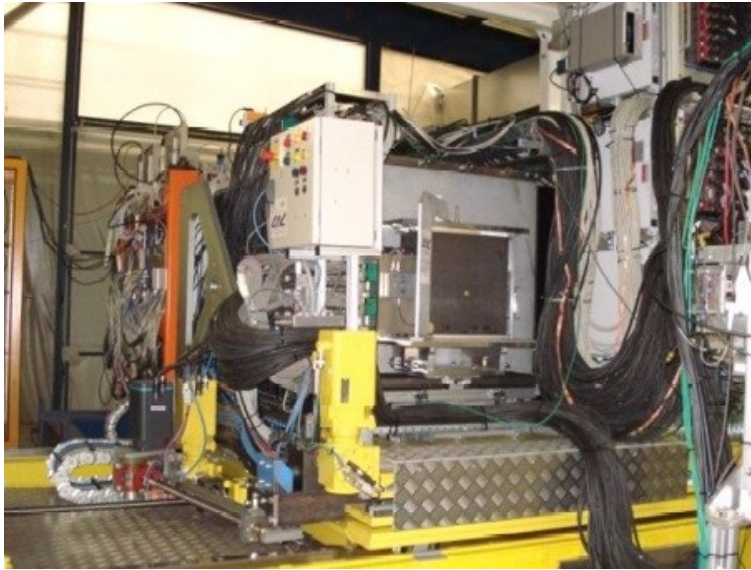
$$\sigma_E / E = 16.5 / \sqrt{E(\text{GeV})} + 1.1 \%$$

Resistivity: 5kΩcm
80 (pairs e/hole)/μm

Beam tests

2006-2011: DESY, CERN, FNAL

e^- , π , μ , p (1 - 180 GeV)



Proof of principle for high granularity calorimeter

Improve our understanding of the detector prototype

- noise, calibration, performances
- validation of simulations

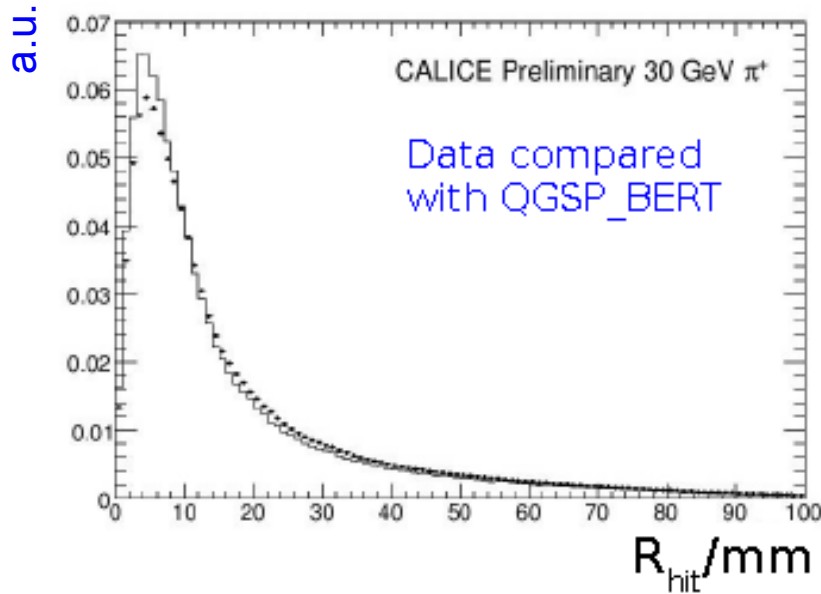
} Development of methods, algorithms...

Unprecedented granularity

- detailed testing of G4 simulations
- better understanding of hadronic interactions

Hadronic shower profiles

Major study for PFA: affects overlap of showers

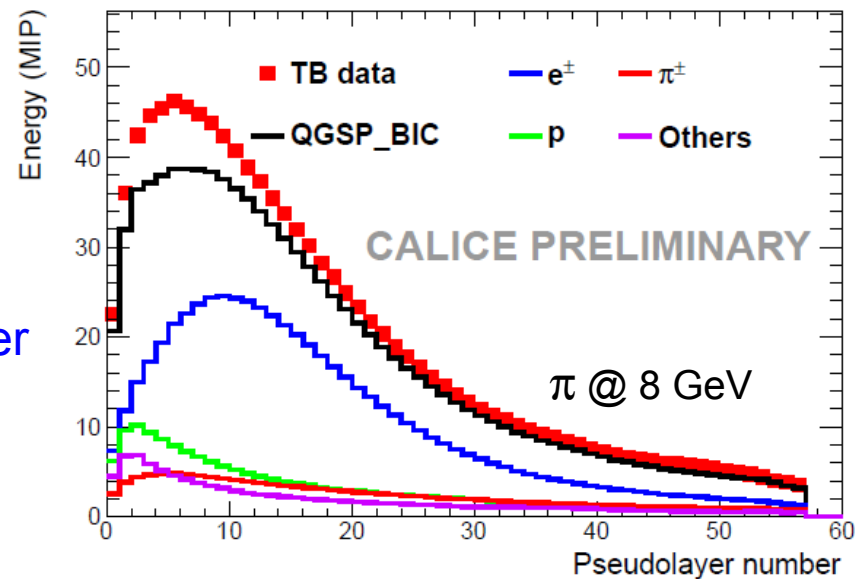


high transverse and longitudinal granularity
→ unprecedented details of the showers

Not easy to select a model (depends on observable, energy...)
...but relatively small difference between models (~20%)

Small X_0/λ_1

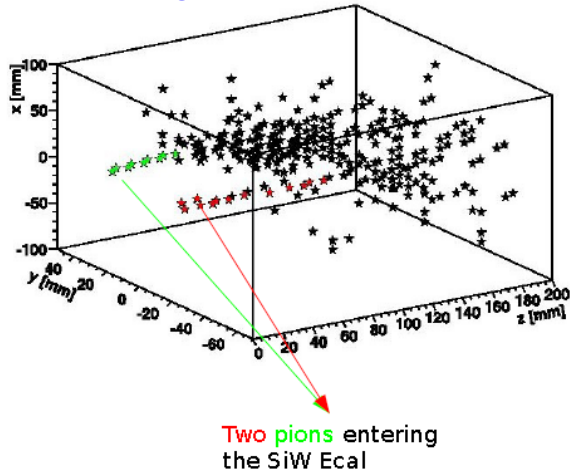
→ study the components of the shower



Imaging interactions

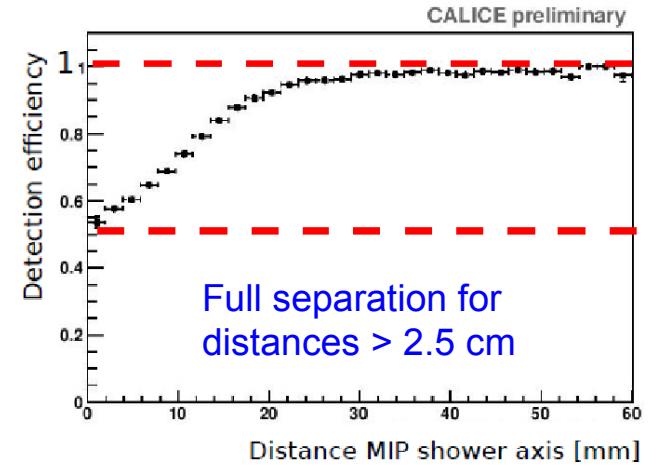
High granularity allows particle tracking through detector

Imaging processing techniques
(Hough transformation)

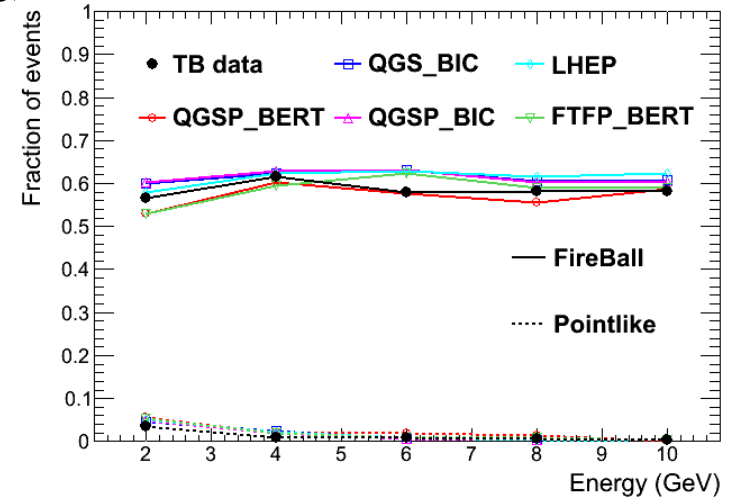
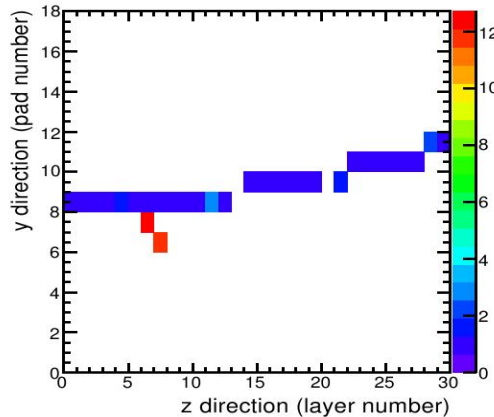
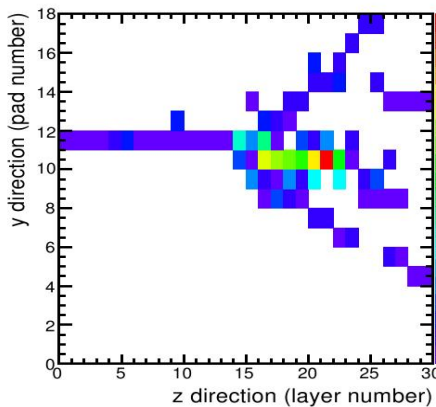


Essential for PFA
(especially for
neutral / charged
particle separation)

Efficiency to separate
MIP - electron



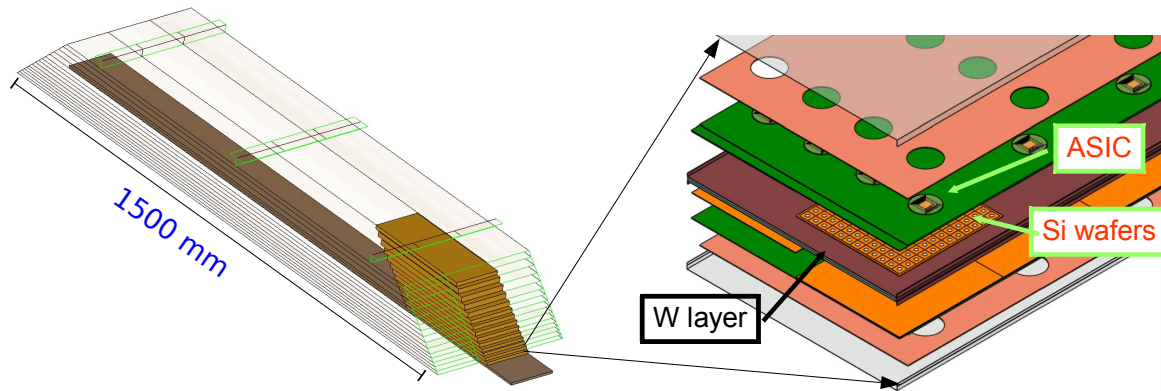
High granularity permits detailed view into hadronic shower



Technological prototype

Technological solutions for the final detector

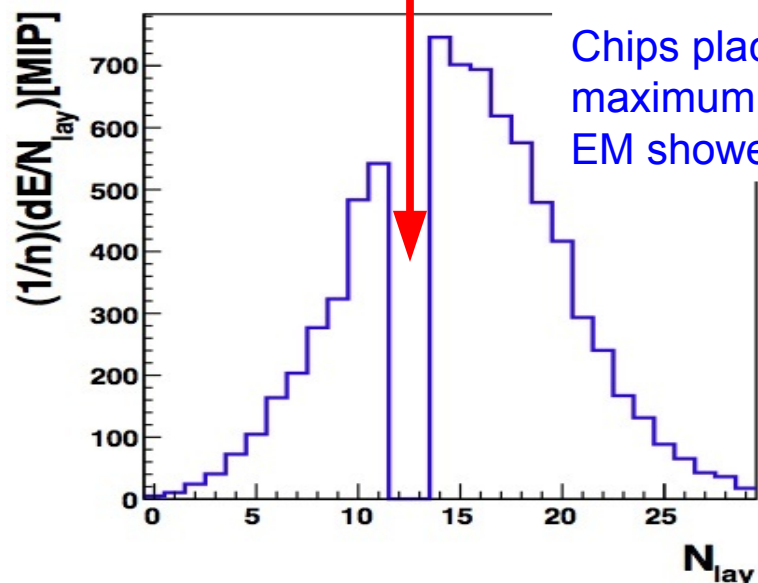
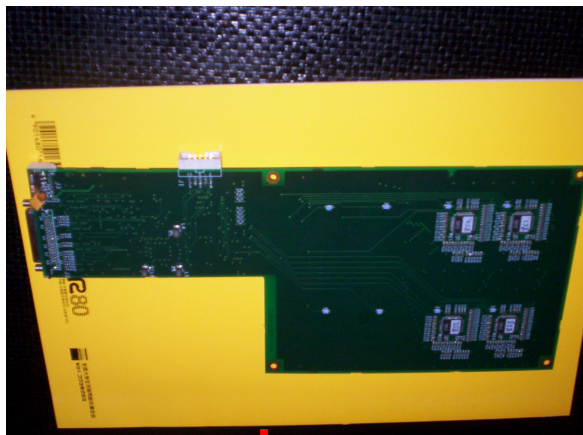
Construction start: 2010



- Realistic dimensions (3/5 of a barrel module of the ILD concept)
- Integrated front end electronic
- Small power consumption (Power pulsed electronics)

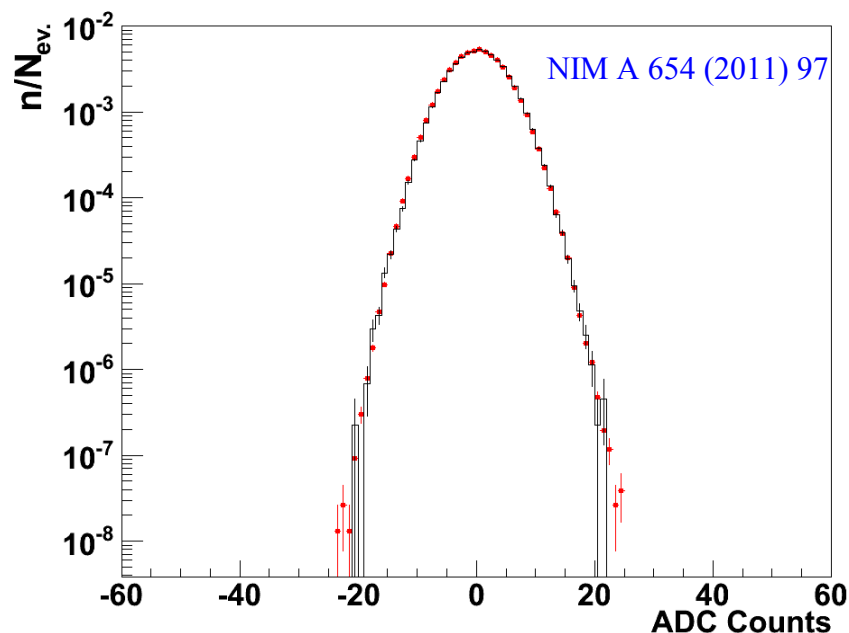
Embedded electronics - Parasitic effects?

Exposure of front end electronics to electromagnetic showers



Chips placed in shower maximum of 70-90 GeV EM showers

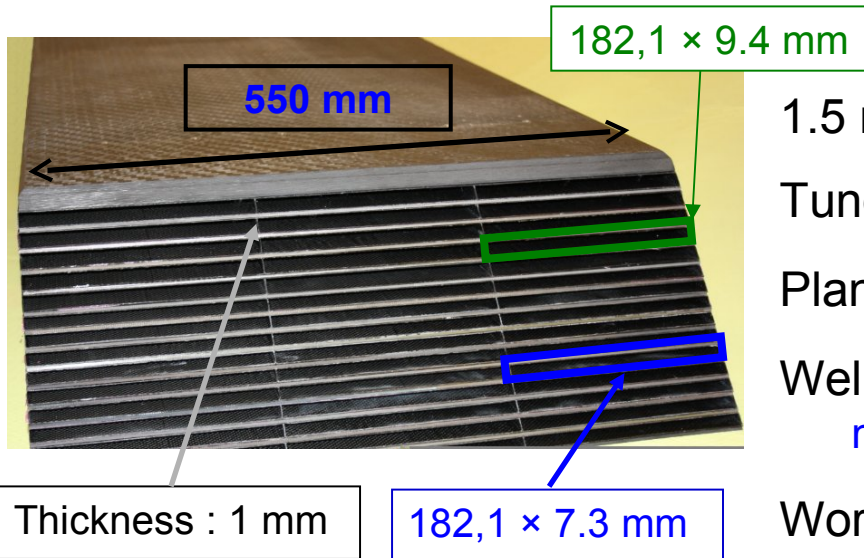
Comparison: Beam events
(Interleaved) Pedestal events



- No sizable influence on noise spectra by beam exposure
 $\Delta\text{Mean} < 0.01\%$ of MIP $\Delta\text{RMS} < 0.01\%$ of MIP
- No hit above 1 MIP observed
=> Upper Limit on rate of faked MIPs: $\sim 7 \times 10^{-7}$

Possible Effects: Transient effects
Single event upsets

Mechanical structure



1.5 m long alveolar structure to house ECAL layers

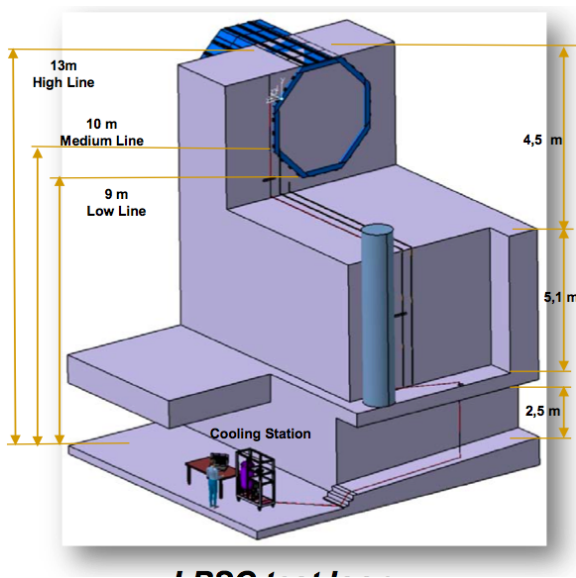
Tungsten plates wrapped into Prepreg

Planar within 5 mm

Well understood

mechanical constraints, thermal behavior

Work on longer structures are ongoing



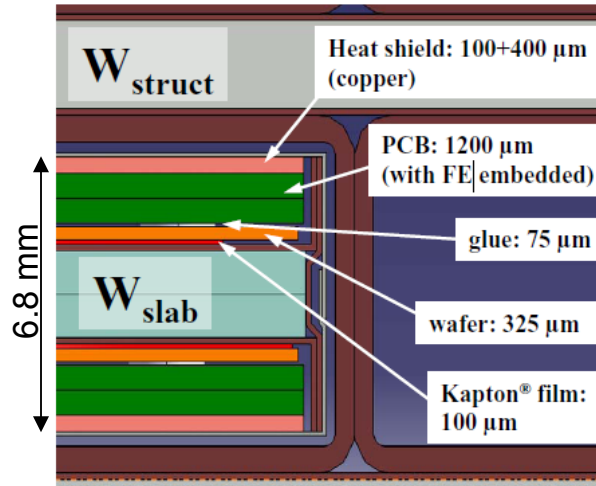
Evacuation of (residual) power of 0.2-0.35 W / layer

Development of a leak less cooling system for a full detector

ECAL layer

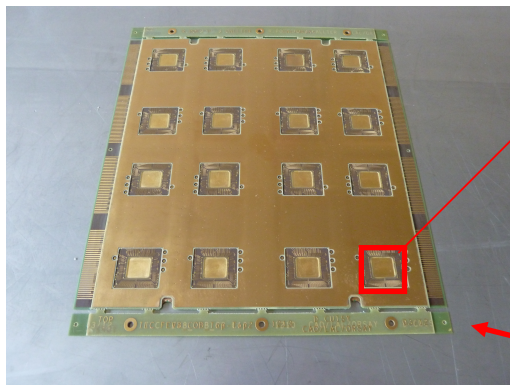
1 Active Sensor Units (ASU)

- 1 kapton (HV for PIN diodes)
- 1 layer PIN diodes
- 1 PCB with microchips embedded
- 1 thermal drain (copper)

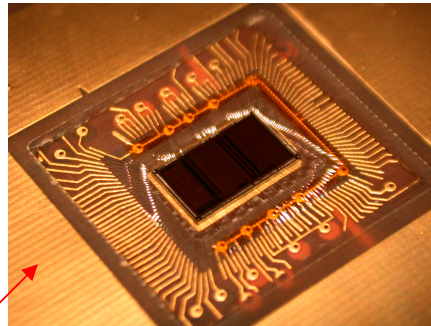


W thickness:

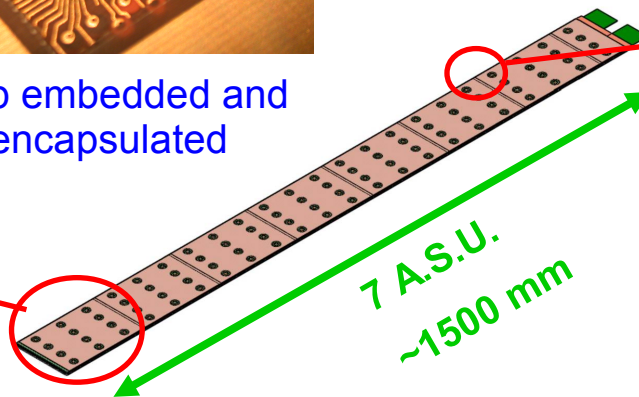
- 2.1 mm (20 layers)
- 4.2 mm (9 layers)



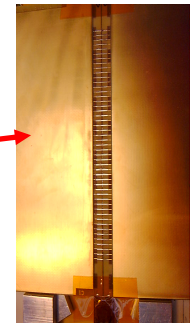
PCB prototype



Chip embedded and encapsulated



Interconnection studies

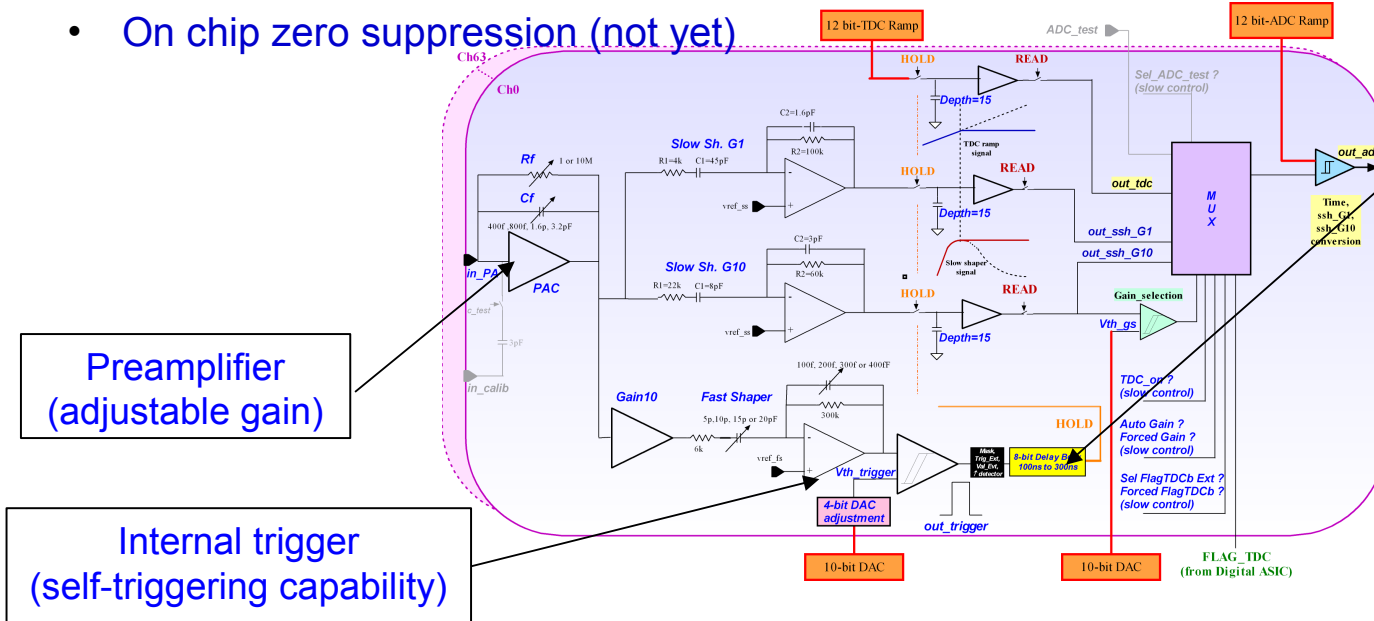
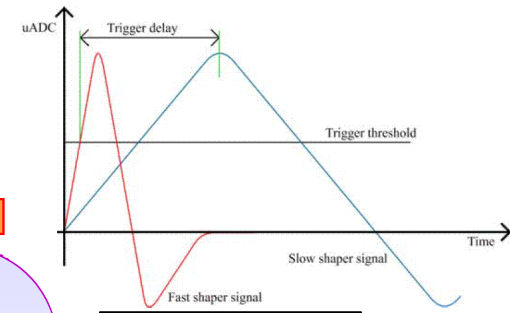
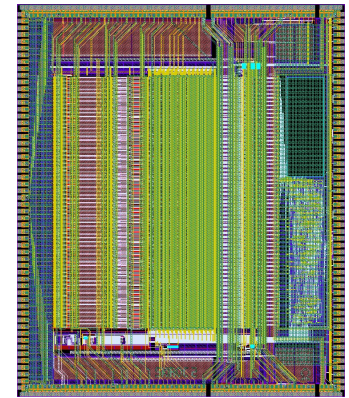


Front end electronics: SKIROC

See Nathalie's talk

SKIROC (Silicon Kalorimeter Integrated Read Out Chip)

- SiGe 0.35 μ m AMS
- 7.5 mm x 8.7 mm
- High integration level (variable gain charge amp, 12-bit ADC, digital logic)
- 64 channels
- Large dynamic range (~2500 MIPS), low noise (0.4 fC – 10 pC)
- Auto-trigger at 1/2 MIP
- Low Power: 25 μ W/ch (power pulsing)
- On chip zero suppression (not yet)



Preamplifier (adjustable gain)

Internal trigger (self-triggering capability)

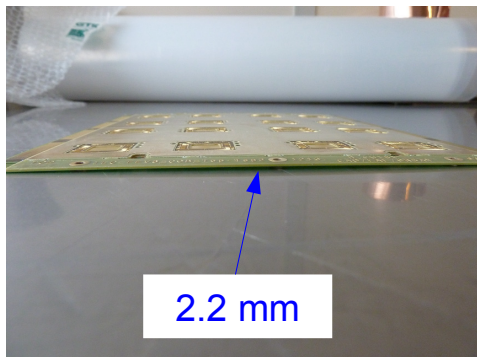
Trigger delay

PCB – Embedded electronics

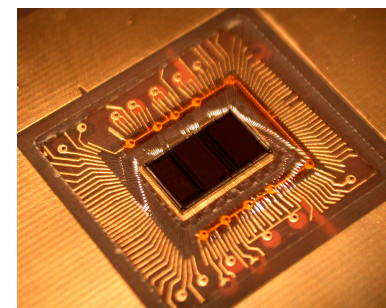
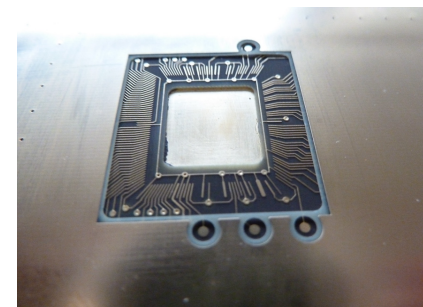
PCB prototype for embedding the chips: aggressive design

1.2 mm height for a board of 18 x 18 cm² and 9 layers

Deviation from total flatness max: 0.5 mm



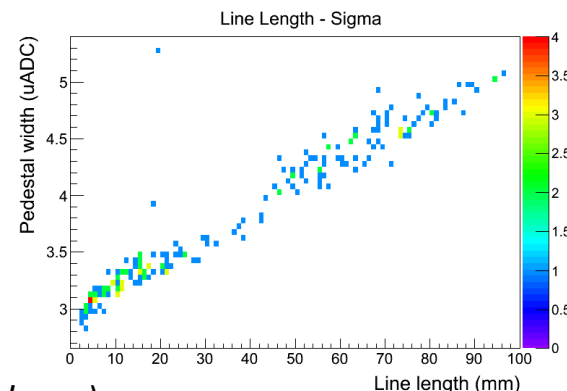
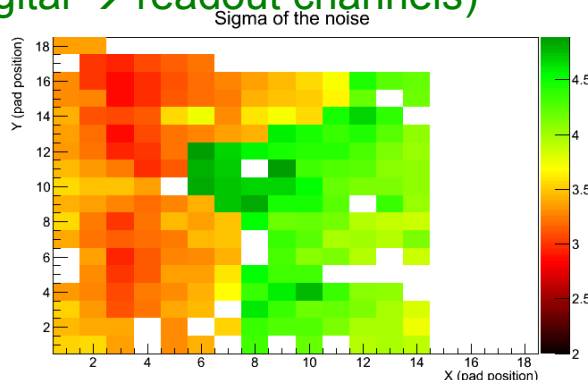
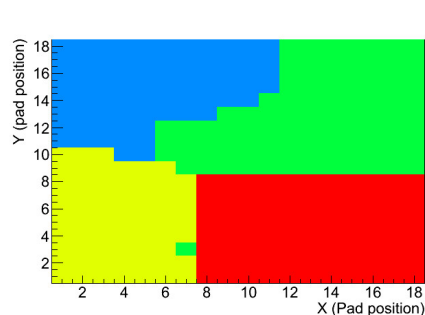
- First board for 16 ASICs (4 wafers) available
- Now equipped with 8 SKIROC ASICs (Bonding by CERN)
 - Needs testing (Bonding was not straightforward, thin bonding pads to be improved)



Line density in PCB → routing is crucial

Critical points are :

- Noise \propto line length
- Cross talk (Digital → readout channels)

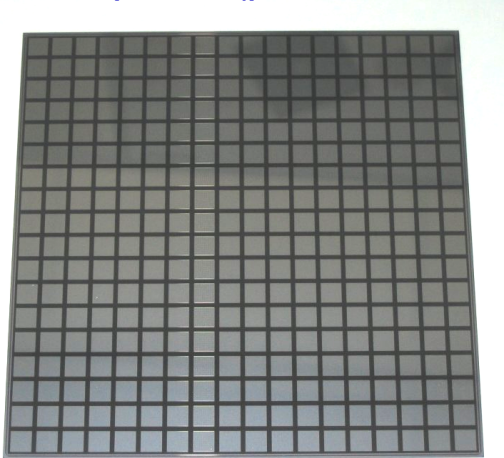


Results with conservative design (chip in package)

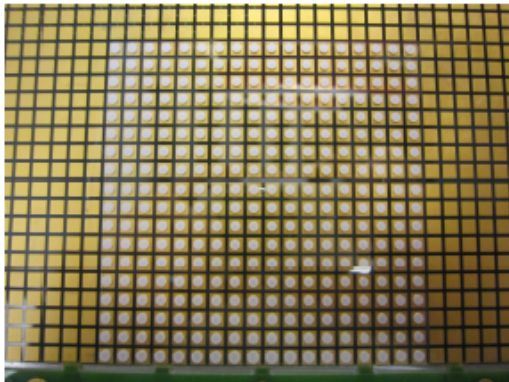
Silicon wafers

Si wafer (HPK):

- $9 \times 9 \text{ cm}^2$
- Thickness = $320 \text{ }\mu\text{m}$
- 324 pixels (pixel size = $5 \times 5 \text{ mm}^2$) → lateral granularity = 4 x better than physics prototype



Gluing onto PCB and development of automatised procedure



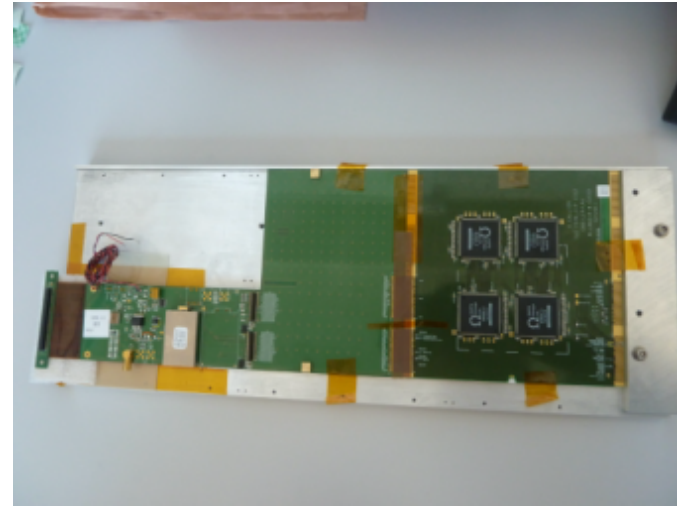
- Optimization studies on guard rings and characterization.
- Guard ring around the wafer to control the leakage currents
- Different technologies are tested

The road to the technological prototype

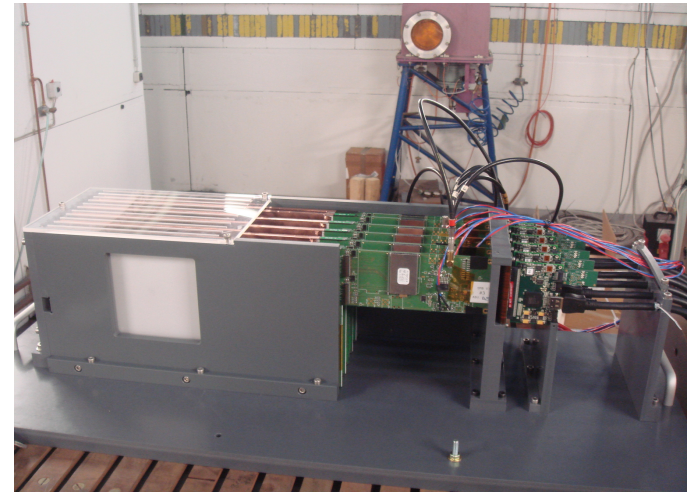
Intermediate step: **Conservative layer design for beam tests**

- First test in beam
- Benchmark to go further

Test beam @ DESY : e- (1 - 5 GeV)

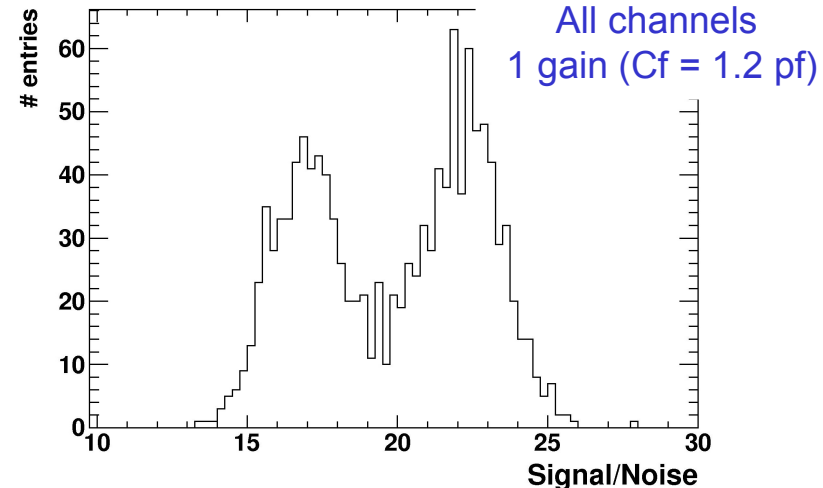
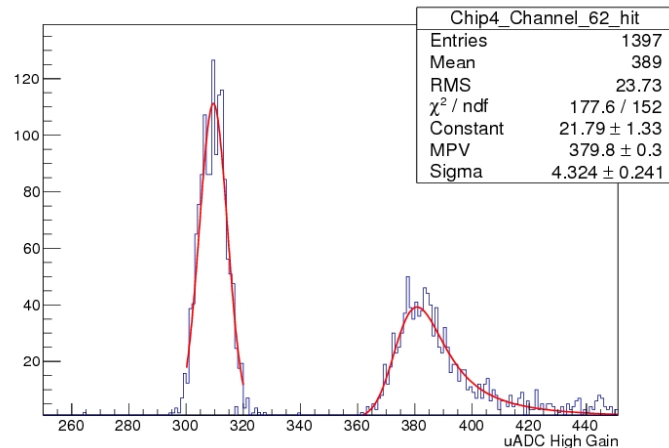
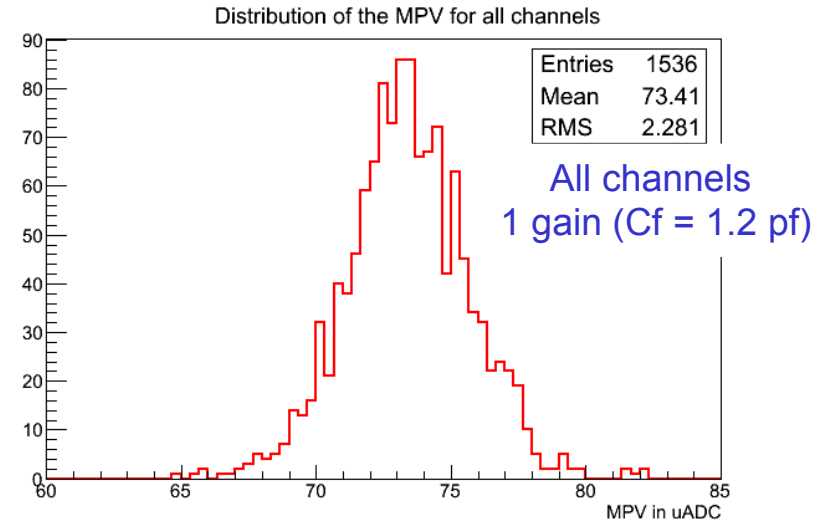
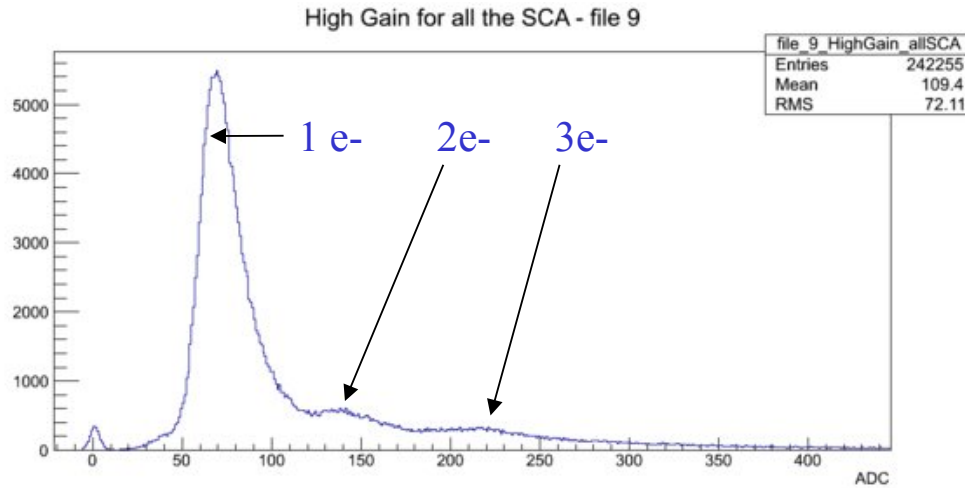


- Single detection layer
- 4 ASICs per slab (1/4 final design) – conservative design (chip in package)
 - 4 SKIROCs x 64 channels = 256 channels/slab
- 6 layers (July 2012) → 1536 channels
- 8 layers (February 2013) → 2048 channels
 - 4 layers in power pulsing



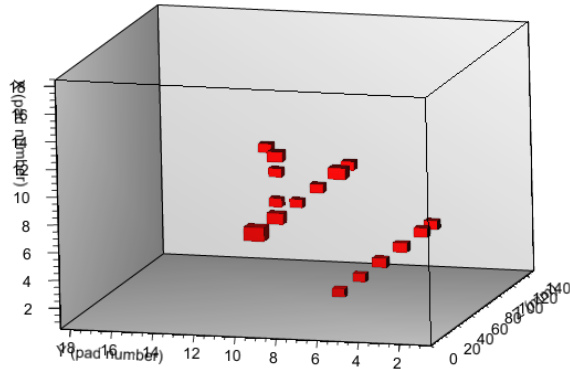
Selection of results

Complete understanding of electronics → Filtering of non-physic events
Establishment of calibration procedure for a larger number of cells
Homogeneity of response (x,y scan of detector)

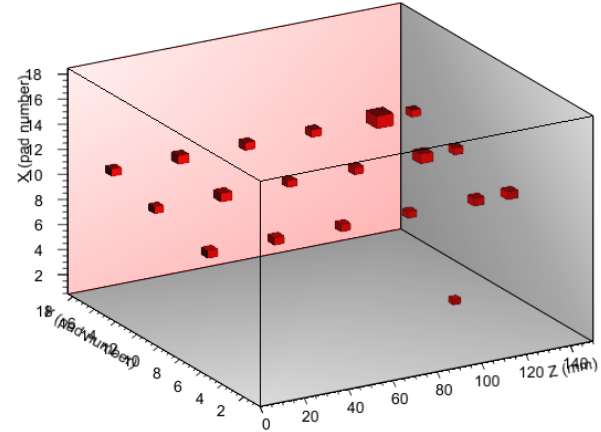


Event display

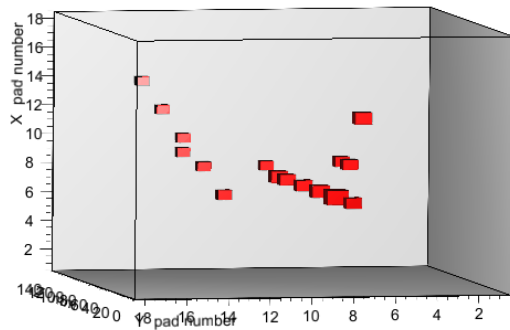
2 e- (3 GeV, no tungsten)



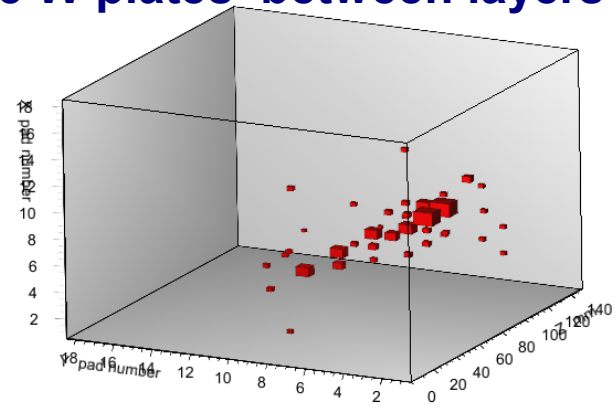
3 e- (3 GeV, no tungsten)



1 cosmic + 1 e- (3 GeV, no tungsten)



**1 e- (5 GeV)
5 W plates between layers**



R&D in progress... first test beams show promising results

Summary and outlook

Successful R&D for a highly granular SiW ECAL physics prototype

Operated over several years

Exposed to several particle beam types and energies

Capacity of separating particles impressively demonstrated

The R&D for technological prototype is ongoing

A lot of work on different aspects to prove the engineering feasibility of the project

- long layers
- power consumption (power pulsing) → critical point
- ...

First test beams with conservative design:

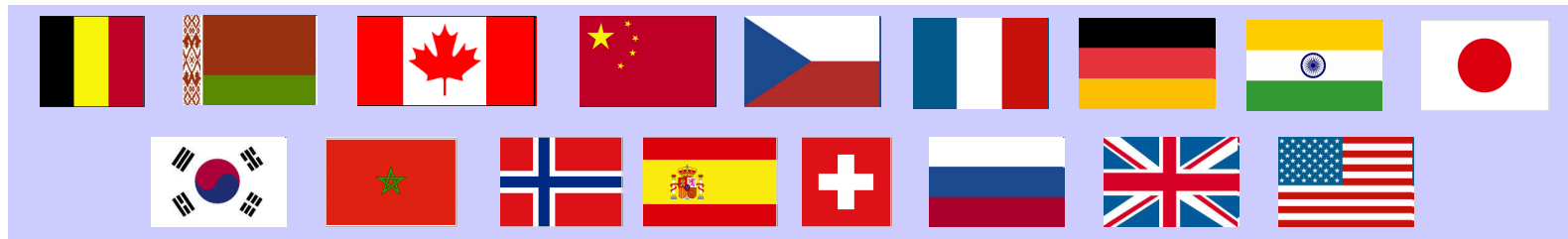
- encouraging results
- identification of open issues

Analysis of power pulsing data is on-going (February 2013 test beam)



Back up

The CALICE collaboration



+300 people, +50 institutes, 17 countries

R&D detector for futur linear e⁺/e⁻ collider

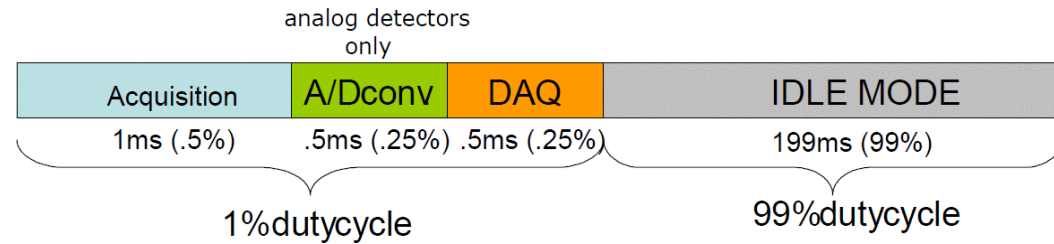
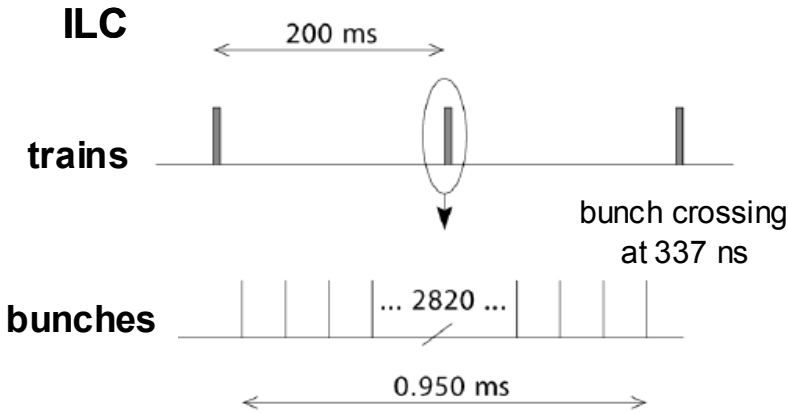
(ECAL, HCAL, muon detectors, tail catchers...)

→ Common approach:

Ultra-granular "imaging" calorimetry → particle flow algorithm

- Physics Prototypes
 - Small prototypes. Proof of principle of technologies.
- Technological prototypes
 - Testing more realistic hardware designs which could be scaled up to full detector
- Combined beam tests
 - Reconstruction algorithms
 - Validate MC simulations

Power pulsing



Long idle time between trains:

- Power intensive fast analog only for <1% of the time
- Long breaks for data handling

Power Pulsing

0 to 10 Amps pulses of 1 ms at 5 Hz

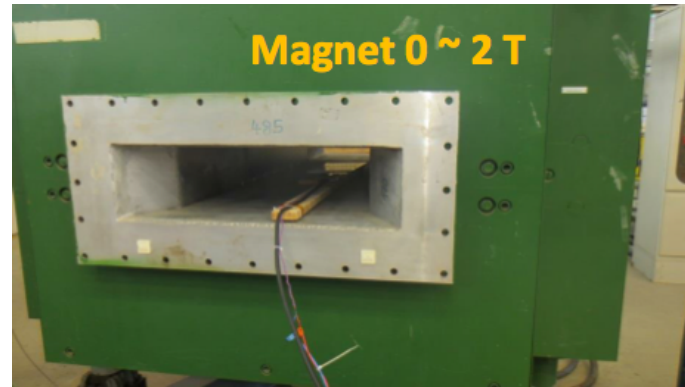
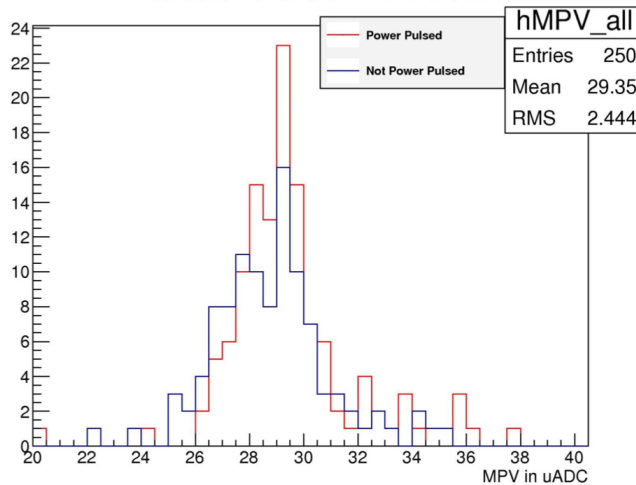
Power pulsing (it may be included in the talk)

Power pulsing (PP): duty cycle 99% , 10Hz

Operation in power pulsing mode requires removal of decoupling capacitances
→ Do not expect as stable performance as in continuous mode

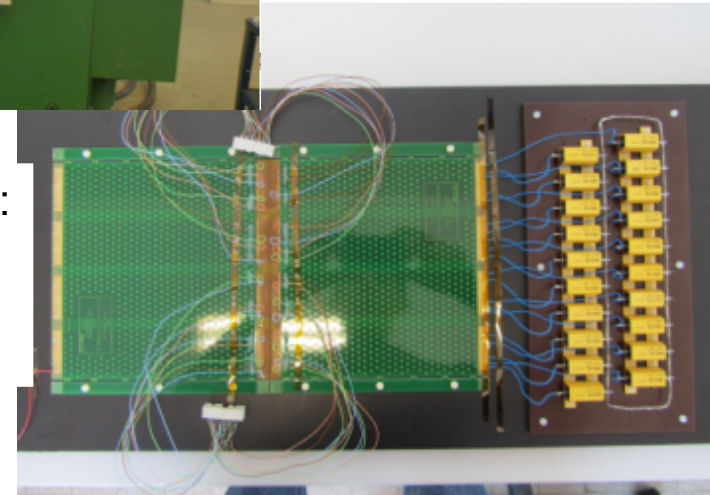
Tests in magnetic field

Tests in beam



Measurement of the pedestal in 1 layer

Interconnection (2 ASUs):
Measurement of the ohmic resistance



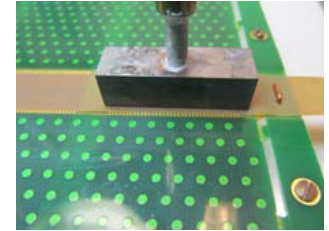
MPV of the landau distribution
Comparison PP - No PP (same layer)


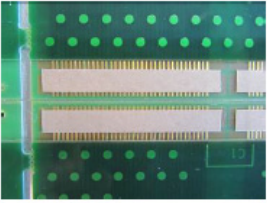

Ongoing analysis but first results are encouraging

Interconnexions

Up to 9 equipped PCBs interconnected to make detector slab

→ Electrical and mechanical connection made thanks to Kapton connecting cable



Technology	Advantages	Disadvantages
N°1 Solder 	<ul style="list-style-type: none"> -Proven technology -Possible to repair -~3 euros/connector 	<ul style="list-style-type: none"> -Difficult procedure -Too much heat for the glue of wafers -Cannot be industrialized
N°2 ACF 	<ul style="list-style-type: none"> -Easy to install -Easy to remove -Easy to industrialize 	<ul style="list-style-type: none"> -Needs to have a perfect planarity -Needs to have a thermode ~15Keuros -10mA maximum per wire -~30 euros/connector -Too much pressure =mechanical stress for the wafers
N°3 Spécial Kapton 	<ul style="list-style-type: none"> -Easy to install -Good reliability -Possible to repair -Easy to industrialize -Good strength -~4 euros/connector 	<ul style="list-style-type: none"> -I don't know yet



Max 600N before destruction



Signal integrity → In progress

Filtering

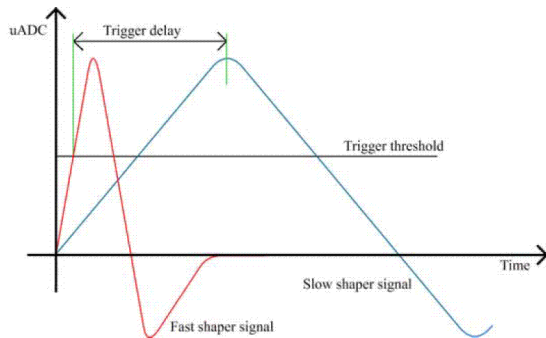
- **Ricochet / BCID+1 effect (without hit)**
 - Seen with SKIROC2 test bench and in TB
 - Understood
 - Easy to cut in TB analysis (cut event if $\Delta \text{BCID} == 1$)
- **Plane events**
 - Instabilities of power supply level \rightarrow fake events
 - power supply common to the 4 ASIC, Self-sustained \rightarrow sometimes filled all the 15 ASIC memories, Highly dependant of the number of ASIC with hits, dependant of the number of triggered channels
 - Cut in TB analysis:
 - $\Delta \text{BCID} \leq 5$
- **Isolated hits**
 - Reconstruction needed to see this effect (not yet well studied: noise, cosmic, related to plane events?)
 - Cut in TB analysis:
 - we ask at least 3 planes with hits in the same event (after reconstruction)

Calibration of ASICs

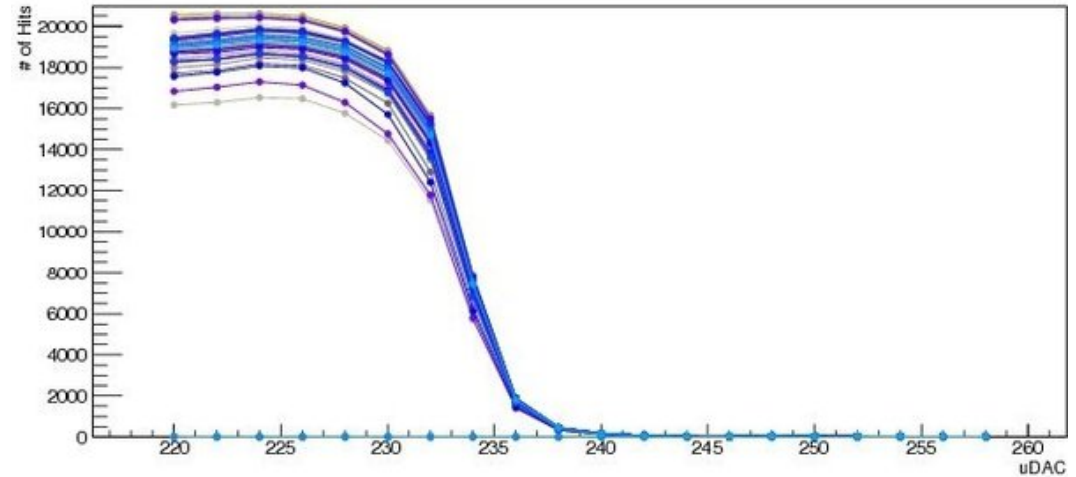
Establishment of calibration procedure for a larger number of cells

Trigger threshold
- depends on the gain

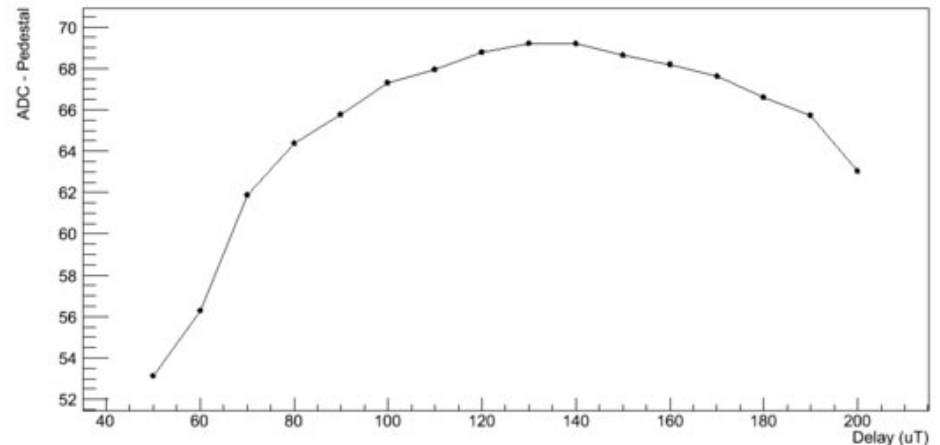
Trigger delay
- depends on the trigger threshold



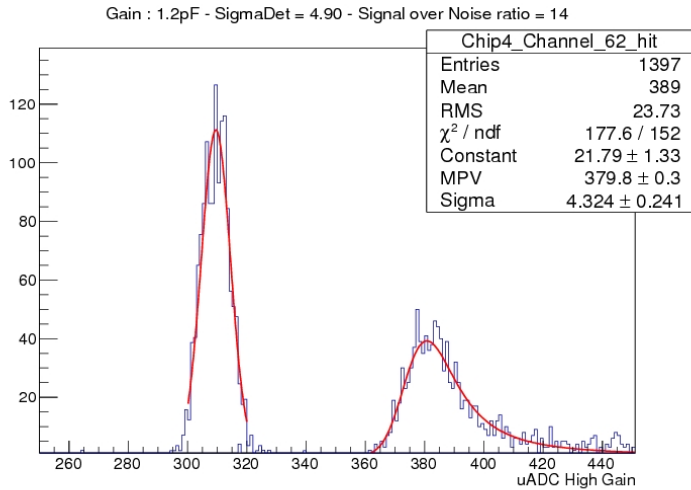
S-Curves for all the channels



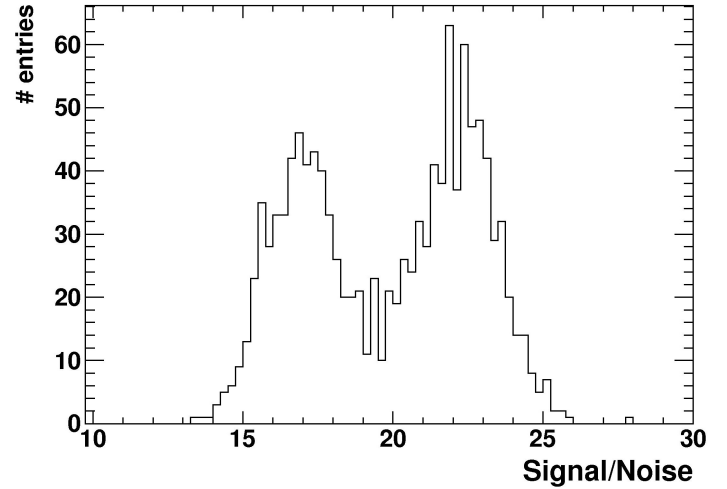
Holdscan - All SCA - Pedestal corrected



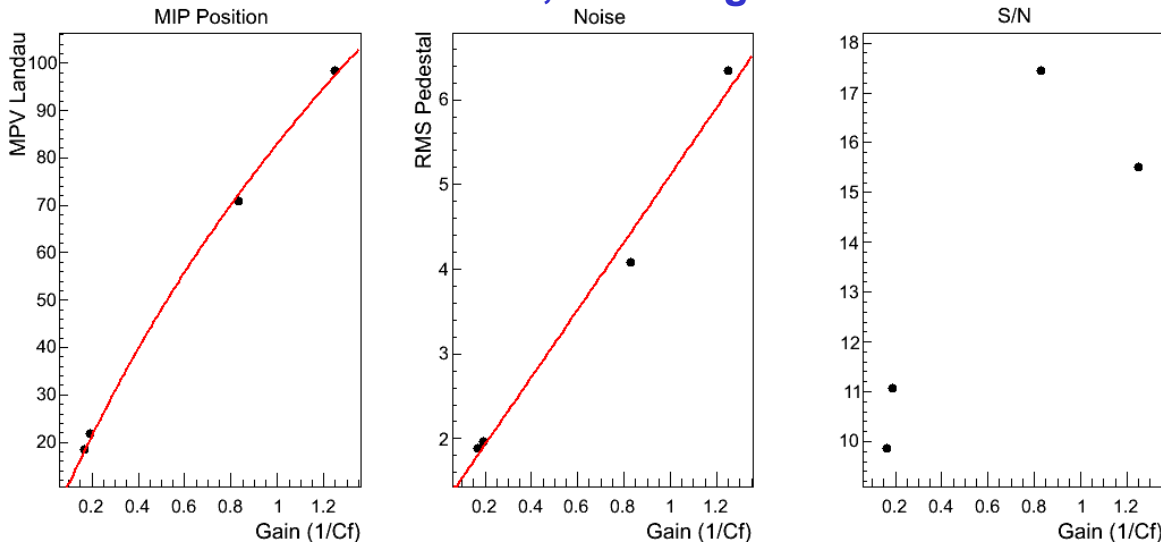
Signal over noise ratio



All channels, 1 gain (Cf = 1.2 pf)



1 channel, several gains



R&D target is 10:1

S/N ≥ 10
(for all gains available with SKIROC2)