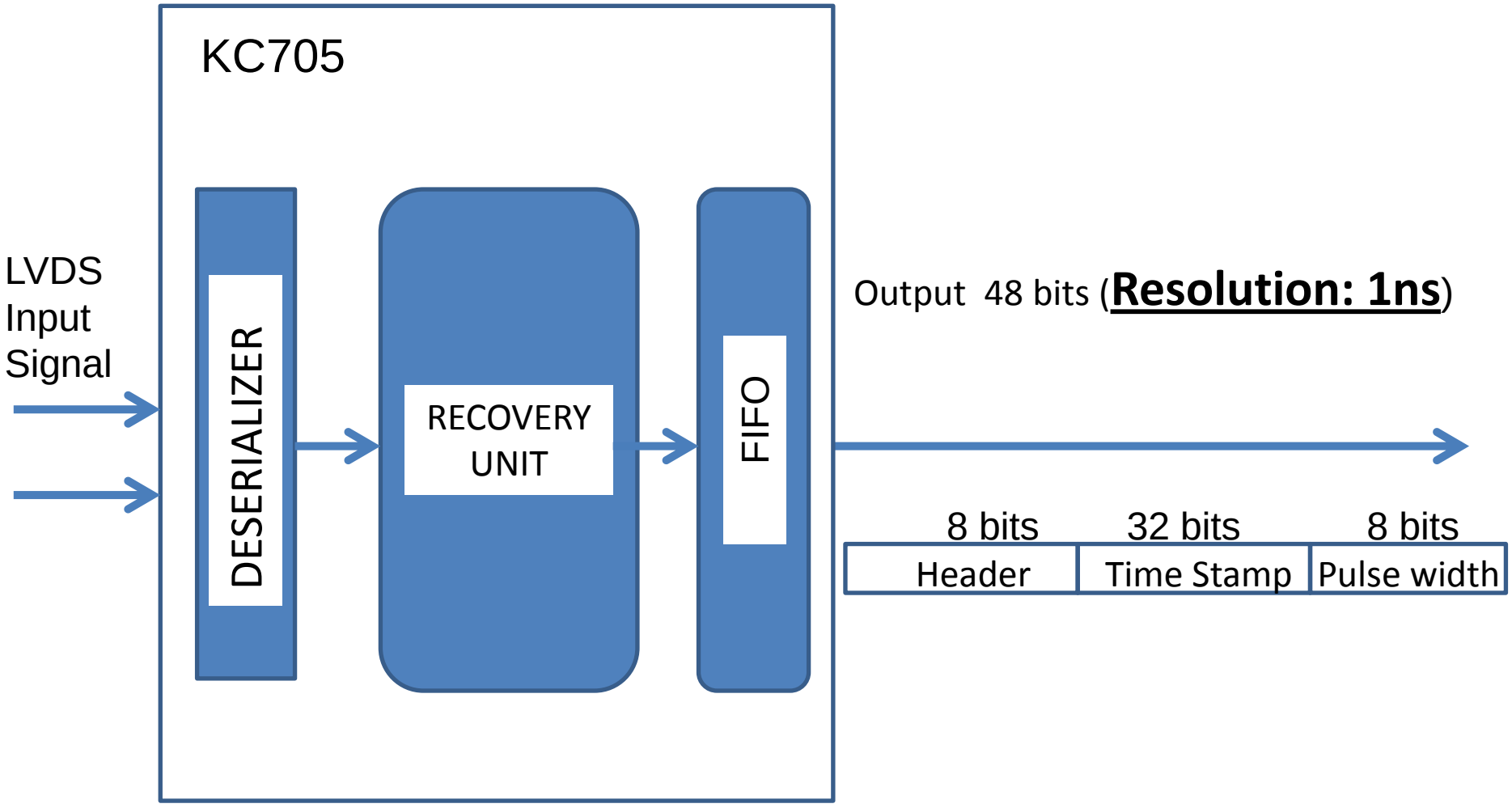
CLB: Current status and development on CLBv2 in Valencia

David Calvo

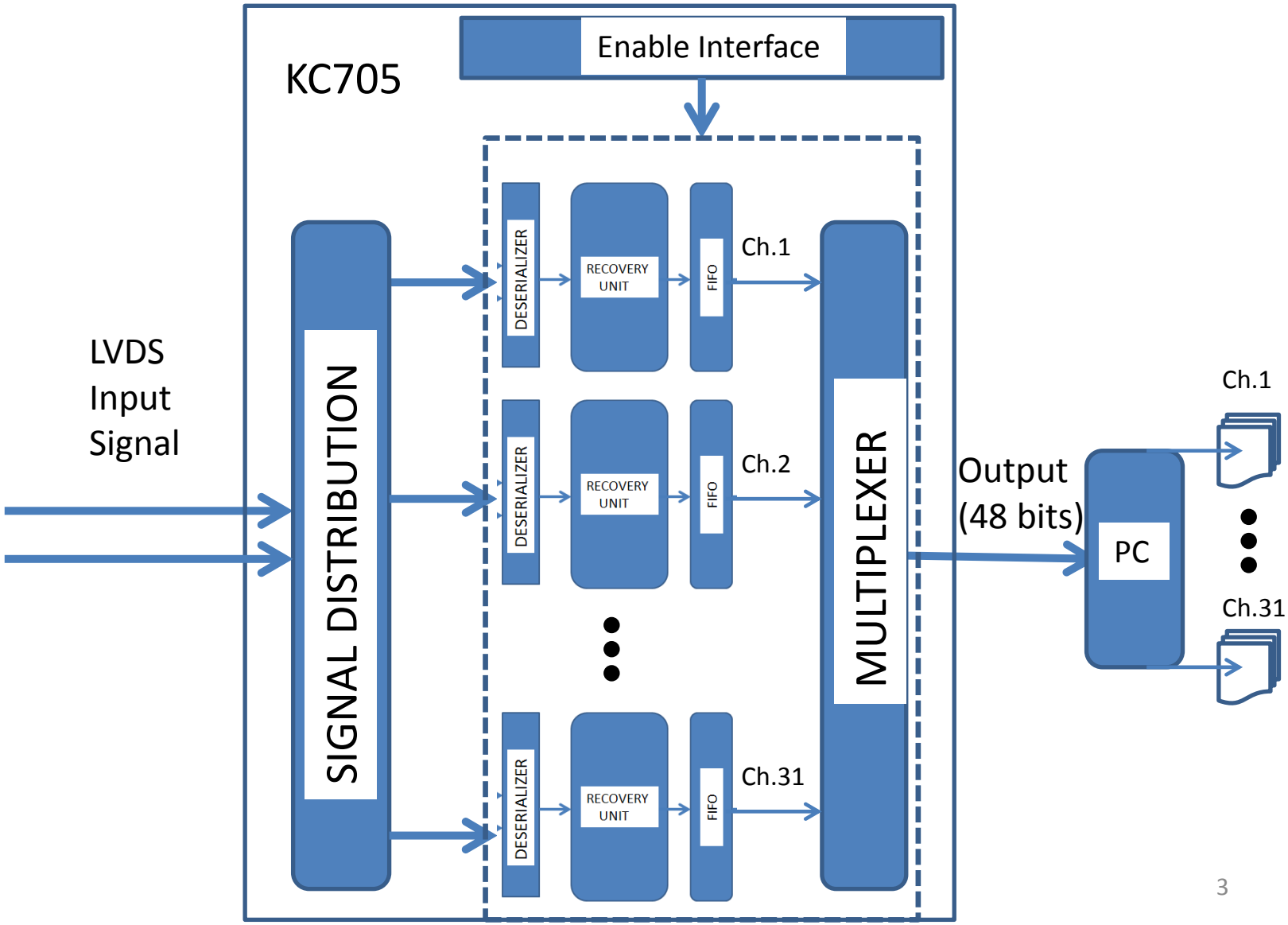
IFIC (CSIC – Universidad de Valencia)

Marseille 30 January 2013

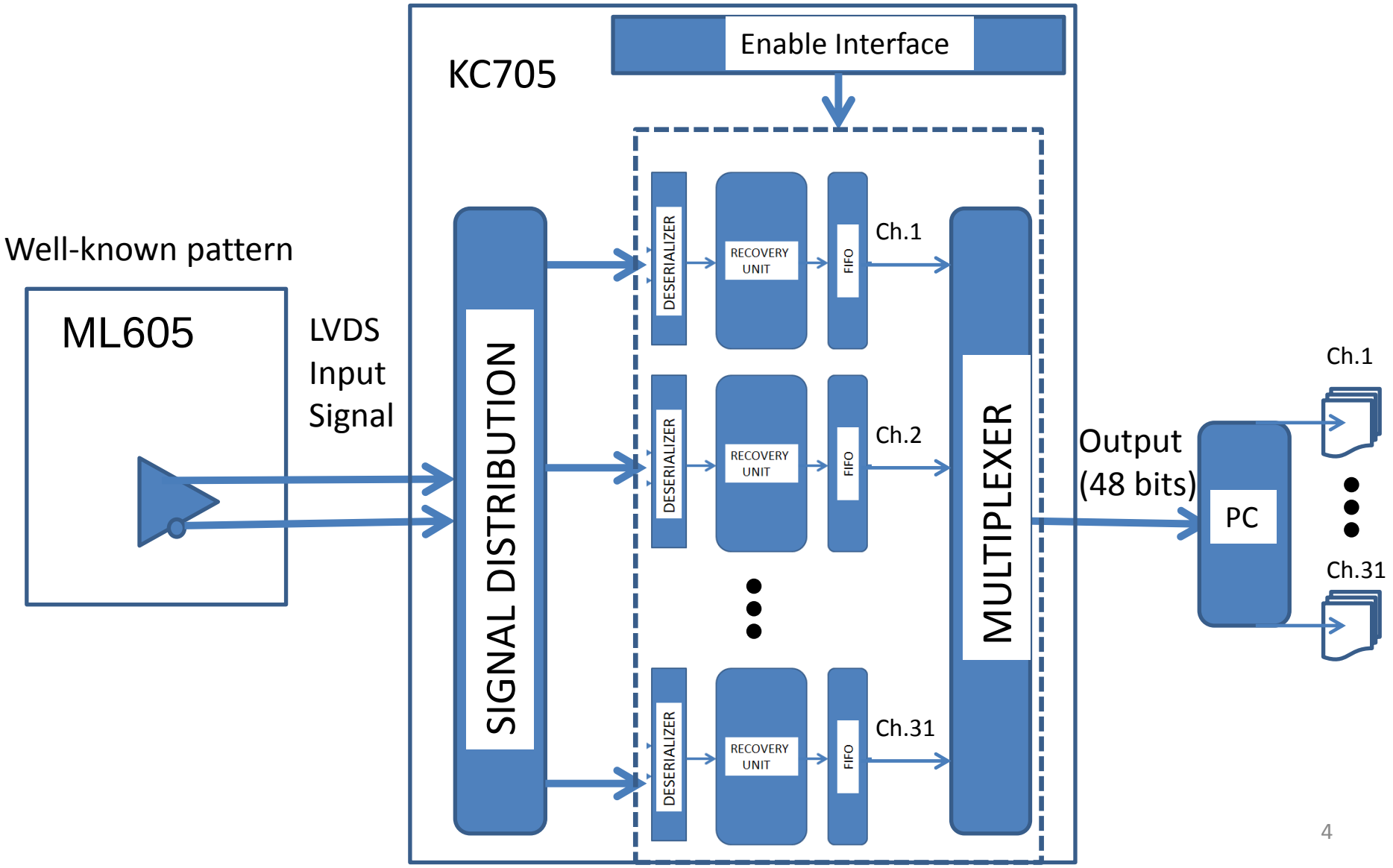
TDC: DESIGN


KC705
LVDS
Input
Signal
DESERIALIZER
RECOVERY
UNIT
FIFO
Output 48 bits (Resolution: 1ns)
8 bits
32 bits
8 bits
Header
Time Stamp
Pulse width

TDC: 31 CHANNELS



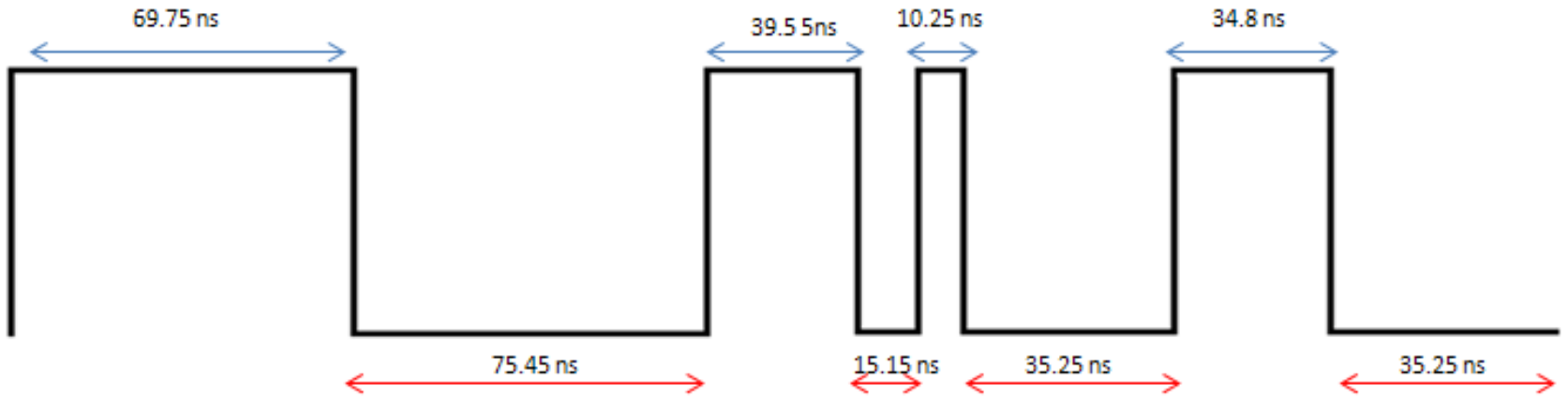
TDC: TEST


KC705
Enable Interface
Well-known pattern
ML605
LVDS
Input
Signal
SIGNAL DISTRIBUTION
DESERIALIZER
RECOVERY UNIT
FIFO
Ch.1
Ch.2
Ch.31
MULTIPLEXER
Output
(48 bits)
PC
Ch.1
Ch.31

TDC: PATTERNS TO TEST

CHANNEL 1

CHANNEL 2



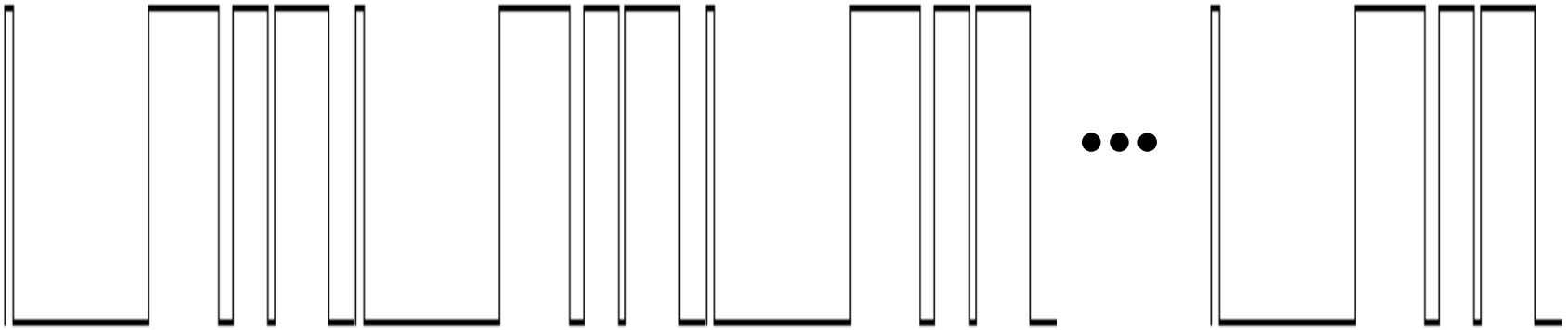
Jitter = 0.3 ns

TDC: PATTERN TO TEST

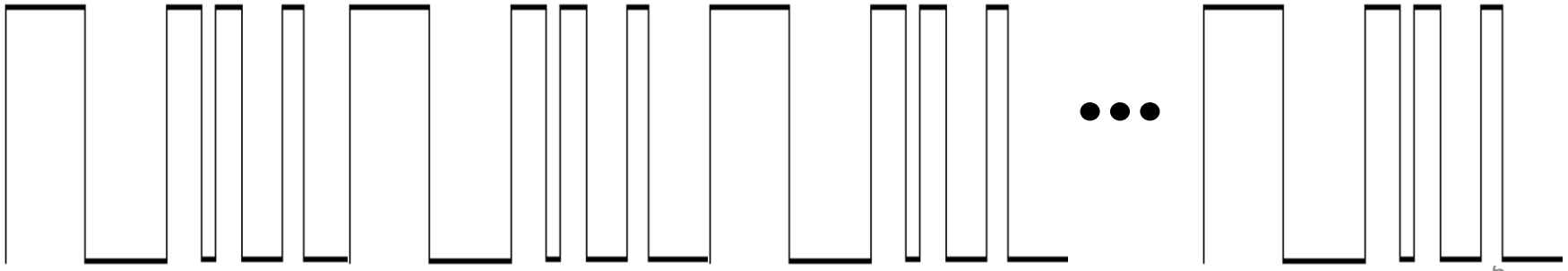
Patterns replicated 250 times

1000 pulses x channel

CHANNEL 1



CHANNEL 2

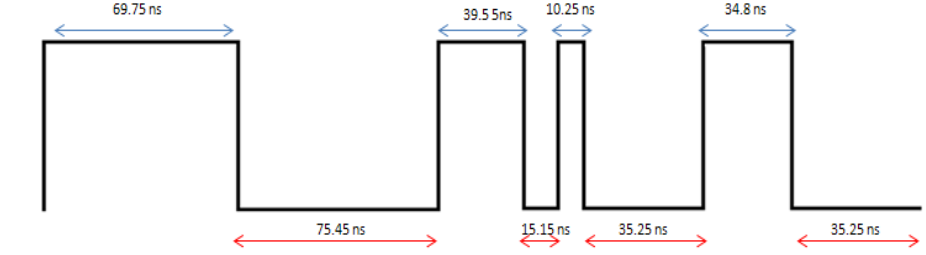


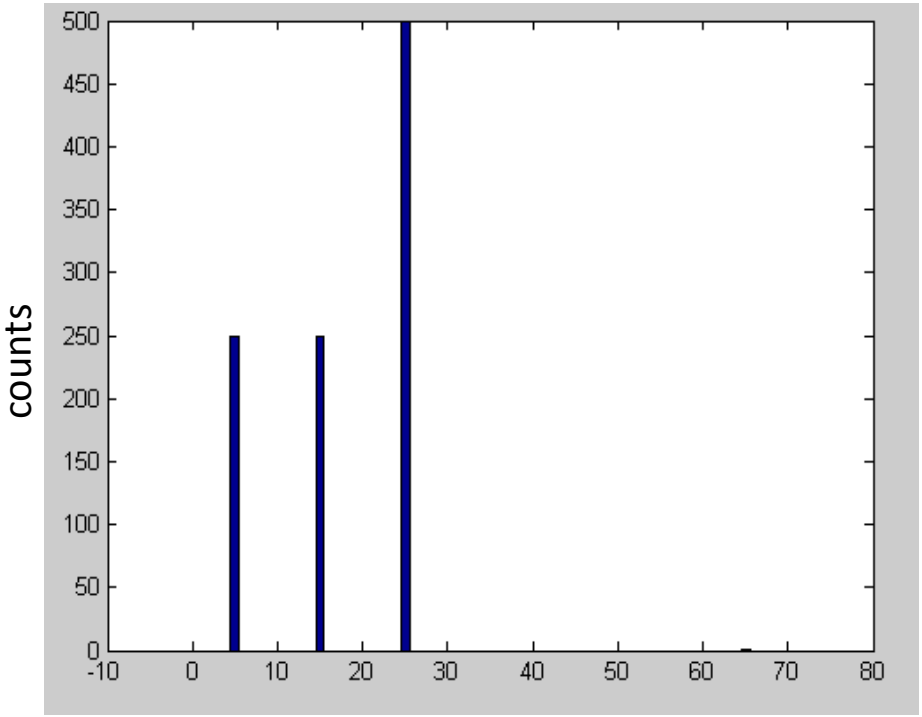
TDC: RESULT

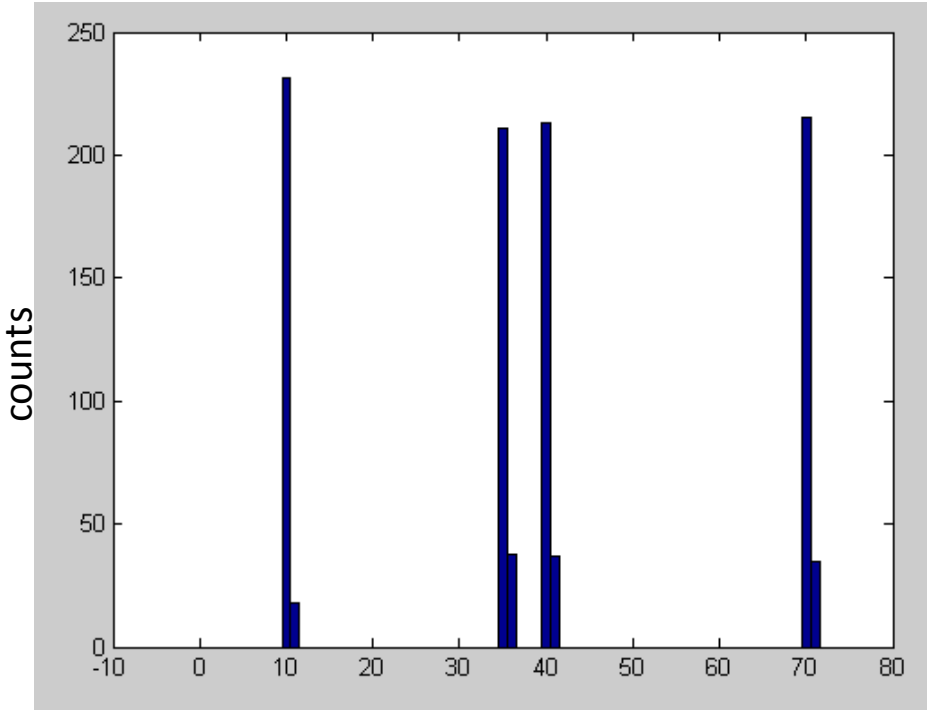
CHANNEL 1

Pulse width

CHANNEL 2

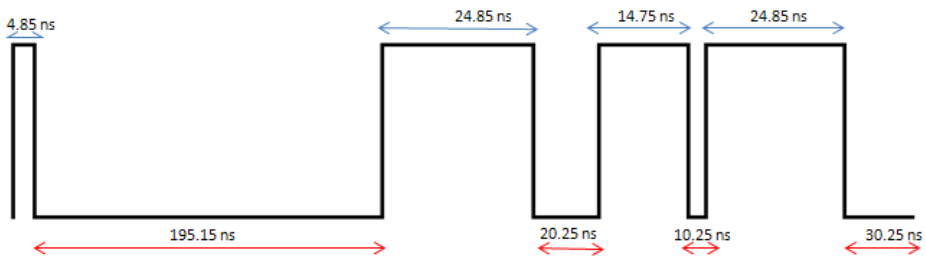


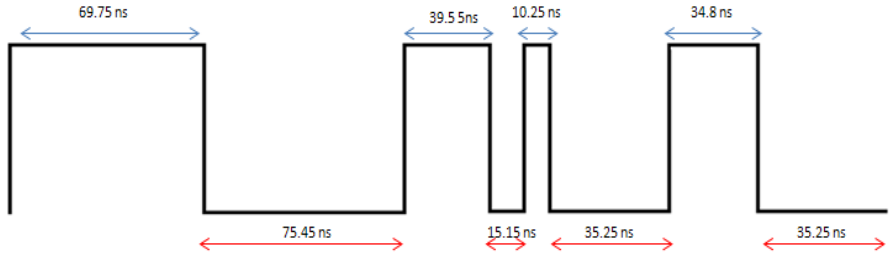


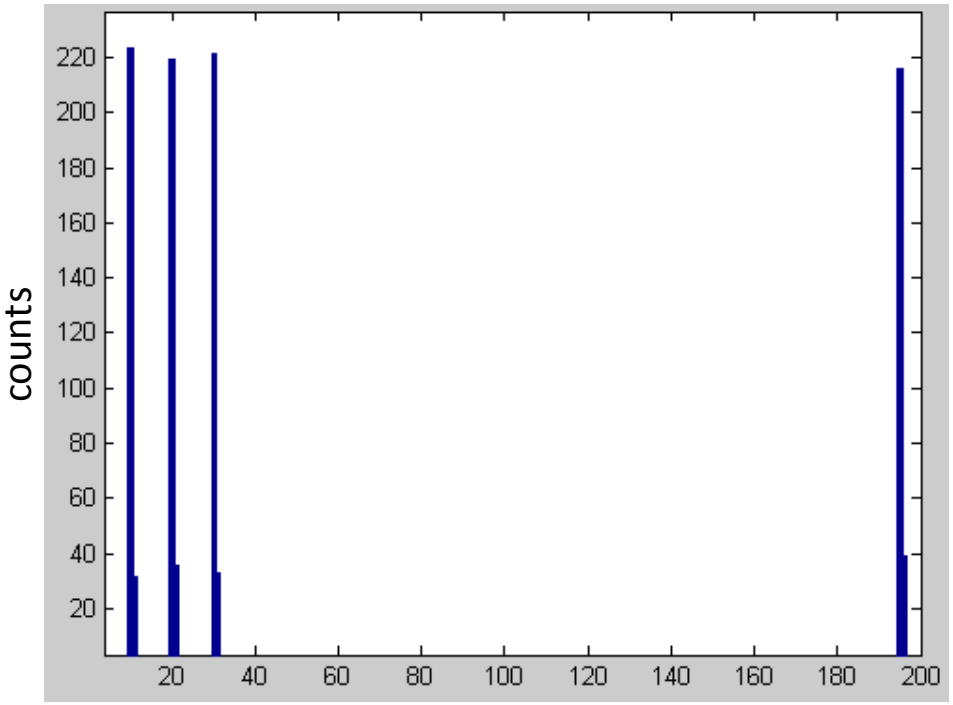


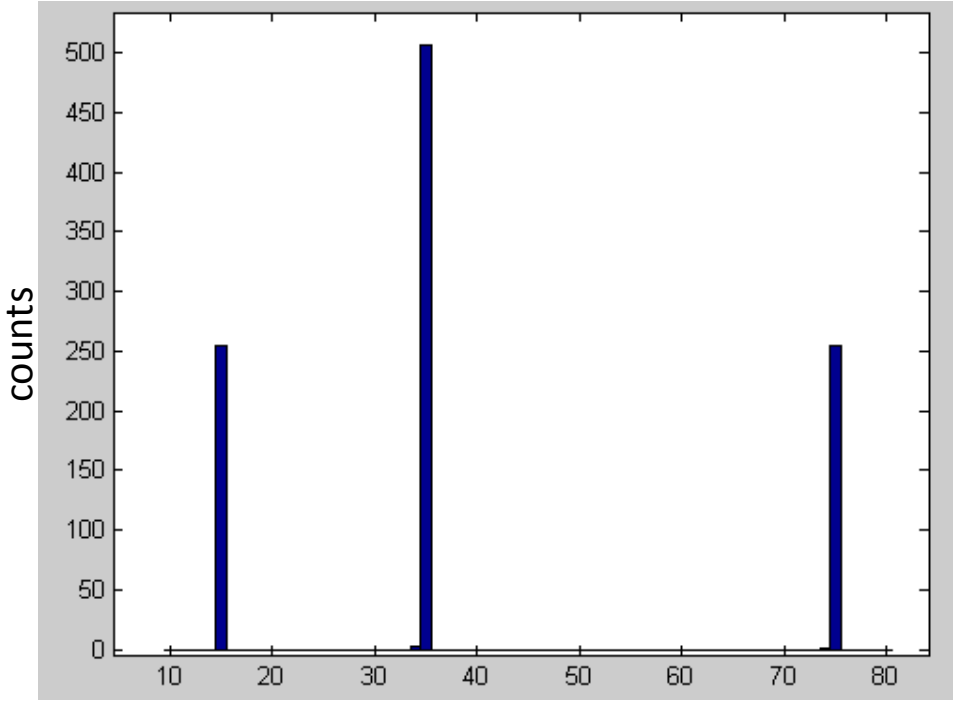
TDC: RESULT

CHANNEL 1 **Time between pulses** CHANNEL 2



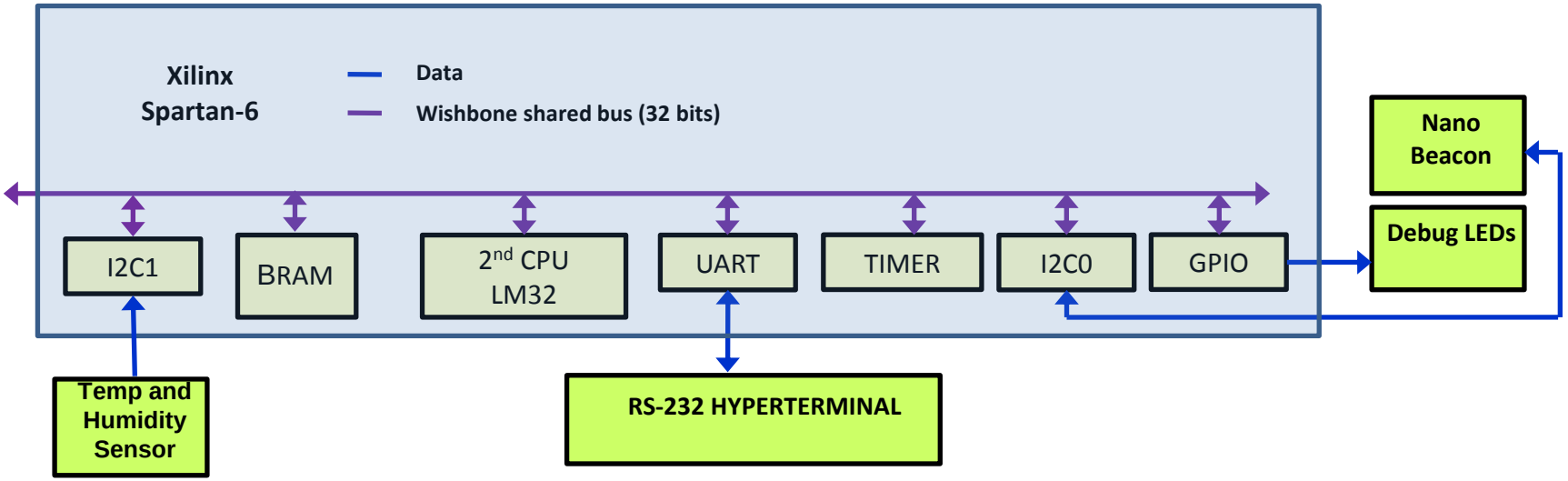




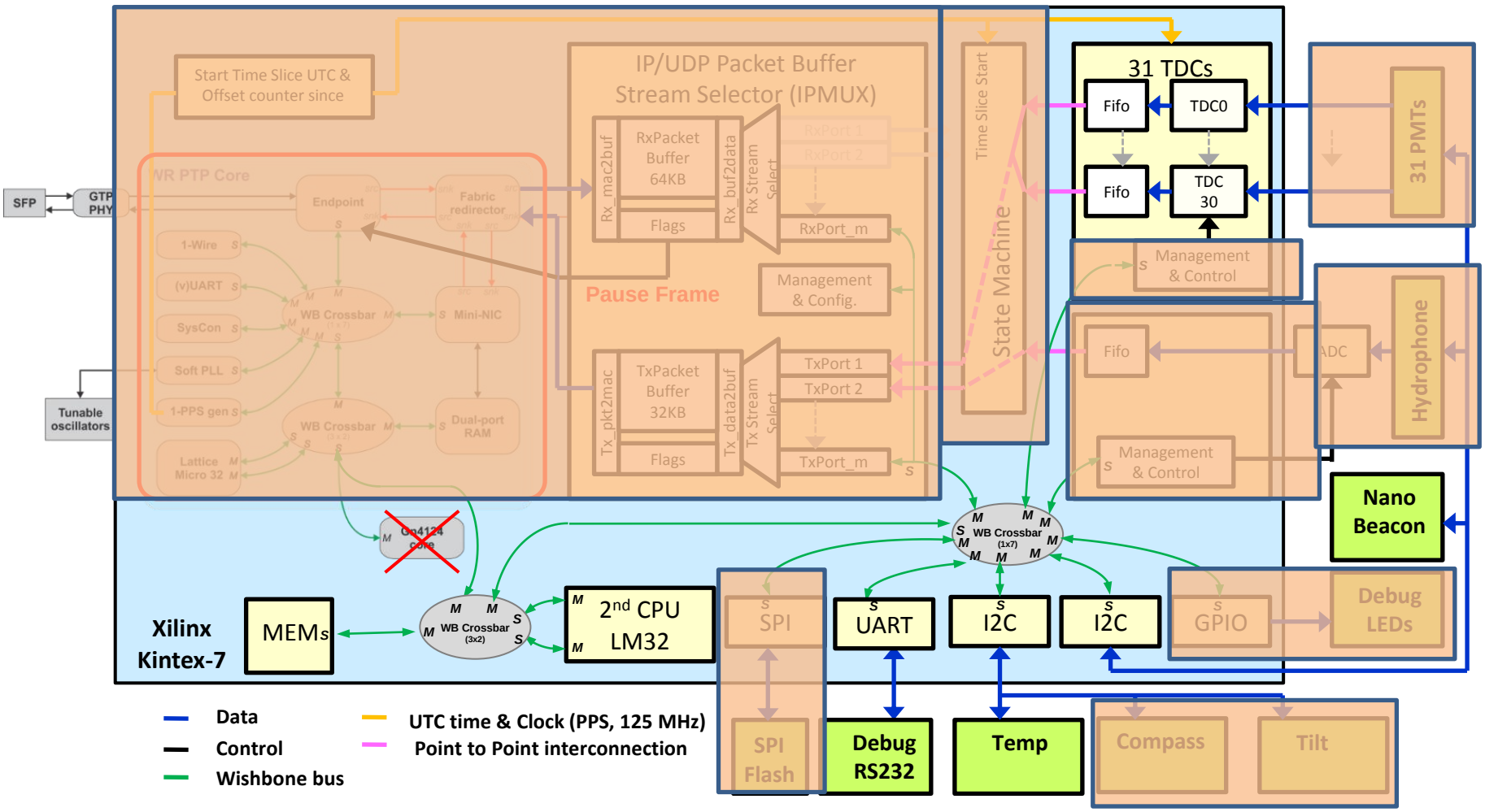


LM32 DEVELOPMENTS IN VALENCIA

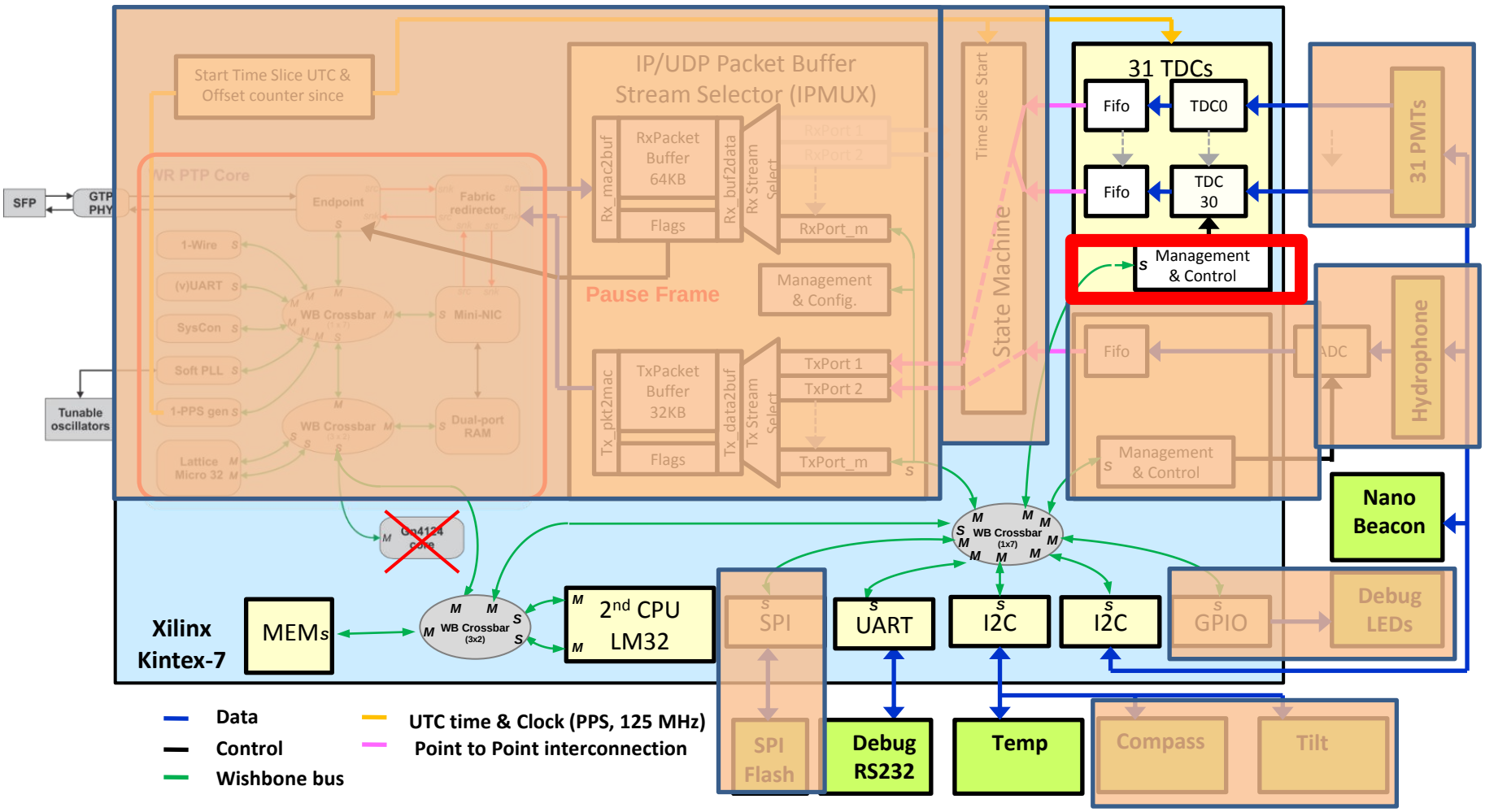
- **LM32 SOC with several wishbone slaves (32 bits bus):**
  - BRAM
  - UART
  - TIMER
  - I2C0 Nanobeacon
  - I2C1 Temperature and Humidity sensor (DIGIPICCO)
  - GPIO



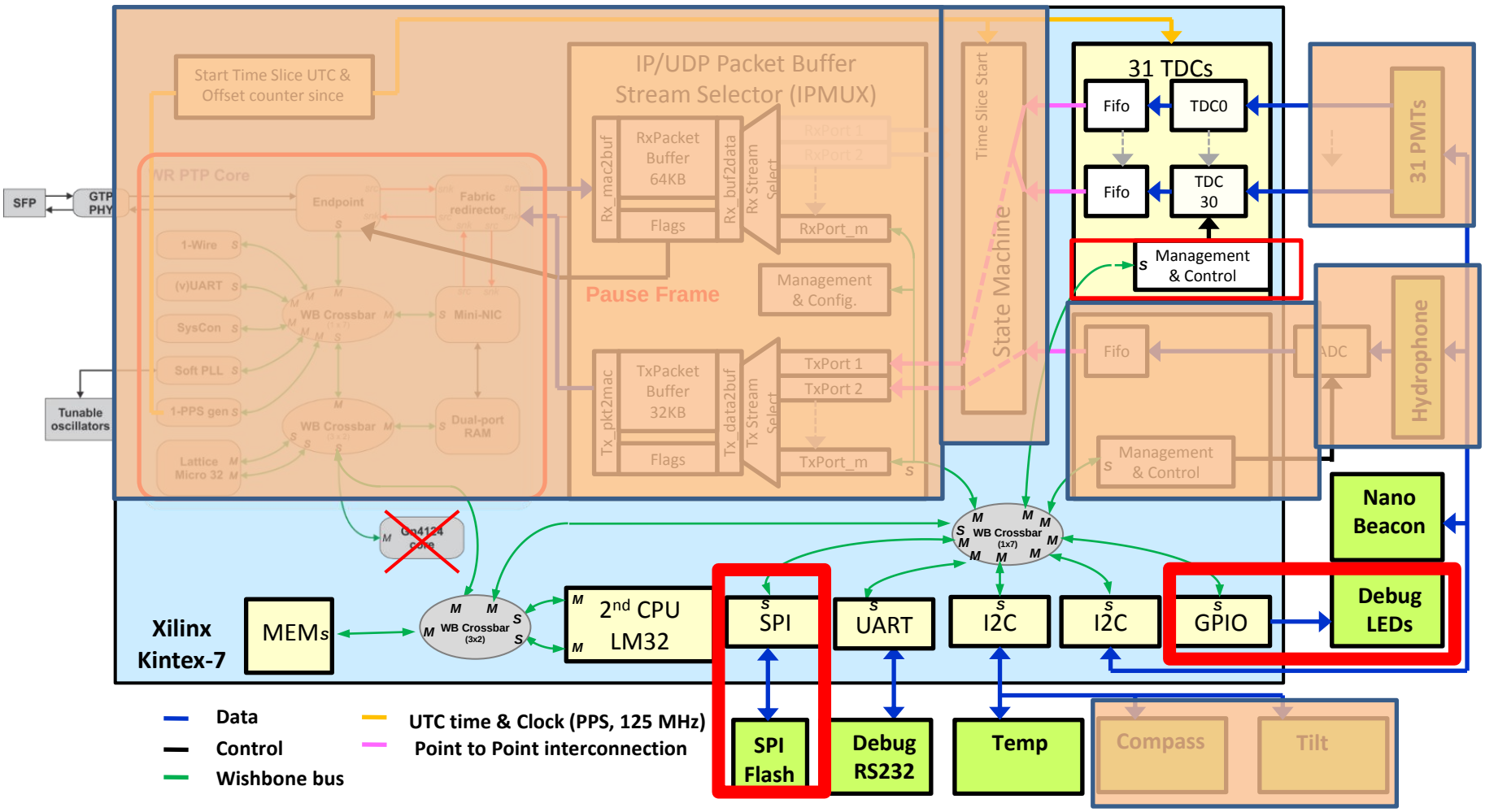
LM32 DEVELOPMENTS IN VALENCIA



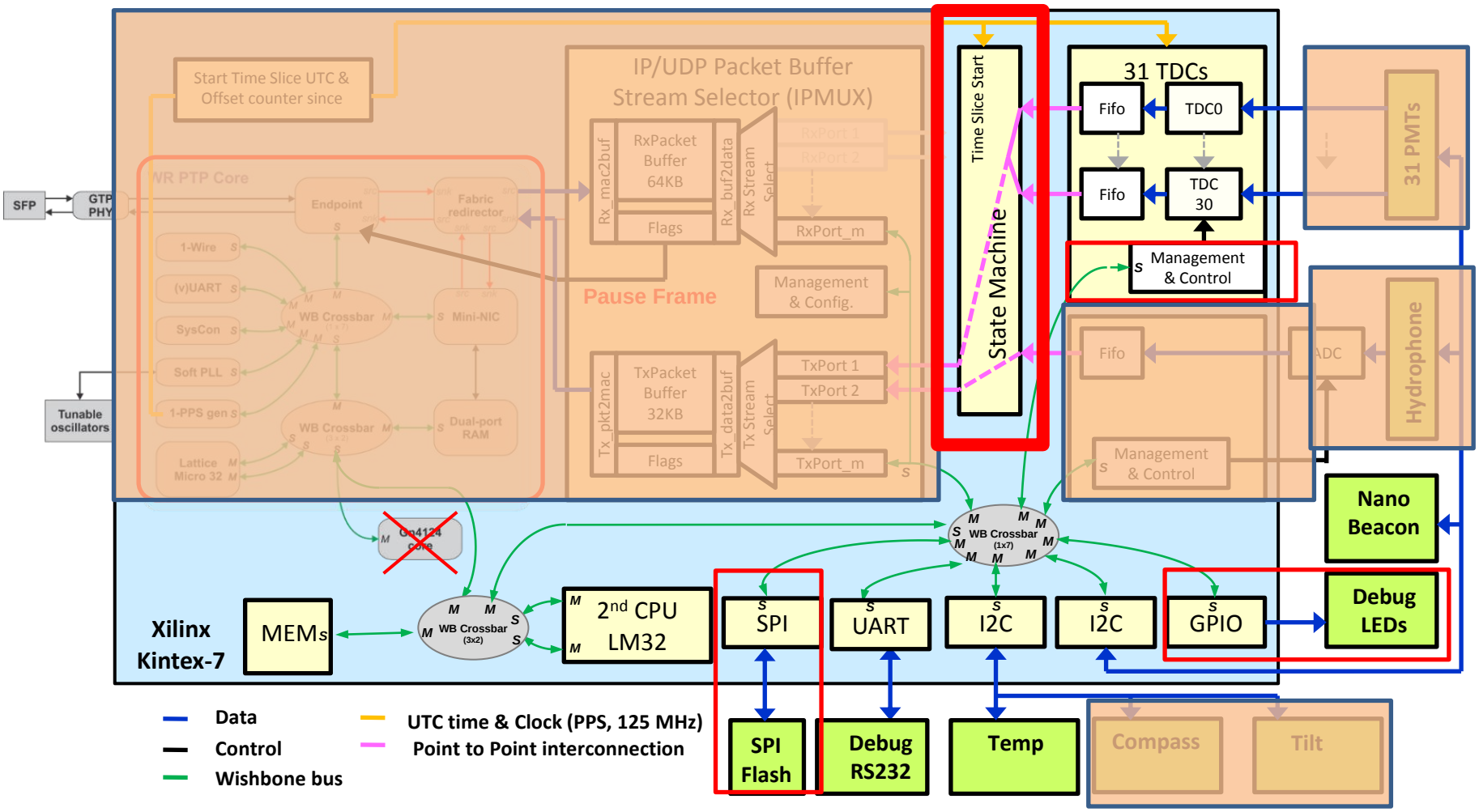
NEXT STEPS IN VALENCIA (I)



NEXT STEPS IN VALENCIA (II)



NEXT STEPS IN VALENCIA (III)

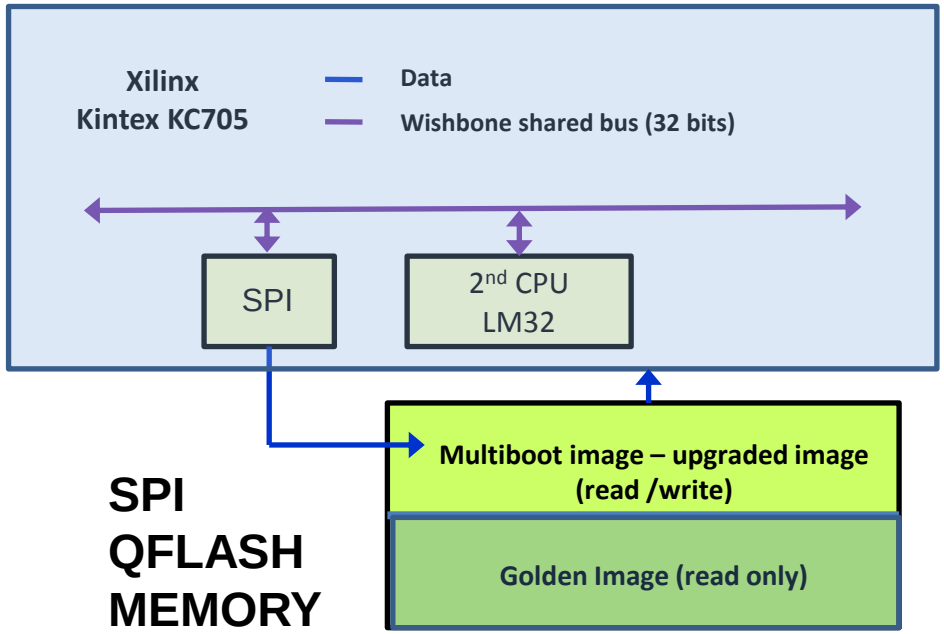


NEXT STEEPS IN VALENCIA (IV)

Implement reconfigurability:

A.- To use the multiboot capabilities of the KINTEX

B.- To be able to write on the SPI FLASH with the LM32



THANKS FOR YOUR ATTENTION!

LM32 developments in Valencia