

# First of all

... as freshly entrusted with DAQ/ReadOut coordination (*thanks to everyone for the confidence !*):

## Priorities

- going through the related topics



- report to the **SC** about the needed manpower/task

[tommaso.chiarusi@bo.infn.it](mailto:tommaso.chiarusi@bo.infn.it)

T. Chiarusi



ALMA MATER STUDIORUM  
UNIVERSITÀ DI BOLOGNA

# The **INFN-Bologna** Group

S. Biagi, T. Chiarusi, A. Margiotta, M. Spurio ***et al.***

INFN-Sezione di Bologna, University of Bologna

*Presented by A. Margiotta*

*(or by TC, if the connection is good !)*

***et al.***

## **Full Time**

- 1 Informatics INFN Post-Doc

**arriving by the  
end of February !!!**

## **Part-Time**

- 2 senior Computer Engineers (Univ. of Bologna)
- 1 Computer Engineers Post Doc (Univ. of Bologna)  
**Experts in S/W & middleware for distributed computing**
- 1 Informatics System Technician (INFN/Sez. Bologna)
- Support from Electronics Technicians of INFN/Sez. Bo

# Tasks of interest in Bologna

**T. Chiarusi** et *those* al.

- Development of data-filters + data managers (+ all needed simuls. of HW interfaces)
- Development of Monitoring
- Development of Middleware for data routing and process communications

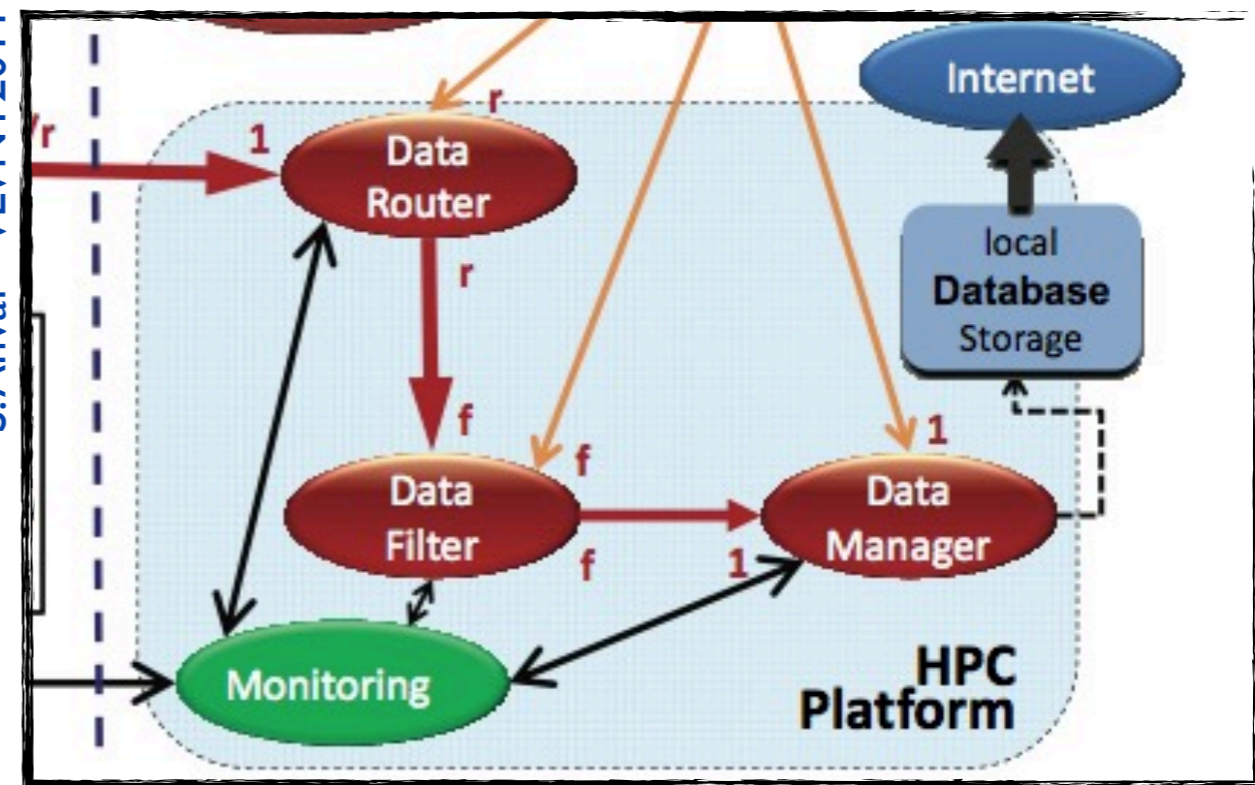
**S. Biagi**, with Italian electronics group (P. Musico, INFN-GE)

- Development of CLB interface to a part of the SC instrumentation, e.g. see figure below:

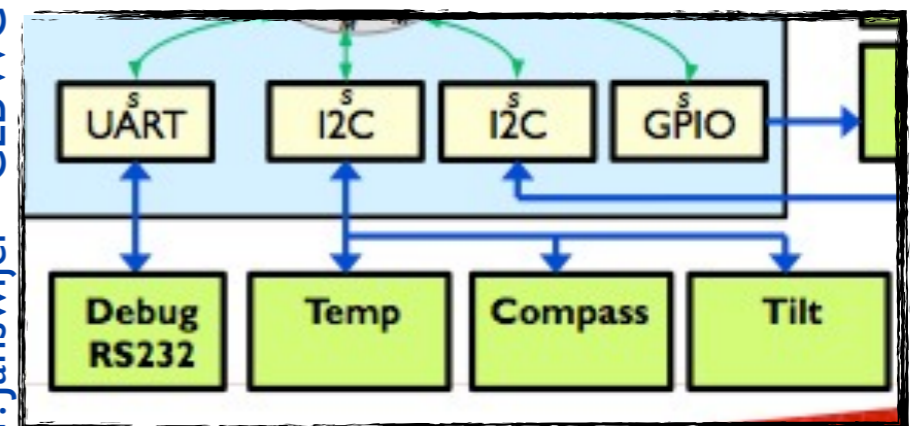
## Common task

- Test-benching with available hw&sw

S.Anvar - VLVNT2011



P.Janswijer - CLB WG



# a kick-off (done) list

## part 1 - Software

✓ Purchased benchmark “twin” server

E-Rack 7126 - 4 x 4 bays SATA 2,5

2 x Dual Xeon – 5520 – Server Dual

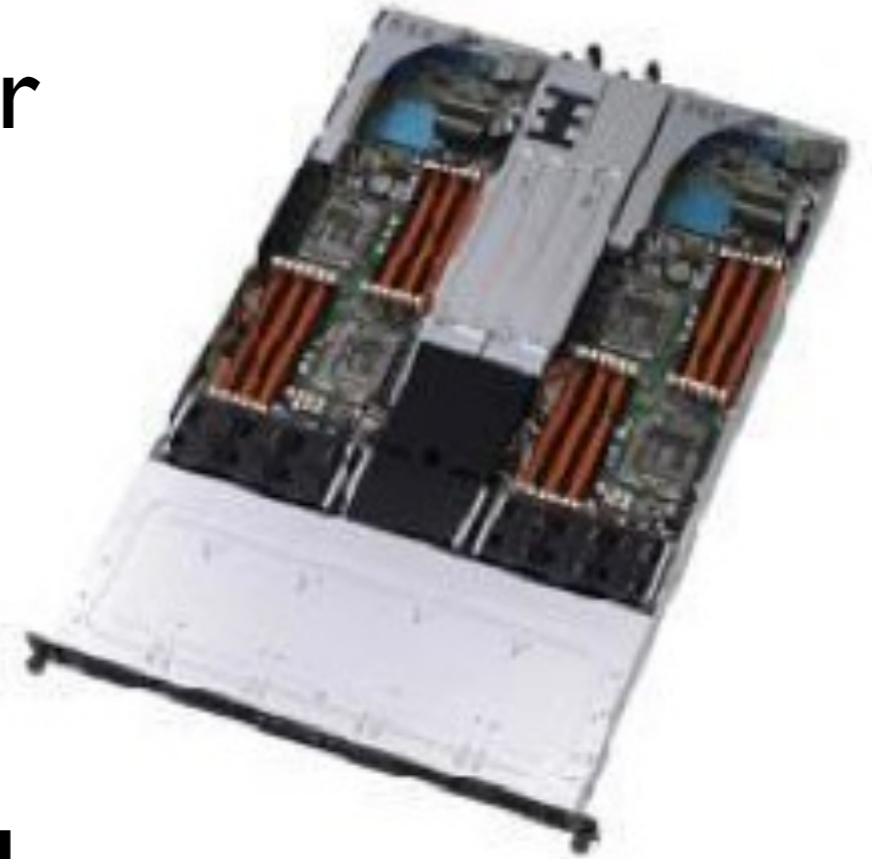
2 x 13179 Intel ICH10R SATA II Raid 6 port

4 x 14033 Xeon SixCore E5645 2,40Ghz 12MB 5,86GT/sec

12 x 19496 Modulo DDR3–1333 Reg. ECC 8 GB

2 x 73125 Intel Gigabit ET Dual Port Server E1G42ET

2 x 15224 SEAGATE 1TB 2,5" SATA 7.200RPM



✓ Translation and Optimization of MdJ  
“*Data Format*” proposal into an actual class  
design + initial study of “ANTARES\_DAQ”

✓ Preliminary test of data streaming I/O

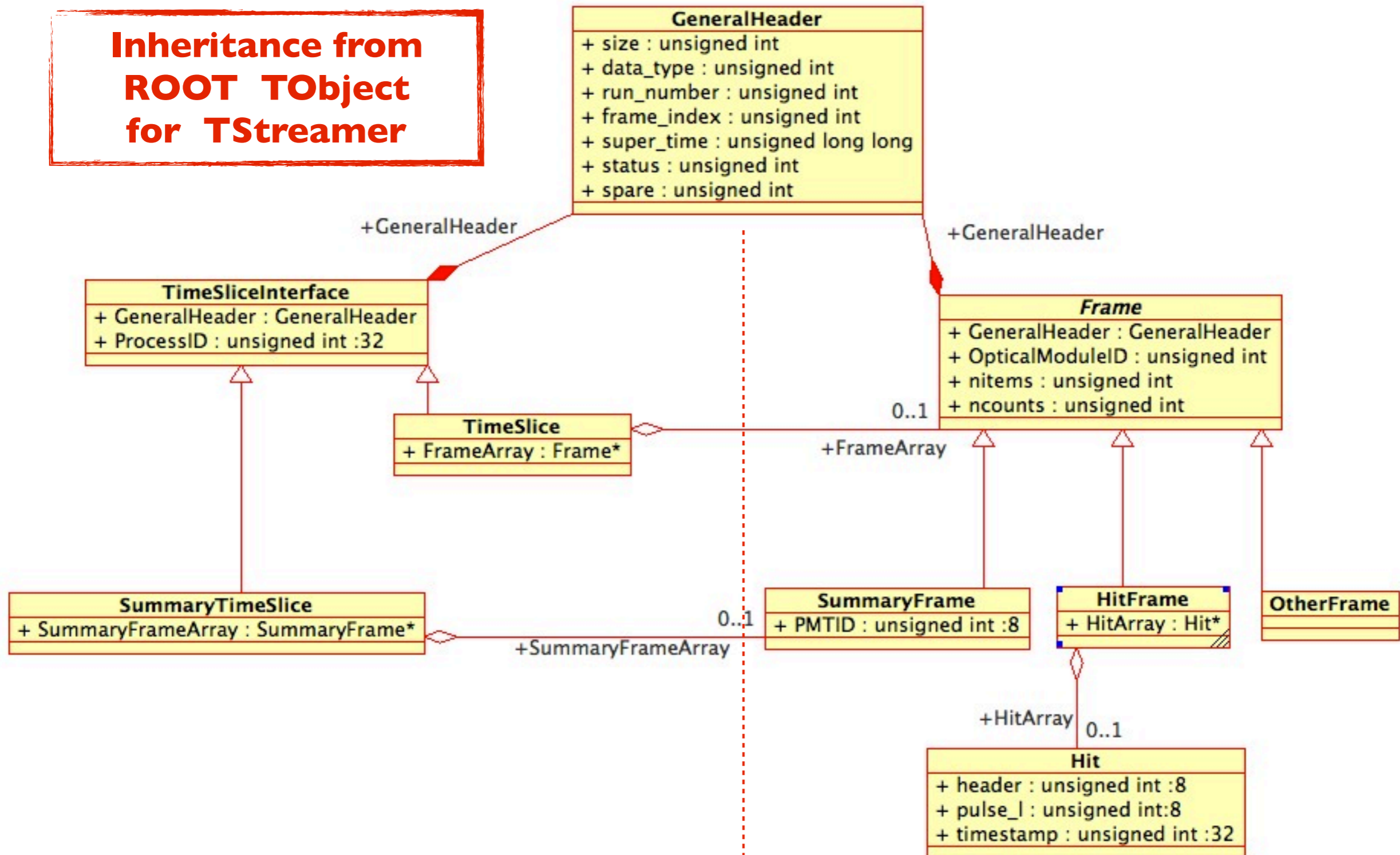
✓ Built up software for versioning (SVN),  
tracking and managing



# Very first implementation of DataFormat Classes

## A logical view

**Inheritance from  
ROOT TObject  
for TStreamer**




# Versioning: SVN code access & management with



## Web-access project managing

Panello di Controllo  
<https://portale-sisinfo.infn.it/>



Integrated SCM & Project Management

logged in as chiarusi | [Logout](#) | [Settings](#) | [Help/Guide](#) | [About Trac](#)

Search

Wiki | Timeline | Roadmap | **Browse Source** | View Tickets | New Ticket | Search

[Last Change](#) | [Revision Log](#)

root / **project**

View revision:

Name ▲	Size	Rev	Age	Last Change
<a href="#">../</a>				
<a href="#">DataFormat</a>		3	10 minutes	chiarusi: Initial import
<a href="#">TriDAS_NF2</a>		2	18 hours	chiarusi: Initial import
<a href="#">trunk</a>		1	18 hours	chiarusi: Initial import

Note: See [TracBrowser](#) for help on using the browser.

[View changes...](#)

Powered by **Trac 0.10.5**  
By [EdgeWall Software](#).

Visit the Trac open source project at  
<http://trac.edgewall.org/>

logged in as chiarusi | [Logout](#) | [Settings](#) | [Help/Guide](#) | [About Trac](#)

Wiki | Timeline | Roadmap | **Browse Source** | View Tickets | New Ticket | Search

[Last Change](#) | [Revision Log](#)



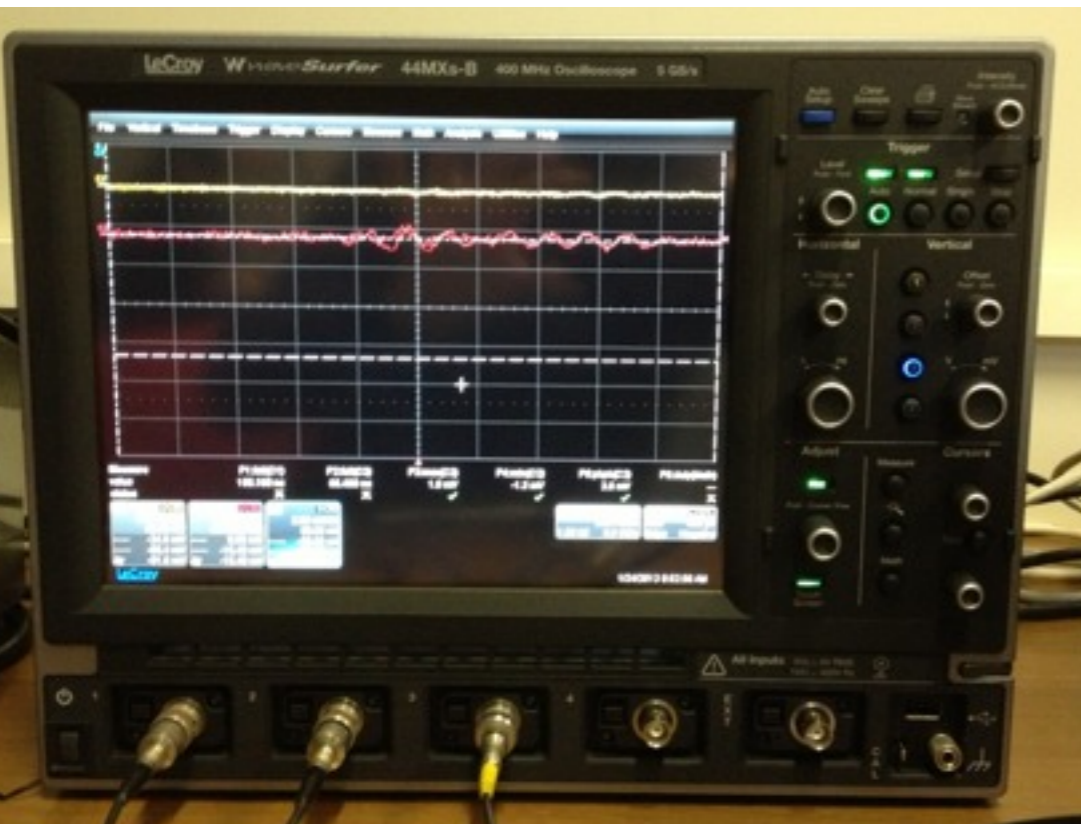
# a kick-off (supplying) list

## part 2- Hardware recently purchased

Arbitrary waveform generator  
RIGOL D05072 @ 70 MHz



LeCroy Wave Surfer 44MXs-B  
400 MHz, 5 GS/s



FPGA - Virtex 5 ML 501  
evaluation board

in addition to:  
other pulsers (analog./digit.), oscilloscopes,  
power supplies, cables and connectors.

We've prepared (so far) a basic-equipped lab .



# outline

## Short-term goals

- S/W: Optimize Data Format streaming and I/O
- S/W: Implement a data-stream Simulator
- H/W: Start “programming” FPGA (ISE WebPack)

## Long-term goals

- M/W & S/W: the effective TriDAS (on-shore DAQ) design and implementation
- H/W: cover an uncovered item (Slow Control or similar business)

## a.s.a.p.-term goal

- Setup a test-bench in Bologna for H/W - S/W match