CLB: Current status and developments on CLBv2

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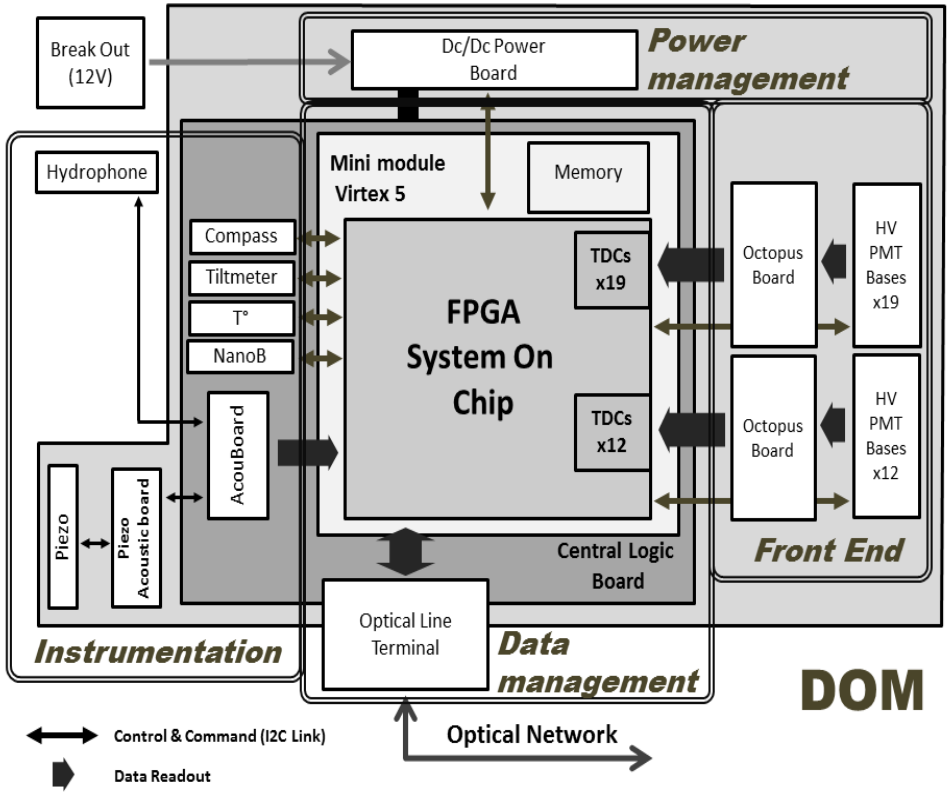
OUTLINE

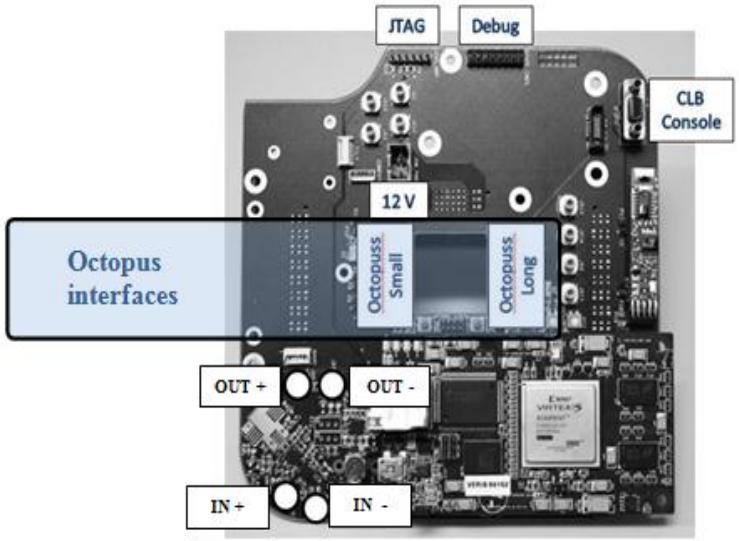
- CLB Current Status
- CLB V2
  - ✓ Requirements
  - ✓ Working group
  - ✓ Tasks
  - ✓ Architecture: Overview
  - ✓ Planning
  - ✓ Seafloor Instrumentation
  - ✓ SVN Repository
  - ✓ Seven Solutions
- SUMMARY

CLB: CURRENT STATUS

A completely operational CLB prototype already exists!! (PPM D.U and Tests)



- Developed by Saclay
- Based on Virtex 5 Xilinx FPGA



CLB: CURRENT STATUS

Batch of 4 CLB prototypes already produced by Valencia:

- One board completely tested at Saclay with the Valencia Crate and with the correspondent power board and instrumentation:
  - Power board - Tilts - Compass - Nanobeacon - Acouboard
- Expected to have the crate installed in Valencia next week
- PPM DU CLBs to be delivered to Nikhef by mid-February

Batch of 8 CLB prototypes already ordered:

- Tests to be carry out in Valencia
- To be used in the different test setups

Price:

- CLB board: 672 €
- Minimodule (V5FXT70): 900 €
- Total price (No VAT): **1572 €**

CLBv2: UPGRADE NEEDED

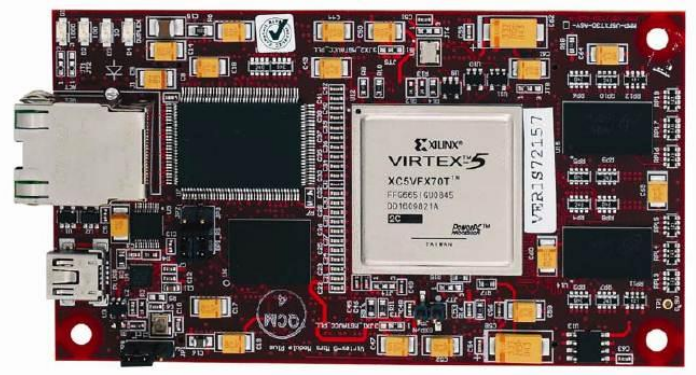
In a scale production the price of the CLB board will be reduced

But:

- **The minimodule is a development tool** and it is not produced in high quantities (a redesign is needed)
- The **price** of the Virtex 5 FPGA mounted is considerable high: 347 $ (2000 pieces)
- The **power consumption** of the Virtex 5 FPGA is considerable high as compared with newer FPGA technology

An upgrade of the CLB is mandatory:

- **Price and power consumption**
- **Standardisation/timing**
- **Availibility/development tools**



CLBv2: REQUIREMENTS

- 31 TDC channels with 1ns resolution
- Able to process more than 200 kHz events per TDC channel
- 1ns nanosecond synchronization between nodes
- Data pushed from PMTs to Shore Station
- Management of the TDCs and IO Instrumentation:
  - Configuration of the instrumentation:
    - Acoustics
    - Nanobeacon
    - Tilt
    - Compass
    - Temp
  - Configuration of the PMTs
  - Read-Out of instrumentation
- Reconfigurability of the firmware
- Low Power Consumption
- Low Cost
- High reliability
- Part of a scalable system

CLBv2: WORKING GROUP

Several groups already participating (Nikhef, APC, Genova, IFIC, Bologna, Democritos, ….) in the development of the CLBv2

The current working group:

- Organization: **Nikhef, Leo and Els**
- CLB for PPM-DU: **Demokritos, Saclay, IFIC, Nikhef, Catania, NOA**
- FPGA choice**: APC, IFIC, Nikhef, Bologna**
- Timing-syncro: **Nikhef**
- TDCs: **IFIC**
- Acoustic Read-out: **Genova, Catania**
- CLB layout: **Nikhef**
- Calibration/instrumentation: **ECAP, IFIC, Genova, Catania**
- Software: **Bologna**
- Data Format: **Nikhef**
- Test Setups for DOM production: **APC**

Any other group interested in participating? Please let us know

CLBv2: TASKS

Timing/synchro: Nikhef is working on it, implementing the White Rabbit system on the Kintex evaluation board. White Rabbit will give the 1 ns synchronization.

TDCs: 31 TDCs channels with 1ns is being implemented and tested on the Kintex Evaluation board. IFIC is in charge of it.

Instrumentation and TDCs configuration management: At the moment Nikhef and IFIC are working with an LM32 soft processor with a Wishbone bus for implementing the configuration management. Genova is starting to work also.

Acoustic read-out: Genova is working on the development of the Acoustic read-out firmware. Development Acouboard: a) hardware b) software for hydrophones, tiltmeters,compass, nanobeacons. New manpower in Spring 2013

CLBv2: TASKS

Reconfigurability: The requirements for reconfigurability are :

- Field updating with a new bitstream
- Guarding against system upsets due to an update failure
- As low as possible resource usage in User Logic.
- Work has started already on the IFIC

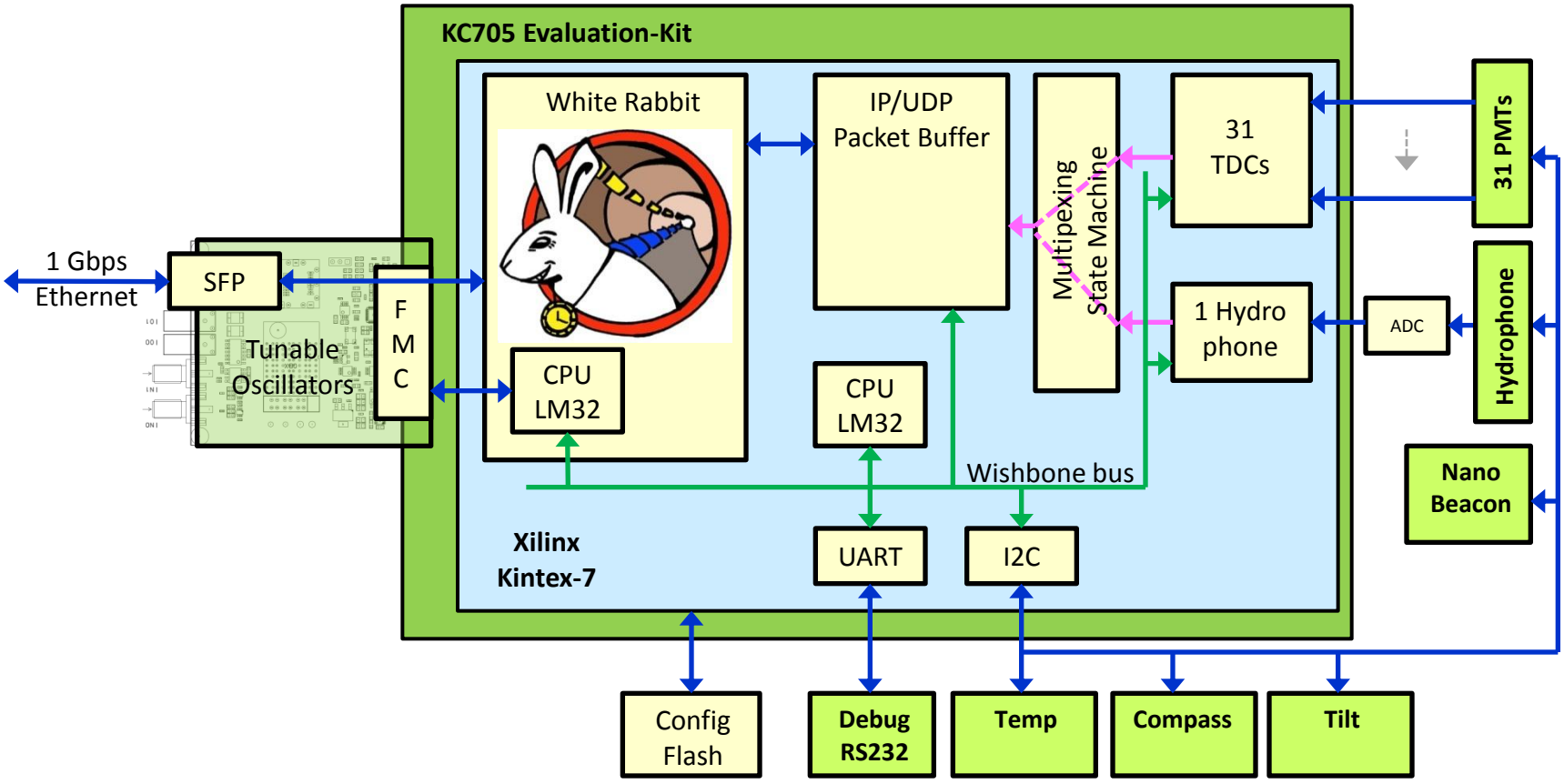
Hardware: The work on hardware will start when enough confidence that it can be implemented, which will depend on how work the tests on the Kintex evaluation board. One company interested on the job (S7)

Software: Bologna is already working on it

Note has been written about dataformat and about FPGA selection ✓

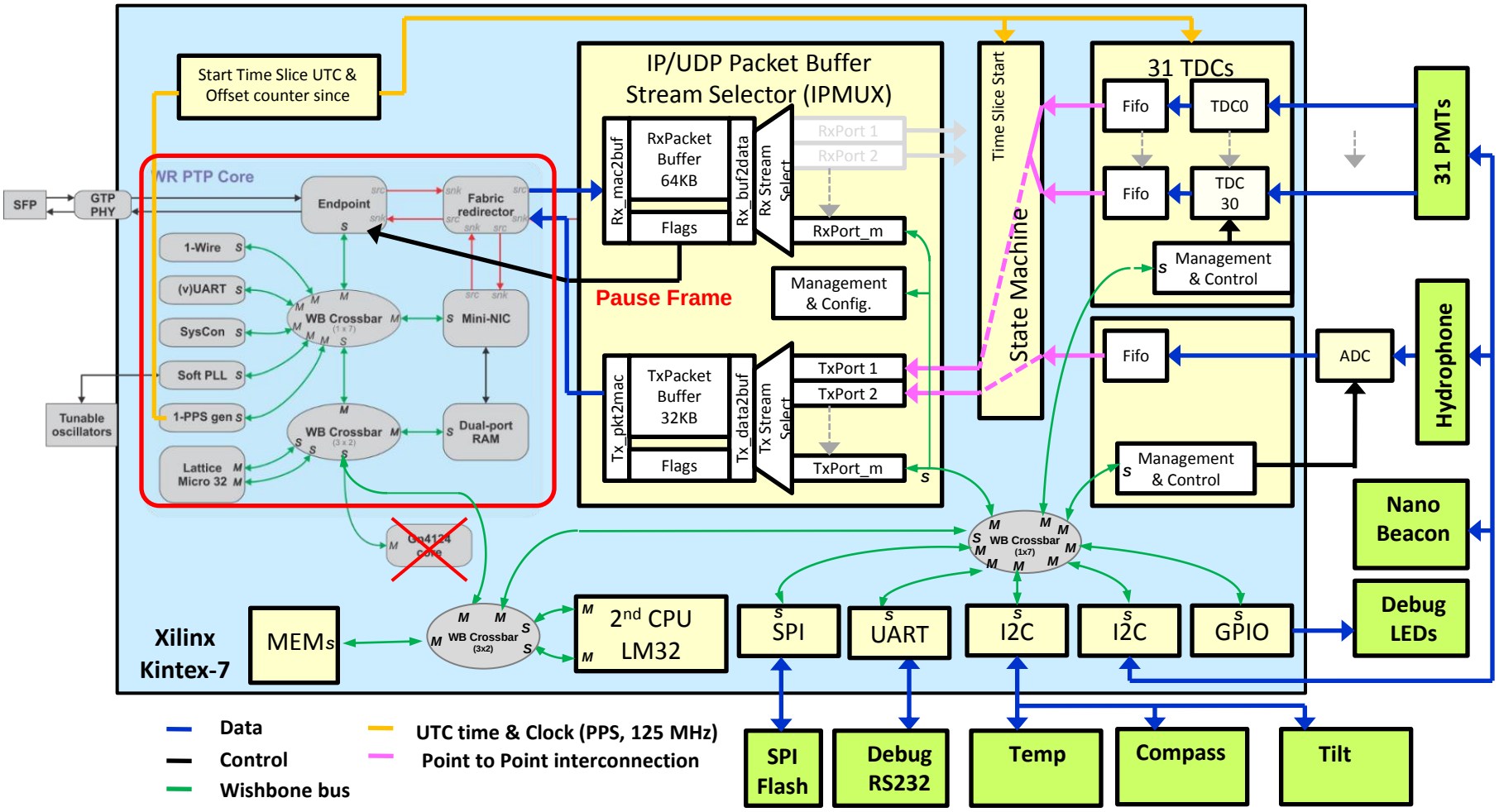
CLBv2: ARCHIRTECTURE: OVERVIEW

Functional prototype on KC705 development board

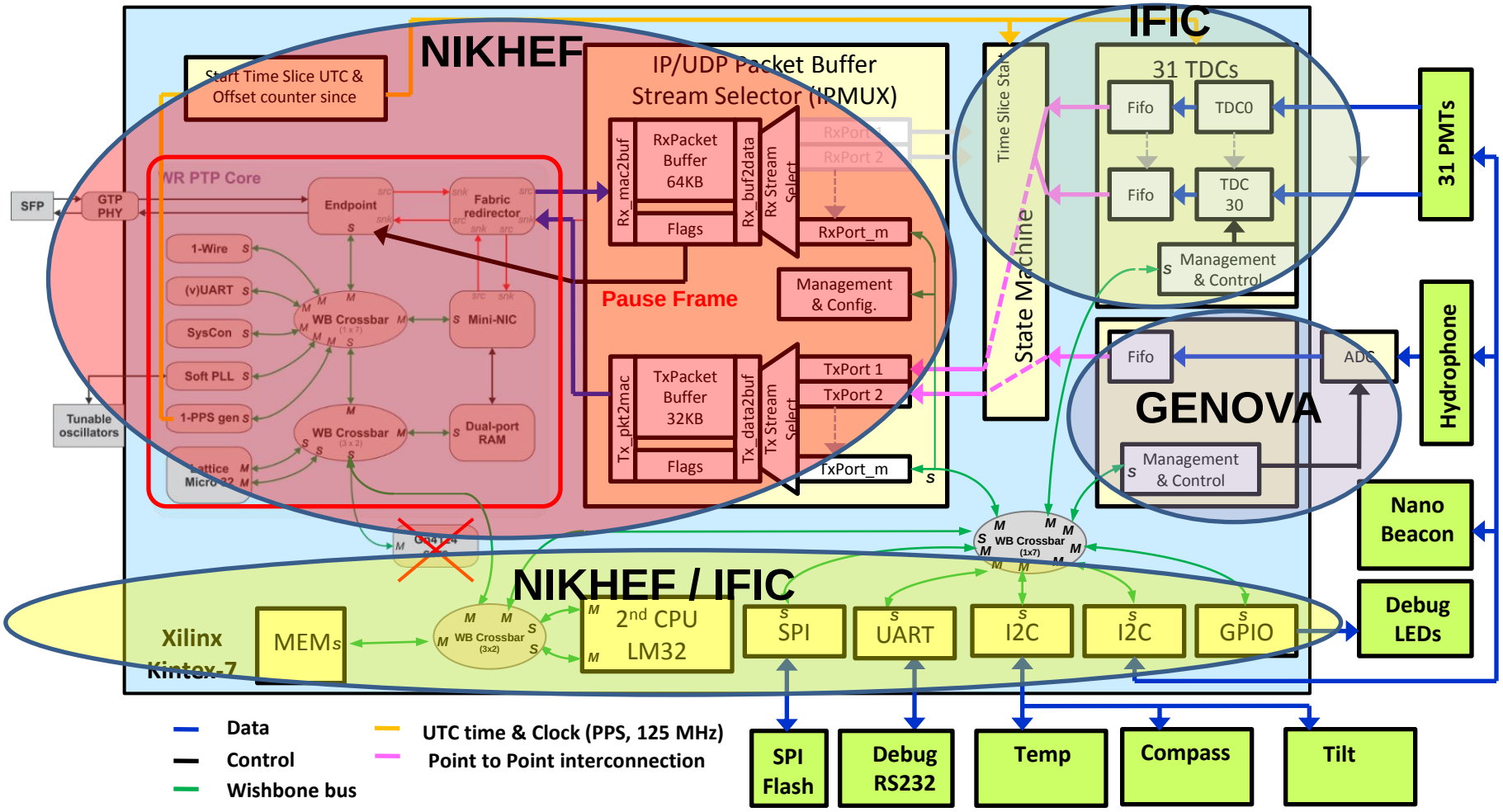


KC705 essential for testing interfaces via Soft PLL board
Test of prototype with White Rabbit switch

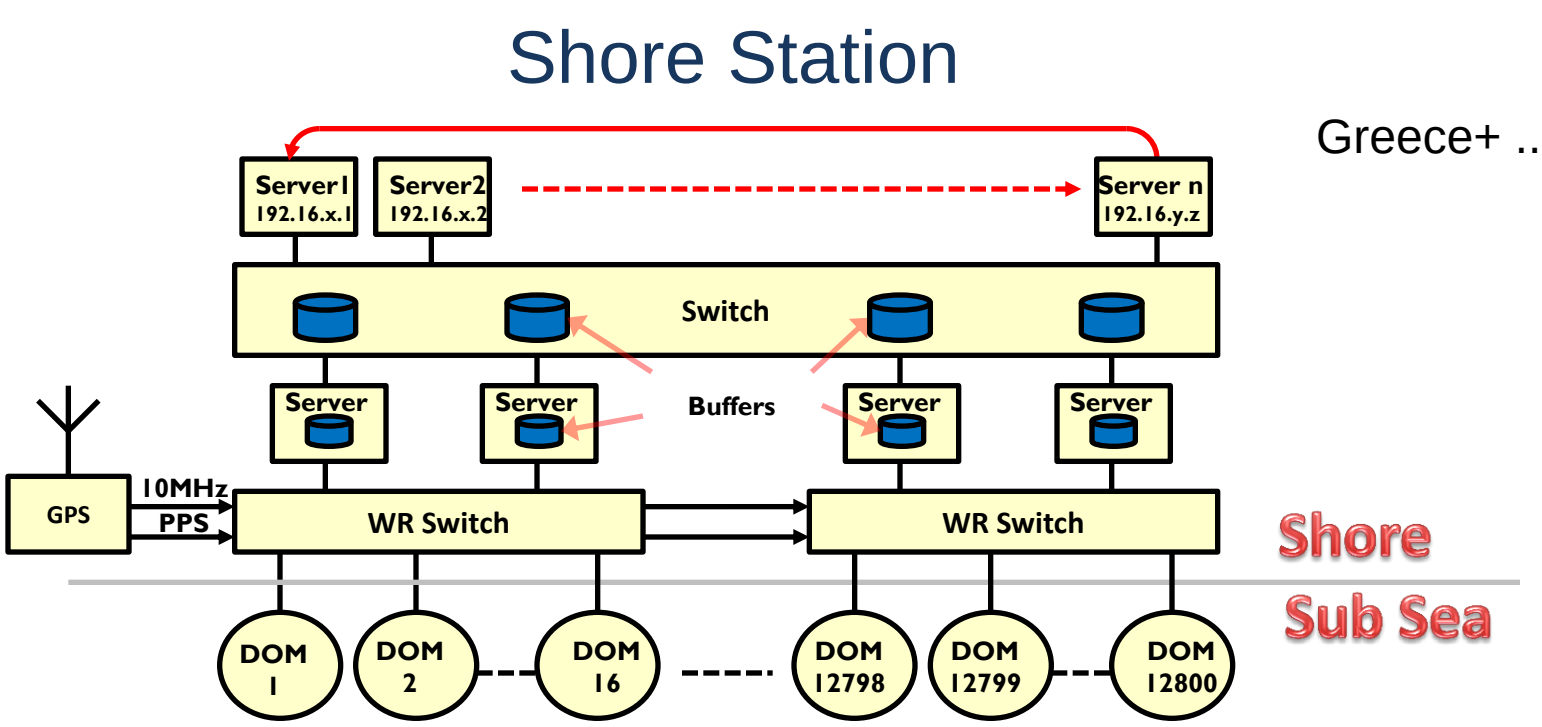
CLBv2: ARCHITECTURE: IN MORE DETAIL



CLBv2: ARCHITECTURE: IN MORE DETAIL

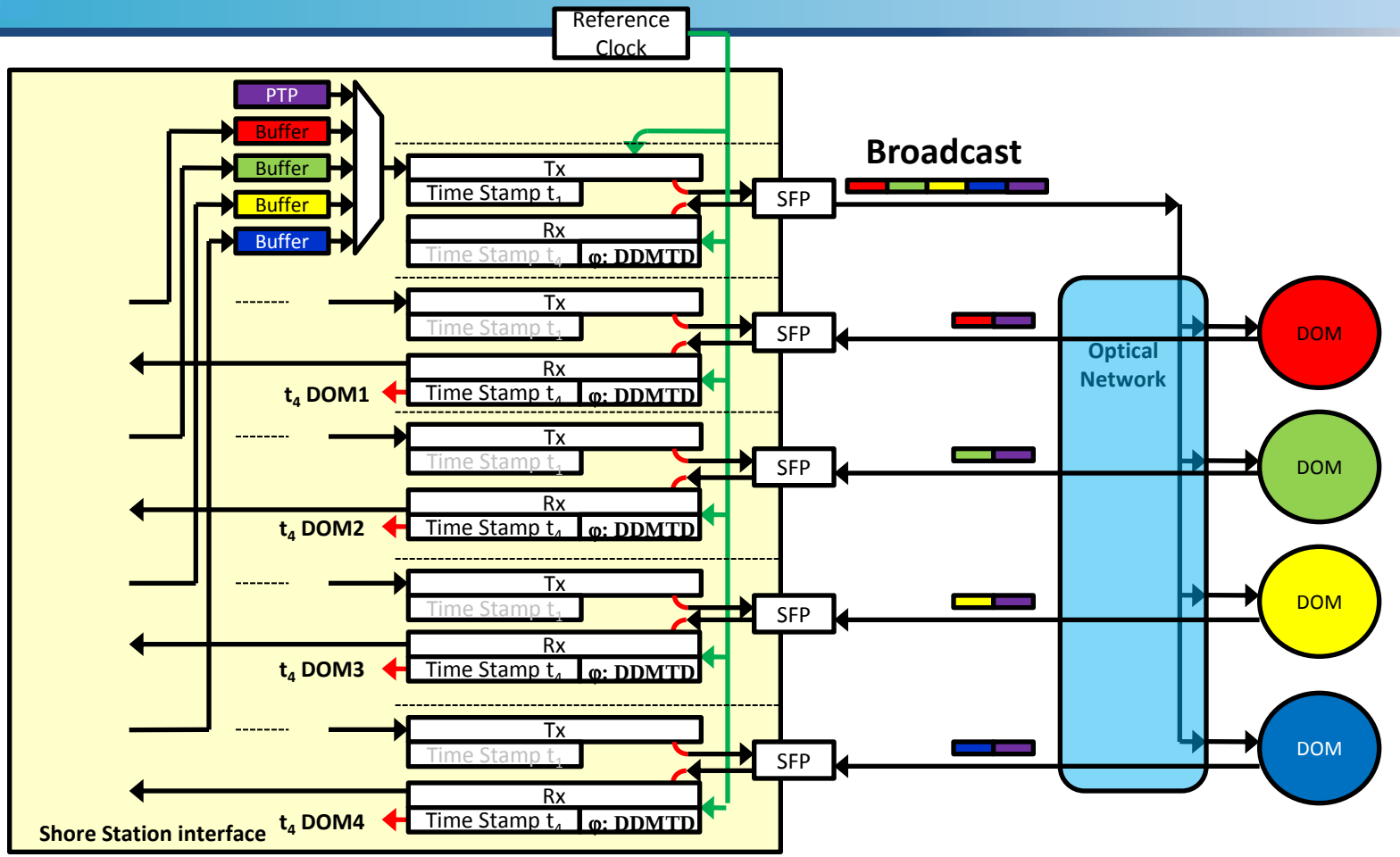


CLBv2: ARCHITECTURE : OVERVIEW



1. **Each DOM synchronizes to the absolute time (using White Rabbit)**
2. **Each DOM uses an IP address look-up table**
3. **DOMs start at an absolute point in time which was communicated via the White Rabbit protocol**

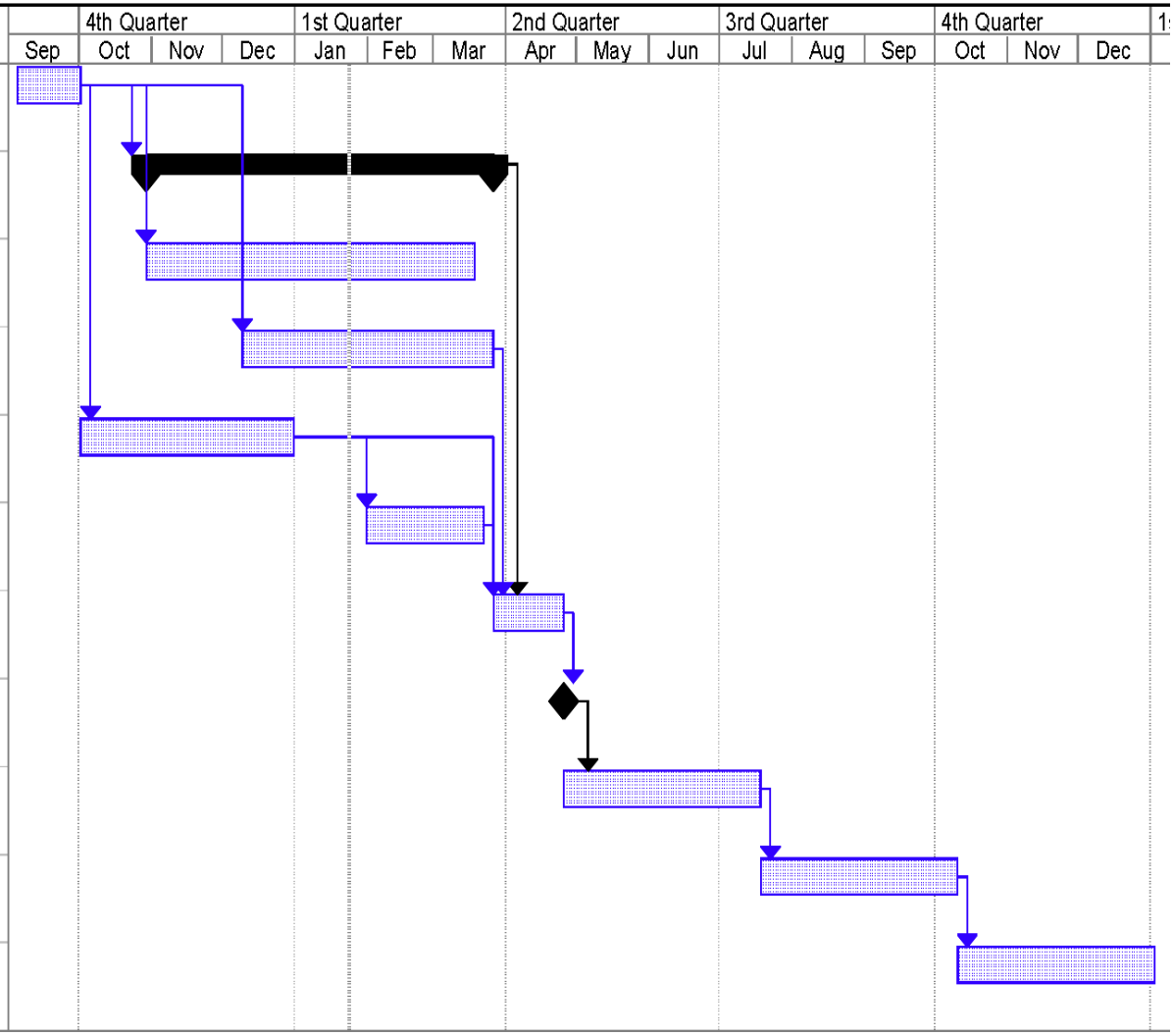
CLBv2: BROADCAST MECHANISM



1. With outgoing and incoming timestamp
2. Routing table: outgoing packets routed via broadcast
3. Ethernet flow control via broadcast
   - Direct bidirectional links would be easier; but consequences for optical network

PROVISIONAL PLANNING

ID	Task Name	Start	Finish
1	Choice FPGA/Kintex	9/5/12	10/1/12
2	**White Rabiit comm.**	**10/30/12**	**3/26/13**
3	Firmware	10/30/12	3/18/13
4	Soft PII board	12/10/12	3/26/13
5	TDC firmware	10/2/12	12/31/12
6	Multiplexer	2/1/13	3/22/13
7	Integration	3/27/13	4/25/13
8	Integration milestone	4/25/13	4/25/13
9	Prototype Design	4/26/13	7/18/13
10	Layout and production	7/19/13	10/10/13
11	Test CLB proto	10/11/13	1/2/14



SEAFLOOR INSTRUMENTATION

Work in progress on instrumentation inventory

Study use of evaluation board for prototype

However:

- Effect on optical network to be studied
- Firmware development not far enough yet
- More manpower needed …

CLBv2: SVN Repository

A SVN repository exists for the CLBv2 development ✓

Access via https or ssh:

https://isvn.ific.uv.es/repos/KM3NeT

For:

- Hardware
- Firmware
- Embedded software
- On-shore software

CLBv2: Seven Solutions

On the Madrid White Rabbit workshop appeared a possible collaboration between Seven Solutions (Producer of the White Rabbit Switch) and KM3NeT

Seven Solutions is interested in developing the hardware for the CLBv2

It seems the most suited framework is the **Eurostars** program:

- 7S (www.sevensols.com) together with another potential European enterprise partner (SME intensive in research ~ 10 % budget in research) would apply to the Eurostarts program for implementing a board with White Rabbit protocol and based on Kintex 7 (To produce the hardware for the CLBv2). 50 % funds provided by the EU.
  - The partner can be either an electronics manufacturer or a software developer. At the moment S7 is looking for a possible partner
  - The dead line for the application is the **3th April**

By end February there will take place a meeting between the Spanish Center for the development of Industrial technology (CDTI) and Seven Solutions to see the best way to canalize the application to the Eurostars program

Also a meeting between CLBv2 responsible persons, KM3NeT management and Seven Solutions would be interesting to organize this possible cooperation

CLB: SUMMARY

- A complete functional CLB is ready (PP-DOM)
- 4 CLBs has been produced (PP-DU). One of them tested satisfactory in Saclay. A CLB test bench will be soon operative in Valencia and the other two PP-DU CLB will be tested.
- The upgrade of the current CLB is on the way
  - A functional upgraded CLB should be expected by beginning 2014