#### Monte Carlo study of a Micromegas ECAL

Max & Jean, October 3<sup>rd</sup> 2012

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# Simulation study

#### Geometry

Active: 2.5 mm Ar Passive: 2.5 mm W + 1 mm of PCB (PCB = epoxy + glass fiber + 10% Cu)

40 layers (40 x 0.6 = 24 cm)

Transverse area 40 x 40 cm<sup>2</sup>

#### Readouts

Analogue: deposited energy

Digital:

- pad of 1 x 1 cm2;
- pad of 0.5 x 0.5 cm2;
- pad of 0.25 x 0.25 cm2;



Data sets: 1000 events

Energy range 5-50 GeV, every 5 GeV

Magnetic field (perp. beam dir.) 0-5 Tesla, evergy 1 T

Energy cut = 15 eV (ionisation potential of the gas)

# (MC) Event display



5 GeV

20 GeV

50 GeV

#### Response



Analogue readout shows best linearity Pure digital non-linear  $\rightarrow$  should improve with more than 1 threshold

## Energy resolution



Analogue readout provides lowest constant term, comparable to Si/W ECAL With a digital readout, the resolution improves with smaller pads

The stochastic term in the gas geometry is much larger than in the Si geometry This is expected because the sampling is different

Si/W ECAL test beam yields: a = 16.5 % and b = 1.14

## Longitudinal profile



Longitudinal energy profile of electron showers

With 40 layers, negligible leakage up to 50 GeV (higher energies to be simulated)

But 40 layers makes a thick ECAL (24 cm)  $\rightarrow$  effect of smaller number of planes on response?

### Number of layers



Less signal and more fluctuations due to increased leakage.

Above 30 layers, the resolution is almost independent on the number of layer up to 50 GeV. (Reminder: leakage correction may be applied)

#### Radial distribution



From right plot, the Moliere radius (90%) is 4.5 cm. Quite larger than in W only (0.8 cm) But can be reduced by increasing the offline threshold.

### Possible R&D in 2013

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Design : Re-use actual PCB design as much as possible \rightarrow ASU
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With a radius of 8 cm, the lateral energy containment is 98% \rightarrow ASU of 16x16 cm2
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Baseline cell size for ECAL is 5 mm

\rightarrow 16x16x4 = 1024 channels \rightarrow 16 ASIC \rightarrow How many chips are left from 2012?
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Space constrains on PCB:
16 ASIC over 256 cm2 \rightarrow 4x4 cm2 / ASIC \rightarrow Reduce package size
Any room left for passive protections? \rightarrow resistive layer?
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Open questions:
Where to get the W? \rightarrow start to collaborate with CERN/CLIC group?
What gap size? 3? 2? 1?
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#### **Prototypes and tests**

Limited funds  $\rightarrow$  at least 2 ASUs Linearity from longitudinal profiles @ DESY (electron beam up to 5 GeV) Effect of the gas mixture (Z) on linearity (He, Ne, Ar) Digital and analogue readout