DVCS 12GeV meeting electronics part

12 & 13 november 2012

Orsay (France)

Magne Magali - LPC Clermont

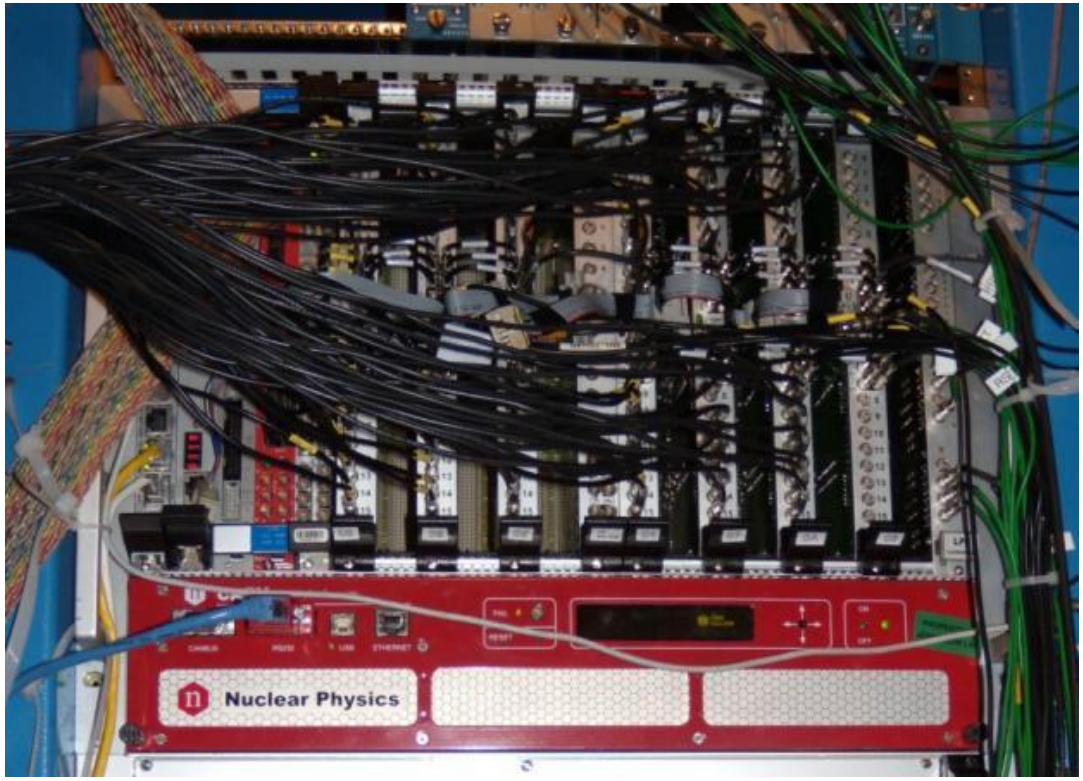
Summary

Summary

- ✓ ARS
- ✓ Trigger
  - ✓ Status
  - ✓ Upgrades

Acquisition part

- Remember … 2010
  - 2 crates with 6 and 7 ARS boards

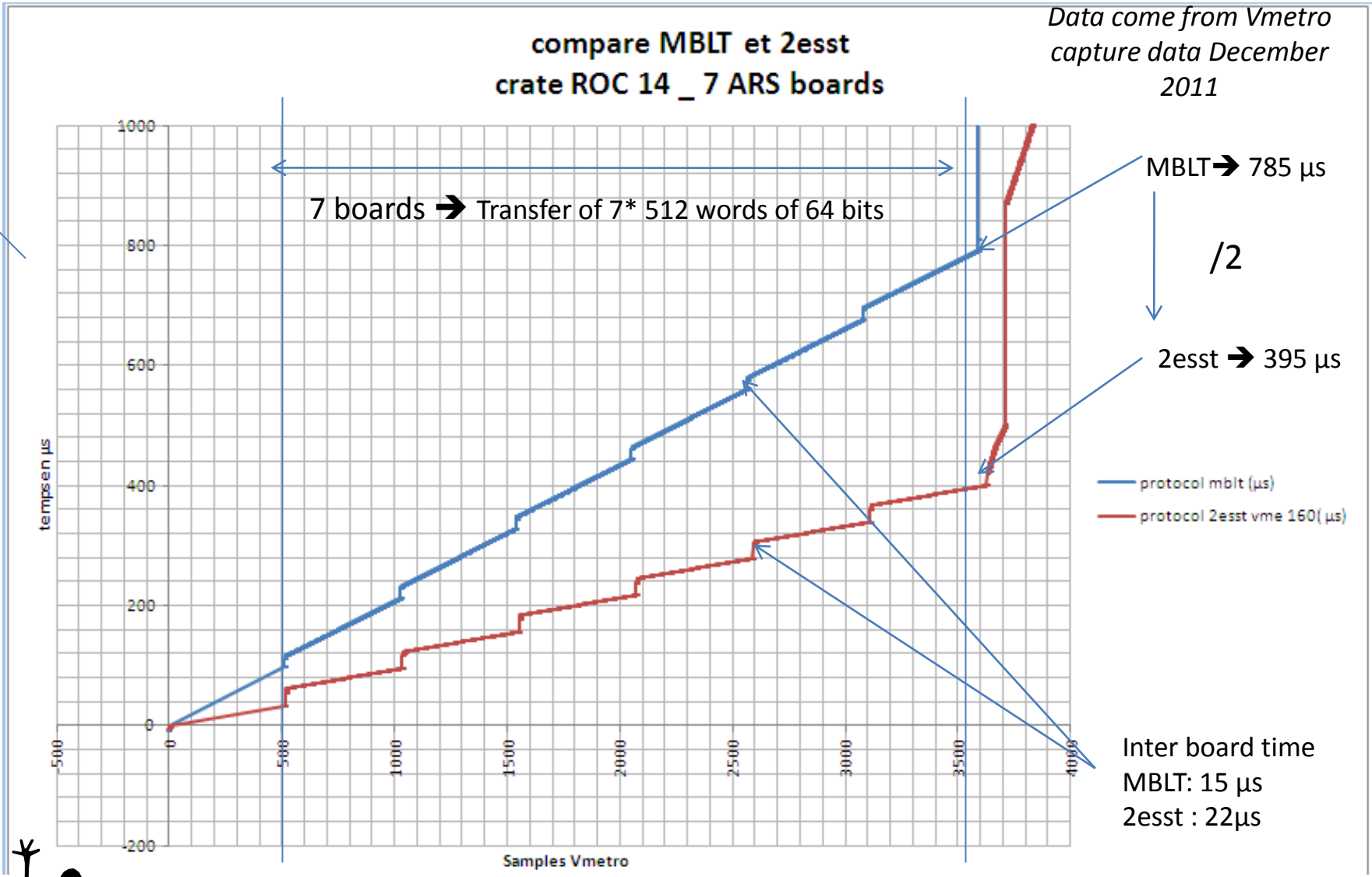


ARS

ARS16VME64

- ✓ Status:
  - ✓ 128 ns sampling by step of 1ns at each valid trigger
  - ✓ Readout VME with the protocol Vme2esst160
    - ✓ With the last Ben firmware (thanks to him)
    - ✓ The data acquisition rate has been increased (see next slide)
  - ✓ 13 boards have been used in two VME crates
- ✓ Upgrade:
  - ✓ Nothing in study

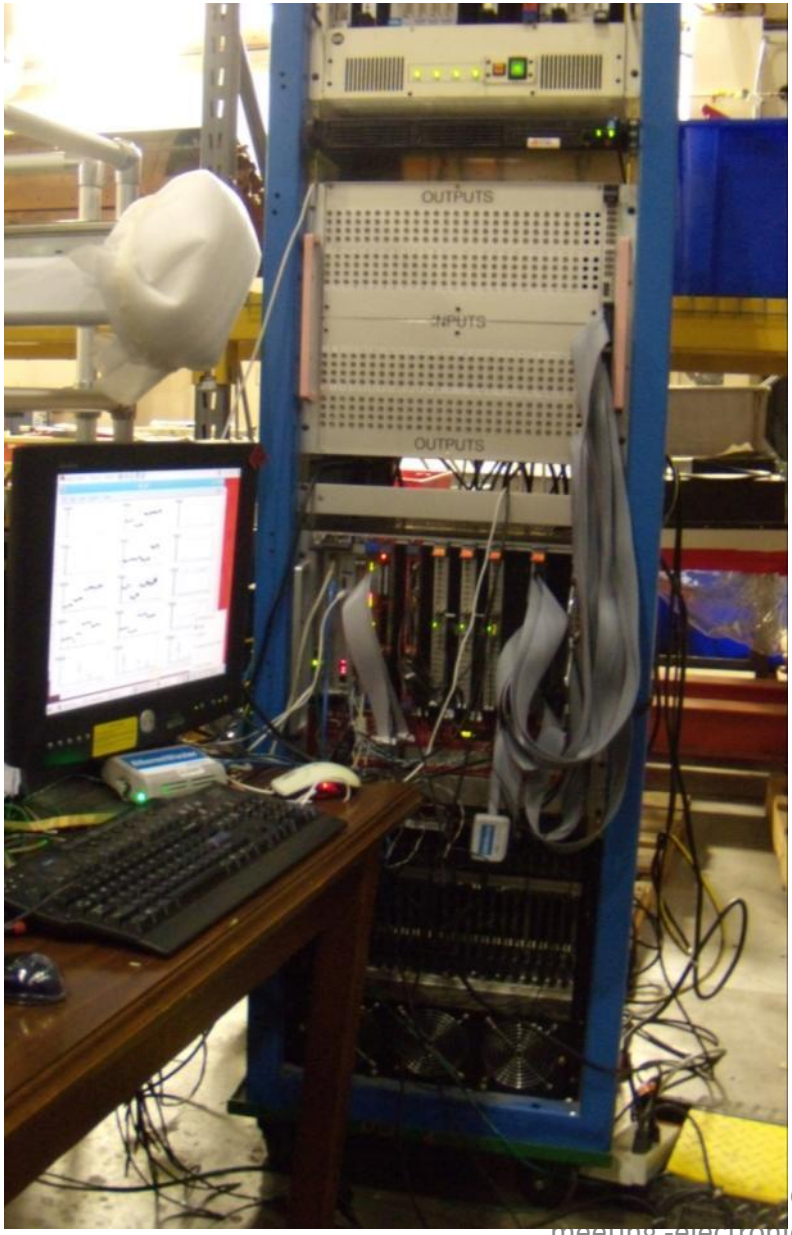
ARS16VME64- acquisition results



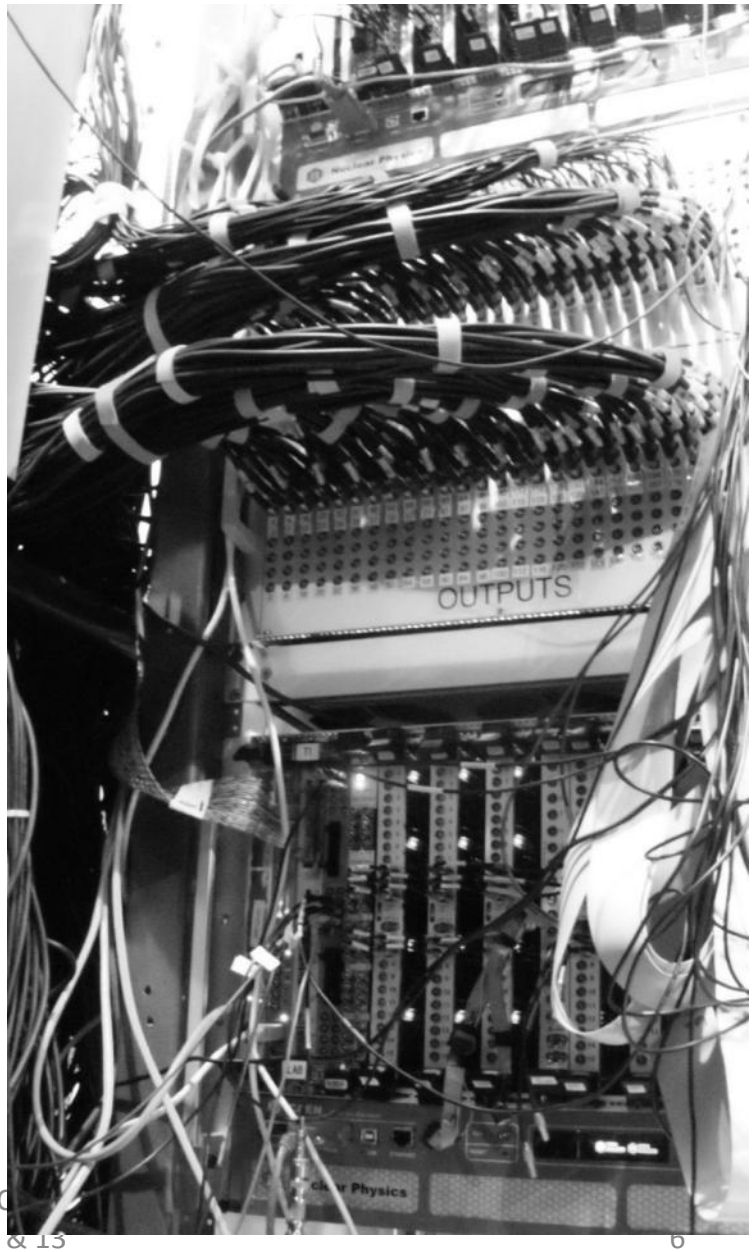
Inter board time
MBLT: 15 µs
2esst : 22µs

The acquisition time has been reduced .
Only the inter boards time can be reduced now

Test lab end of June 2010



Hall A of October 2010



The Trigger

- The goal of the trigger is to make a fast decision, for the data acquisition of the ARS boards for the memorization or the rejection of an event.
- For this purpose each signal is :
  - integrated during a gate of 60 ns
  - digitalized with a 12 bits ADC
  - Summed by clusters of 4 neighbors
  - Compared to a threshold
- The validation must be obtained after about 500 ns

Data transfer – design story (before 2010)

- For technical reasons the numeric data don't arrive in the same place.
- The technical choice is 3 FPGAs to receive the 208 ADC data , but this choice needs to add interconnection bus to transmit the data to do all the possible clusters.
- Each FPGA receives one part of all the data,
  - makes a global sum of these data and of all clusters of 4 possible neighbors
  - compares it to a programmable threshold
  - Transmits the neighbors data needed to the others FPGA.
- The goal of this system is to have a faster result of the clusters sum and / or the total sums

The ADC values needed to do the clusters sum neighbor to 2 FPGA, use only 9 of the 12 bits of the original value (the less significant bits are set by default at one).

This thing happens because of the low size of the interconnection bus between the different FPGA.

The result is : you can take a decision with a value of the real cluster sum lower than the threshold.

Calorimeter versus cluster

14	29	44	59	74	89	104	119	134	149	164	179
13	28	43	58	73	88	103	118	133	148	163	178
12	27	42	57	72	87	102	117	132	147	162	177
11	26	41	56	71	86	101	116	131	146	161	176
10	25	40	55	70	85	100	115	130	145	160	175
9	24	39	54	69	84	99	114	129	144	159	174
8	23	38	53	68	83	98	113	128	143	158	173
7	22	37	52	67	82	97	112	127	142	157	172
6	21	36	51	66	81	96	111	126	141	156	171
5	20	35	50	65	80	95	110	125	140	155	170
4	19	34	49	64	79	94	109	124	139	154	169
3	18	33	48	63	78	93	108	123	138	153	168
2	17	32	47	62	77	92	107	122	137	152	167
1	16	31	46	61	76	91	106	121	136	151	166
0	15	30	45	60	75	90	105	120	135	150	165

The status of the precision of the all the clusters is :

In green : 147/ 180 - (81,6%) of the case.

➔ no incertitude of the result

In blue : 3 /180 - (1,67%) of the case .

➔ the incertitude can be 7 lsb max under the threshold

In purple : 27 /180 - (15%) of the case .

➔ the incertitude can be 14 lsb max under the threshold

In red : 3 /180 - (1,67%) of the case .

➔ the incertitude can be 21 lsb max under the threshold

Interconnection bus

BEFORE → NOW

- It's a 36 bits bus :
  - At each clock cycle it permits to transfer 9 of the 12 bits for the ADC data.
  - Result : a non precise result for some clusters sums

- It's now a 78 bits bus .
  - All 12 bits of the ADC data is transmitted
- Only 48 bits is necessary for this transfer.
  - The other bits can be used to transfer some new data (see slide , new option)

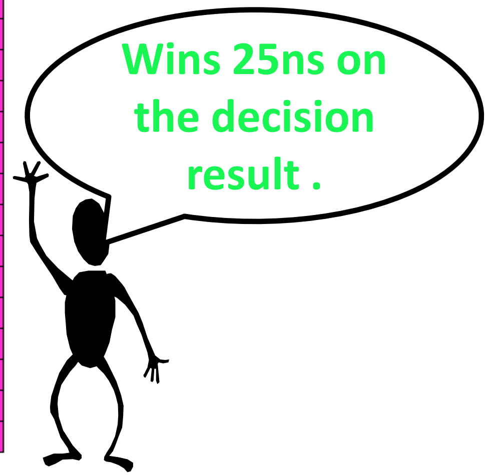
Solves the incertitude of the clusters decision

Calorimeter view by the FPGAs

BEFORE → NOW

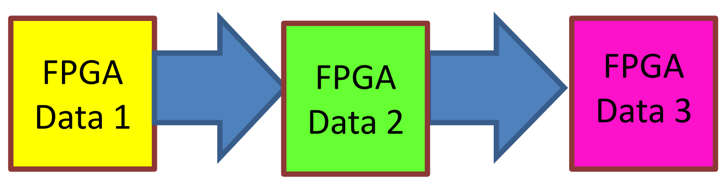
BEFORE

15	31	47	63	79	95	111	127	143	159	175	191	207
14	30	46	62	78	94	110	126	142	158	174	190	206
13	29	45	61	77	93	109	125	141	157	173	189	205
12	28	44	60	76	92	108	124	140	156	172	188	204
11	27	43	59	75	91	107	123	139	155	171	187	203
10	26	42	58	74	90	106	122	138	154	170	186	202
9	25	41	57	73	89	105	121	137	153	169	185	201
8	24	40	56	72	88	104	120	136	152	168	184	200
7	23	39	55	71	87	103	119	135	151	167	183	199
6	22	38	54	70	86	102	118	134	150	166	182	198
5	21	37	53	69	85	101	117	133	149	165	181	197
4	20	36	52	68	84	100	116	132	148	164	180	196
3	19	35	51	67	83	99	115	131	147	163	179	195
2	18	34	50	66	82	98	114	130	146	162	178	194
1	17	33	49	65	81	97	113	129	145	161	177	193
0	16	32	48	64	80	96	112	128	144	160	176	192



NOW

15	31	47	63	79	95	111	127	143	159	175	191	207
14	30	46	62	78	94	110	126	142	158	174	190	206
13	29	45	61	77	93	109	125	141	157	173	189	205
12	28	44	60	76	92	108	124	140	156	172	188	204
11	27	43	59	75	91	107	123	139	155	171	187	203
10	26	42	58	74	90	106	122	138	154	170	186	202
9	25	41	57	73	89	105	121	137	153	169	185	201
8	24	40	56	72	88	104	120	136	152	168	184	200
7	23	39	55	71	87	103	119	135	151	167	183	199
6	22	38	54	70	86	102	118	134	150	166	182	198
5	21	37	53	69	85	101	117	133	149	165	181	197
4	20	36	52	68	84	100	116	132	148	164	180	196
3	19	35	51	67	83	99	115	131	147	163	179	195
2	18	34	50	66	82	98	114	130	146	162	178	194
1	17	33	49	65	81	97	113	129	145	161	177	193
0	16	32	48	64	80	96	112	128	144	160	176	192



FPGA1 to FPGA2

19 ADC values => 5 clock cycles

FPGA2 to FPGA3

16 ADC values => 4 clock cycles

FPGA1 to FPGA2

16 ADC values => 4 clock cycles

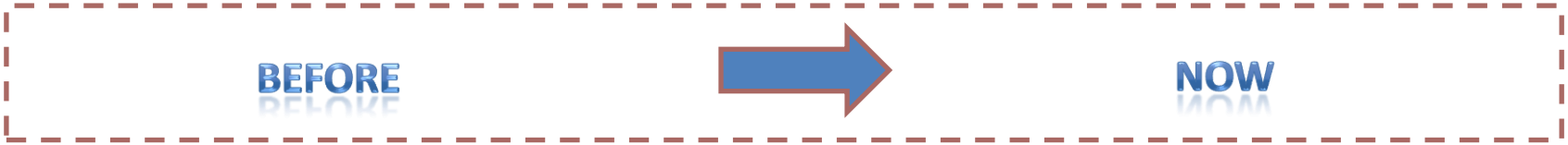
FPGA2 to FPGA3

16 ADC values => 4 clock cycles

☹ **Impossible to reduce more this time**

Adding functionalities

External Inputs/Outputs



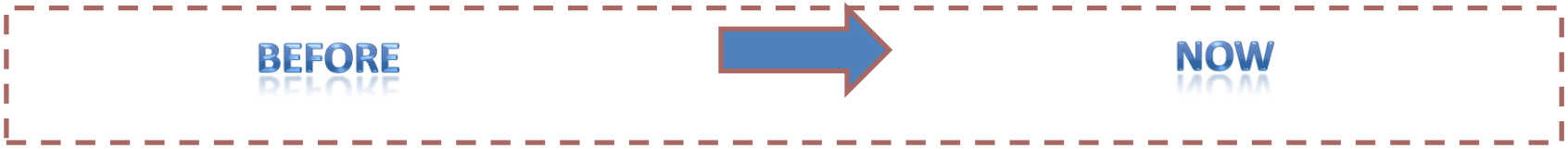
- The IO are using NIM format:
  - 12 inputs
  - 8 outputs
- All the IO have been used during the experiment.

- The number of IO has been increased :
  - 16 NIM inputs
  - 16 NIM outputs
- a new format of signals has been added:
  - 4 ECL inputs
  - 4 ECL outputs

The old IO has the same place of the previous.

The new IO has needed the design of two new small electronic boards with a compatible format of the daughter board.

Logic unit –control part

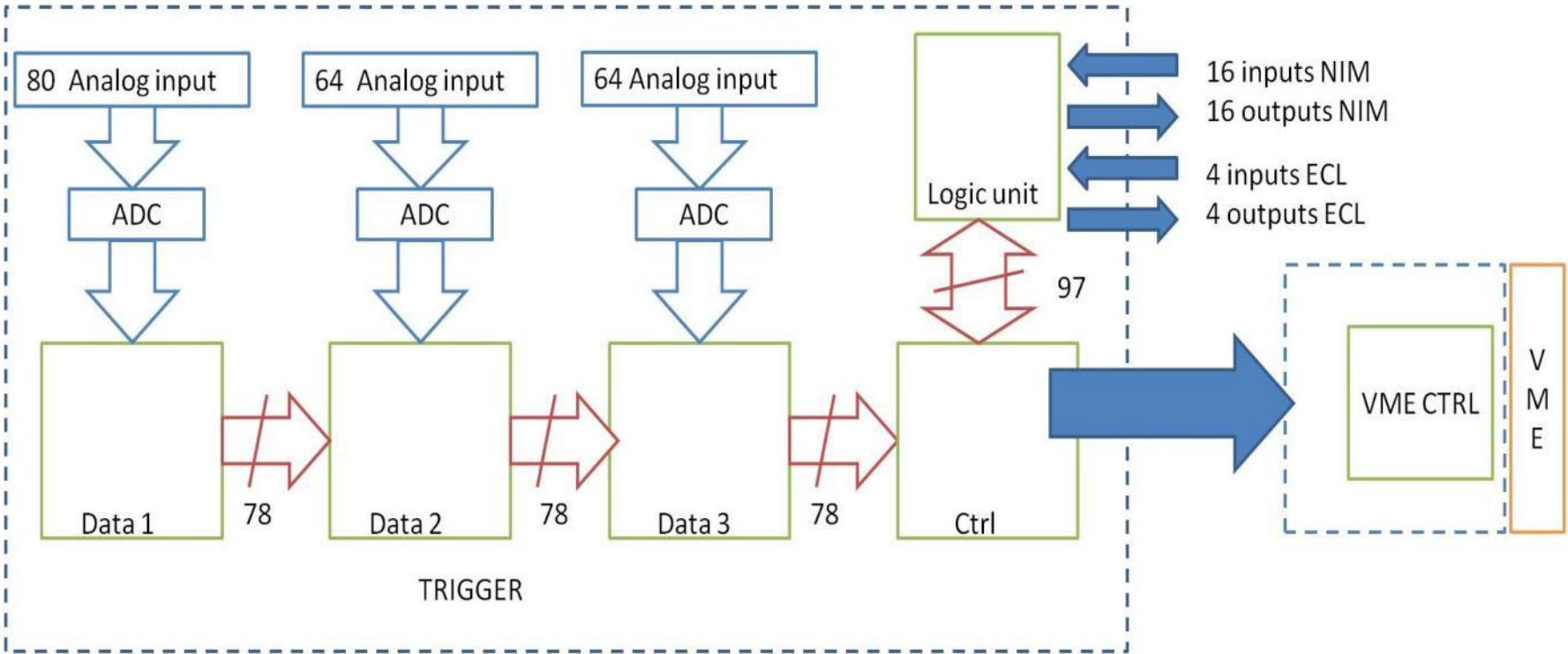


Before :

-the logic unit part and the control part are in the same FPGA

Now :

- each part has is own FPGA.



Adding functionalities

New trigger philosophy acquisition

Goal

Reduce the acquisition time

Calorimeter versus ARS boards and crate

ARS CRATES → **CALORIMETER**

crate hight (1)

		$05	$09	$02	$04	$07	$0A	$03
	0	8	40	72	104	136	168	192
	1	12	44	76	108	140	172	196
	2	26	58	90	122	154	186	200
	3	30	62	94	126	158	190	204
	4	9	41	73	105	137	169	193
	5	13	45	77	109	141	173	197
	6	27	59	91	123	155	187	201
	7	31	63	95	127	159	191	205
	8	10	42	74	106	138	170	194
	9	14	46	78	110	142	174	198
	10	24	56	88	120	152	184	202
	11	28	60	92	124	156	188	206
	12	11	43	75	107	139	171	195
	13	15	47	79	111	143	175	199
input:	14	25	57	89	121	153	185	203
ARS	15	29	61	93	125	157	189	207

crate low(2)

		$01	$06	$0D	$0E	$0F	$08	
	0	0	32	64	36	128	160	
	1	4	36	68	100	132	164	
	2	18	50	82	114	146	178	
	3	22	54	86	118	150	182	
	4	1	33	65	97	129	161	
	5	5	37	69	101	133	165	
	6	19	51	83	115	147	179	
	7	23	55	87	119	151	183	
	8	2	34	66	98	130	162	
	9	6	38	70	102	134	166	
	10	16	48	80	112	144	176	
	11	20	52	84	116	148	180	
	12	3	35	67	99	131	163	
	13	7	39	71	103	135	167	
input:	14	17	49	81	113	145	177	
ARS	15	21	53	85	117	149	181	

15	31	47	63	79	95	111	127	143	159	175	191	207
14	30	46	62	78	94	110	126	142	158	174	190	206
13	29	45	61	77	93	109	125	141	157	173	189	205
12	28	44	60	76	92	108	124	140	156	172	188	204
11	27	43	59	75	91	107	123	139	155	171	187	203
10	26	42	58	74	90	106	122	138	154	170	186	202
9	25	41	57	73	89	105	121	137	153	169	185	201
8	24	40	56	72	88	104	120	136	152	168	184	200
7	23	39	55	71	87	103	119	135	151	167	183	199
6	22	38	54	70	86	102	118	134	150	166	182	198
5	21	37	53	69	85	101	117	133	149	165	181	197
4	20	36	52	68	84	100	116	132	148	164	180	196
3	19	35	51	67	83	99	115	131	147	163	179	195
2	18	34	50	66	82	98	114	130	146	162	178	194
1	17	33	49	65	81	97	113	129	145	161	177	193
0	16	32	48	64	80	96	112	128	144	160	176	192

For clusters of 4 neighbors.

You have 1 to 4 boards touch (but 2 in each crate).
The reading time can be reduces

BEFORE AND NOW → **FUTUR ???**

- ✓ 13 ars boards
  - ✓ 1 trigger
- ✓ 1 acquisition cycle :
  - ✓ 7 borads in 2esst ➔ 395 µs
  - ✓ dead time of ARS : 128 us

- ✓ 13 ars boards
  - ✓ 13 individual triggers
- ✓ 1 acquisition cycle :
  - ✓ Min : 1boards in 2esst
    - ➔ 57 µs in 1 crate
  - ✓ Max : 2 boards in 2esst
    - ➔ 130 µs per crates.