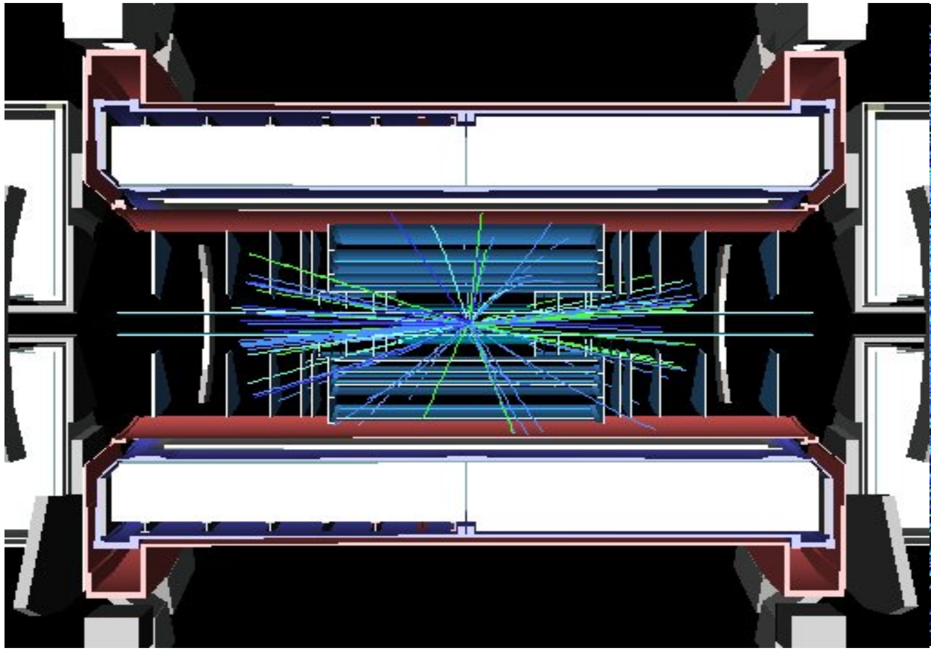
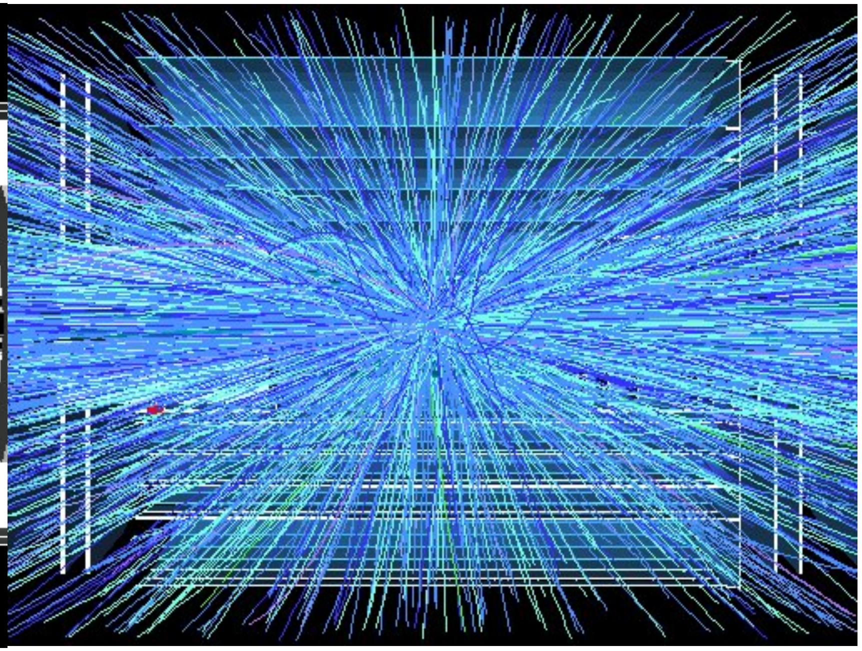
# The ATLAS tracker upgrade towards the SLHC era



5 Collisions (0.2 x $10^{34}$ $cm^{-2}$ $s^{-1}$)



400 Collisions ($10^{35}$ $cm^{-2}$ $s^{-1}$)

G.Calderini (LPNHE, Paris)

on behalf of the French Laboratories working
for this effort

LPNHE PARIS

# Why working now for the upgrade?

Every time that people think about the luminosity upgrade, there is the impression that it's a very distant phase in the future

So, why to bother with it now?

- (General answer)
  Everybody who took part to the design of an experiment knows that it takes several years (the construction and installation itself is typically 5-6 years, after the R&D and design phase is finished)
  Time flows fast!

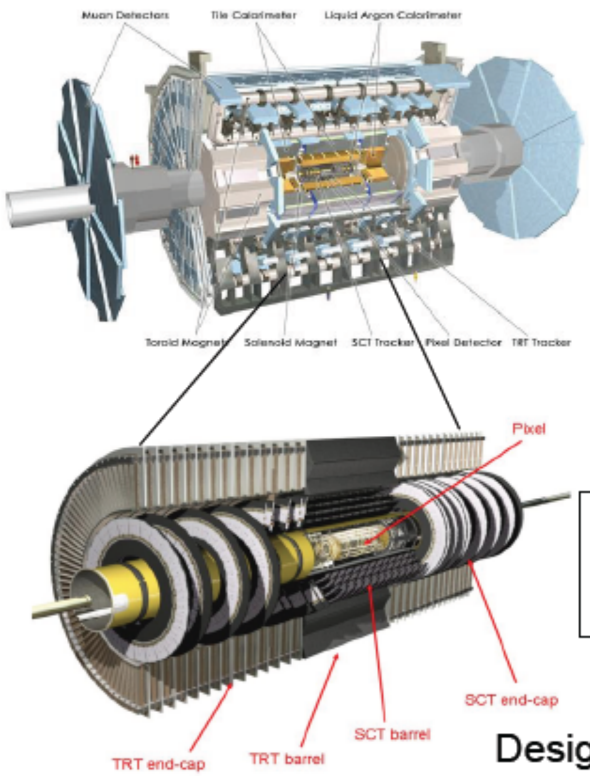
- ("Not-so-obvious-to-everybody" answer)
  LHC will not be the same between now and 2020
  Radical improvements making it impossible to run until then with the initial detector ("Phase I upgrade")

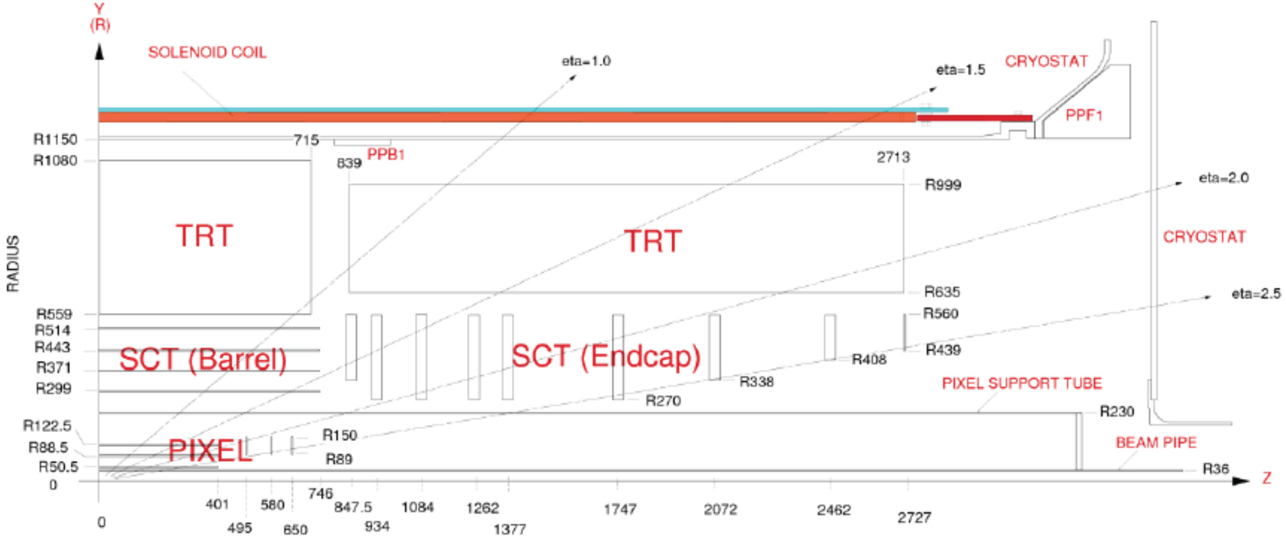
# The LHC roadmap

See talk L. Ponce

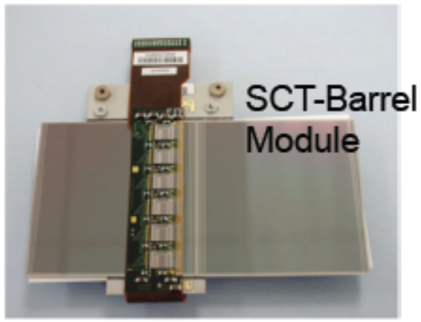
| | | | |
|---|---|---|---|
| 2009 | | LHC start-up $\sqrt{s}$ = 900GeV | |
| 2010–2012 | | $\sqrt{s}$ = 7TeV rising to 8TeV, $\mathcal{L}$= $6\times10^{33}cm^{-2}s^{-1}$, bunch spacing 50ns | ~25fb$^{-1}$ |
| 2013–2014 | LS1 | Go to design energy and nominal luminosity | |
| 2015–2017 | | $\sqrt{s}$ = 13-14TeV, $\mathcal{L}$= $1\times10^{34}cm^{-2}s^{-1}$, bunch spacing 25ns | ≥50fb$^{-1}$ |
| 2018 | LS2 | Injector and LHC Phase-I upgrade to full design luminosity | |
| 2019–2021 | | $\sqrt{s}$ = 14TeV, $\mathcal{L}$= $2\text{-}3\times10^{34}cm^{-2}s^{-1}$, bunch spacing 25ns | ≥300fb$^{-1}$ |
| 2022 | LS3 | HL-LHC Phase-II upgrade, crab cavities, new IR, ... | |
| 2023 … 2030? | | $\sqrt{s}$ = 14TeV, $\mathcal{L}$= $5\times10^{34}cm^{-2}s^{-1}$ (luminosity levelling) 25ns | ~3000 fb$^{-1}$ |

# Just a reminder of the present Silicon Tracker




| | | |
|---|---|---|
| **Pixel** | (n+-on-n sensor) : 3 barrels + 2x3 discs | (5 < R < 15cm) |
| **Strip (SCT)** | (p+-on-n sensor) : 4 layers + 2x9 discs | (30 < R < 51cm) |
| **TRT** | (straw drift tubes) : Barrel + Wheel | (55 < R < 105cm) |




Designed for fluences of :

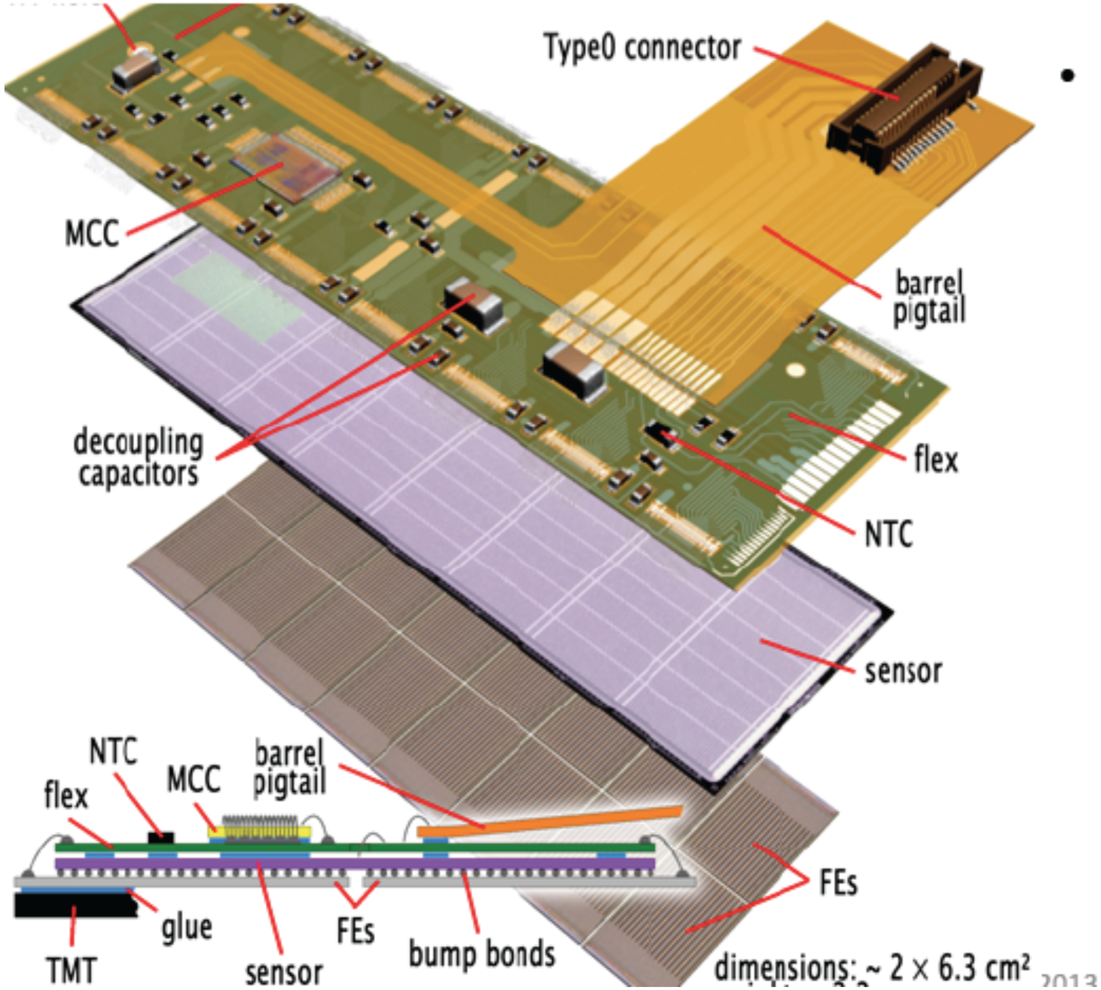
- Pixel B-layer : $1 \times 10^{15}$ 1MeV $n_{eq}/cm^2$
- SCT layer 1 : $2 \times 10^{14}$ 1MeV $n_{eq}/cm^2$
- TRT outer rad : $3 \times 10^{13}$ 1MeV $n_{eq}/cm^2$

~ 50 Mrads !

- 80M channels
- Temperature: T=-5 / -13 C by evaporative (C3F8) cooling

# A FE-I3 based pixel module

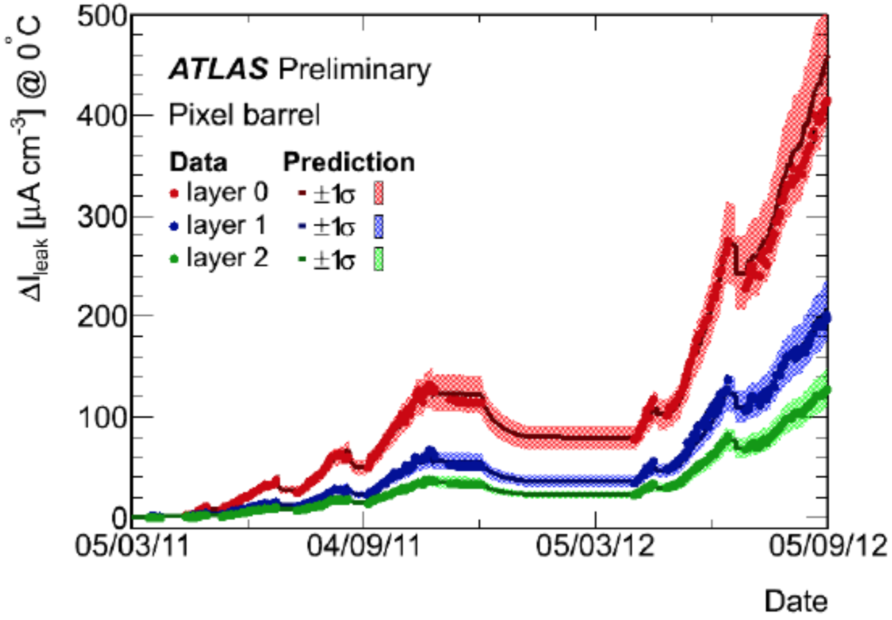
- Sensor: planar 250 µm thick n-on-n sensor
  - Typical pixel size 50 x 400 µm$^2$ (50 x 600 µm$^2$ pixels in gaps between FE chips)
  - Bias voltage 150 V (up to 600 V )



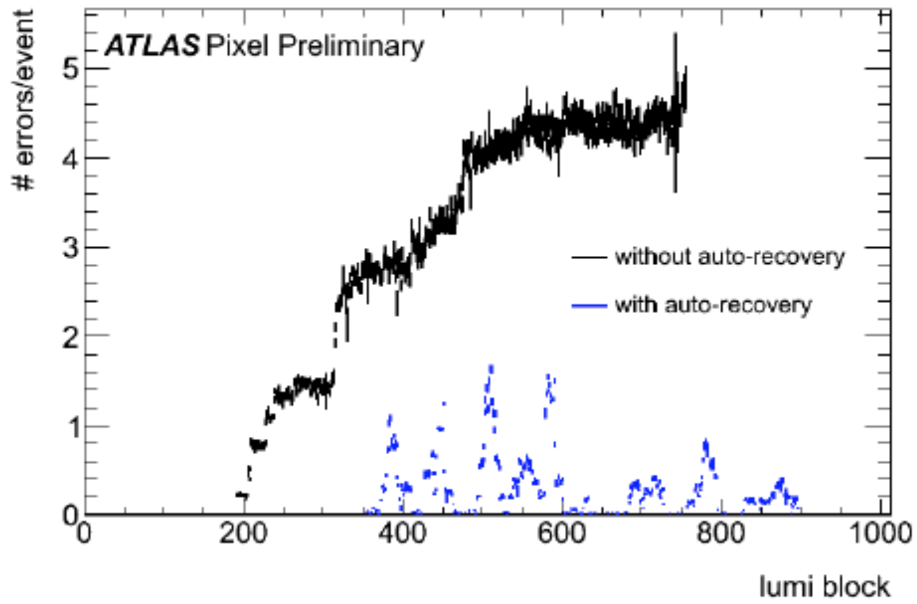

- Readout:
  - 16 FE chips, 2880 pixels each
  - 47232 (328 x 144) pixels
  - Zero suppression in the FE chip
  - Controller ( MCC ) builds module event
  - Charge measured by means of Time over Threshold
  - Data transfer 40 – 160 Mbit/s depending on layer

# First tracker upgrade: the IBL

The present tracker (especially the layer_0) will be in trouble at a certain point due to radiation damage and occupancy

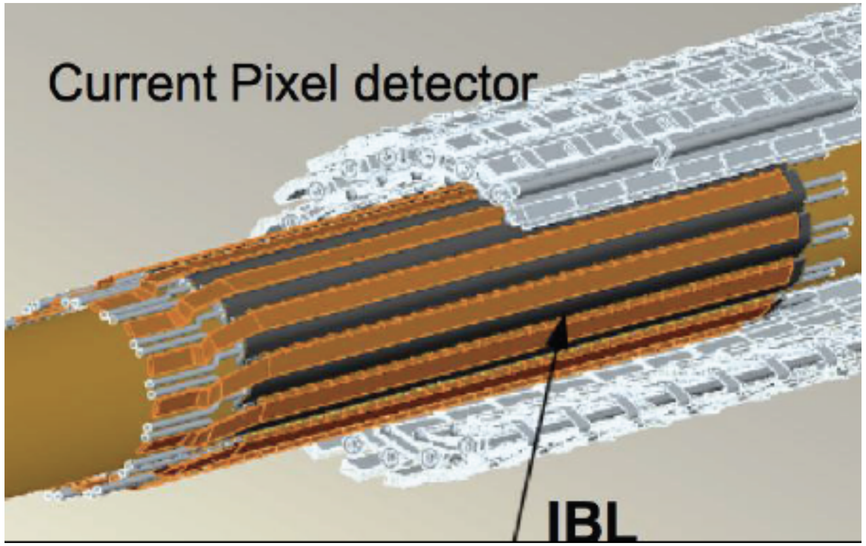


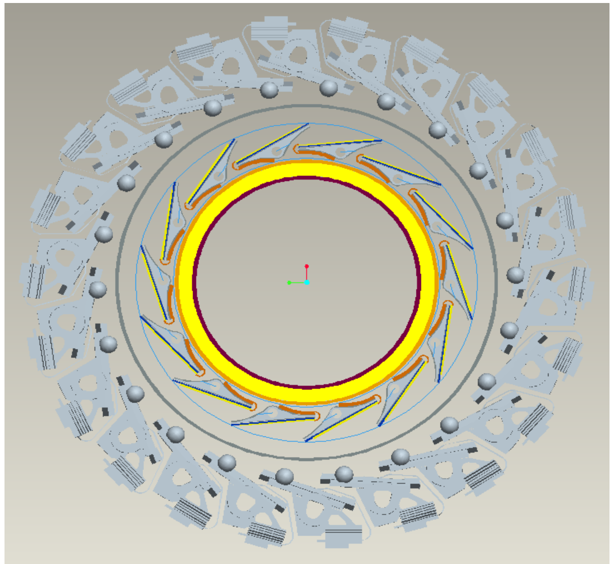

Behavior of leakage current normalized at 0C as a function of date



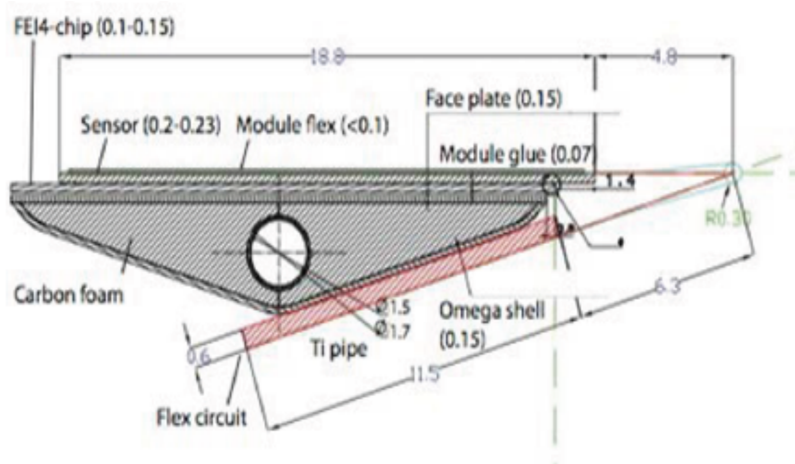

Module de-synchronizations at the beginning of each fill (FE-I3)

# The IBL: Insertable B-Layer



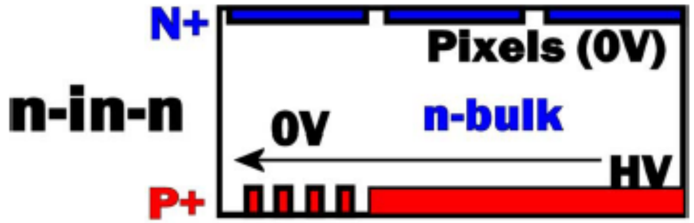
- Fourth hit in pixel tracking
- Small radius 3.3 cm  (beam pipe 2.65 cm)
- Low material budget of 1.9% X0
- Smaller segmentation (50x250 um)
- Higher dose tolerance (FE-I4, 250 Mrad)
- 14 staves with 32 FE-I4 chips per stave
- Planar n-in-n (double chips)
- 3D n-in-p (one chip) at high-eta



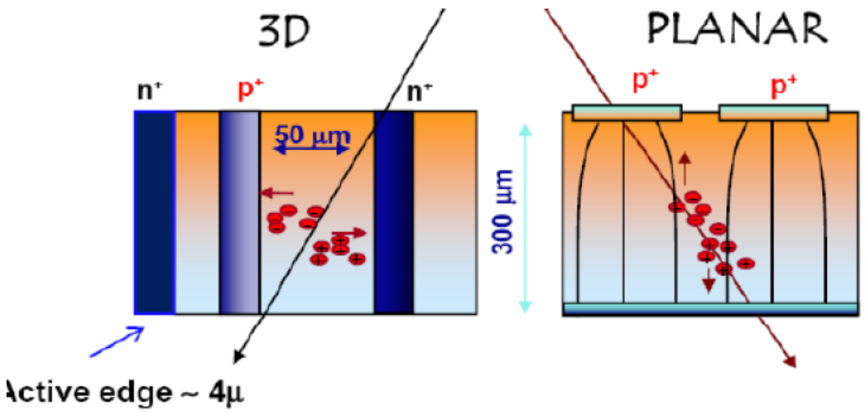
# Two sensor technologies co-exist in the IBL

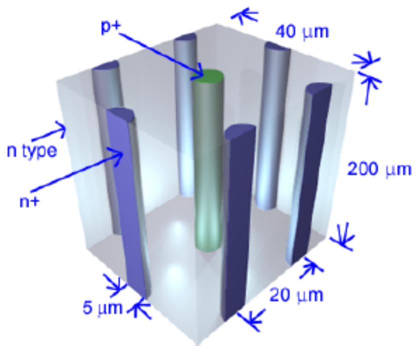
## Planar pixels n-in-n

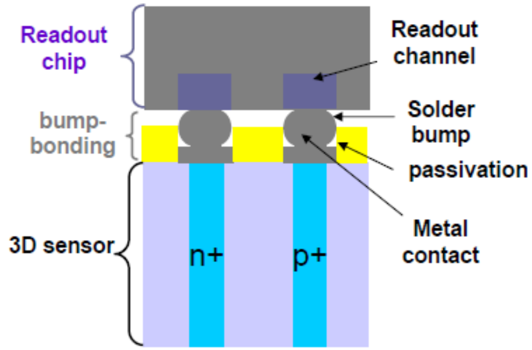
- The same technology used in the present trackers
- Well known and tested




## 3D Pixels:



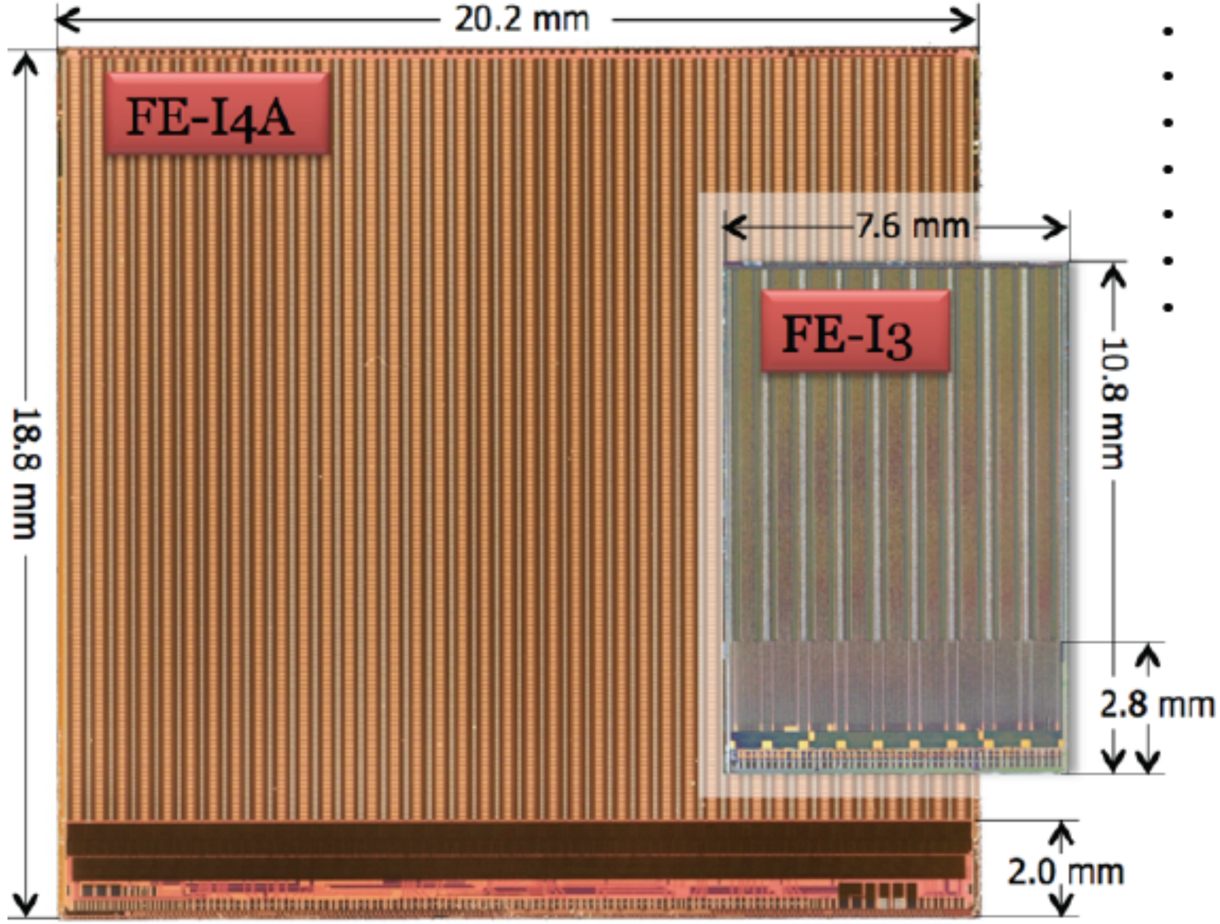




- Here the electrodes are columns passing from one face to the other
- In this way the electric field is parallel to the face of the sensor and the charge drift evolves in a few tens of um
- Intrinsically more radiation hard

# Upgraded readout electronics: the FE-I4

- Largest hybrid pixel chip in HEP 80 col x 336 rows of 50x250 μm pixels
- 26880 pixels, 80M transistors, up to 200 kHz trigger rate
- maximize active area, reduce bump bonding cost
- distributed memory, zero suppression inside pixels, small size periphery
- time-walk improved by digital treatment inside 4 pixel regions




- 130 nm CMOS
- 150 μm thickness
- Charge by 4 bits ToT
- 160 Mb/s readout
- Power 200 $mW/cm^2$
- Total dose tested up to 750 MRad
- SEU error cross-section $<10^{-15}$ $cm^2$

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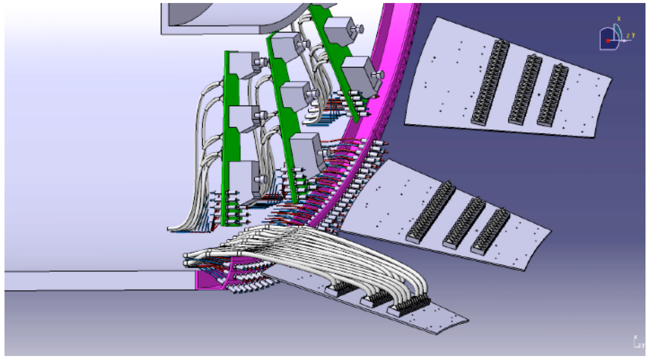
# Big French contribution in the design of services

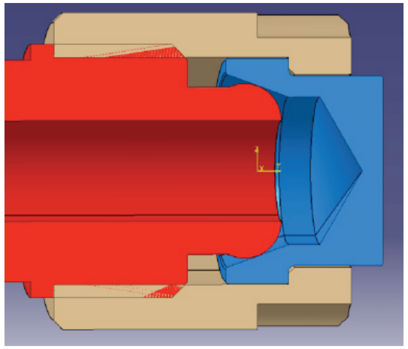
## Design of PP1 connections



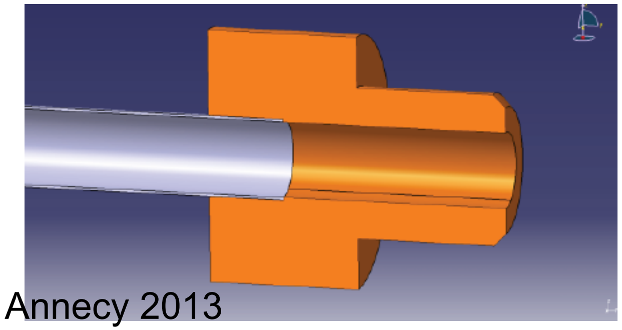
## Fittings and Ti pipes

- No industrial solution fitting the IBL envelope (and PP1!)
- Leak tight @ 20bars $CO_2$, radhard (no organic), reliable

Electron beam welding, laser welding, brazing techniques under investigation (already good results)

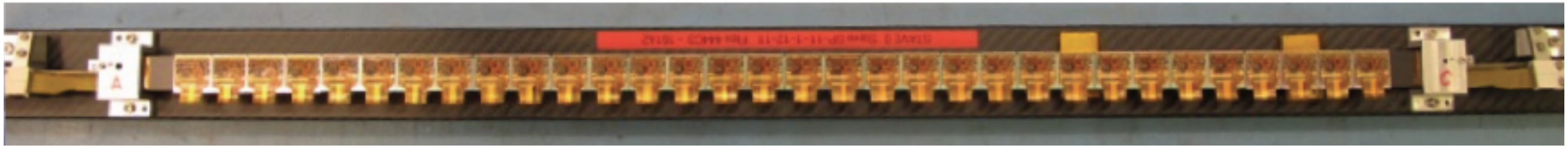


design much more relaible of the present ATLAS fitting



# IBL status

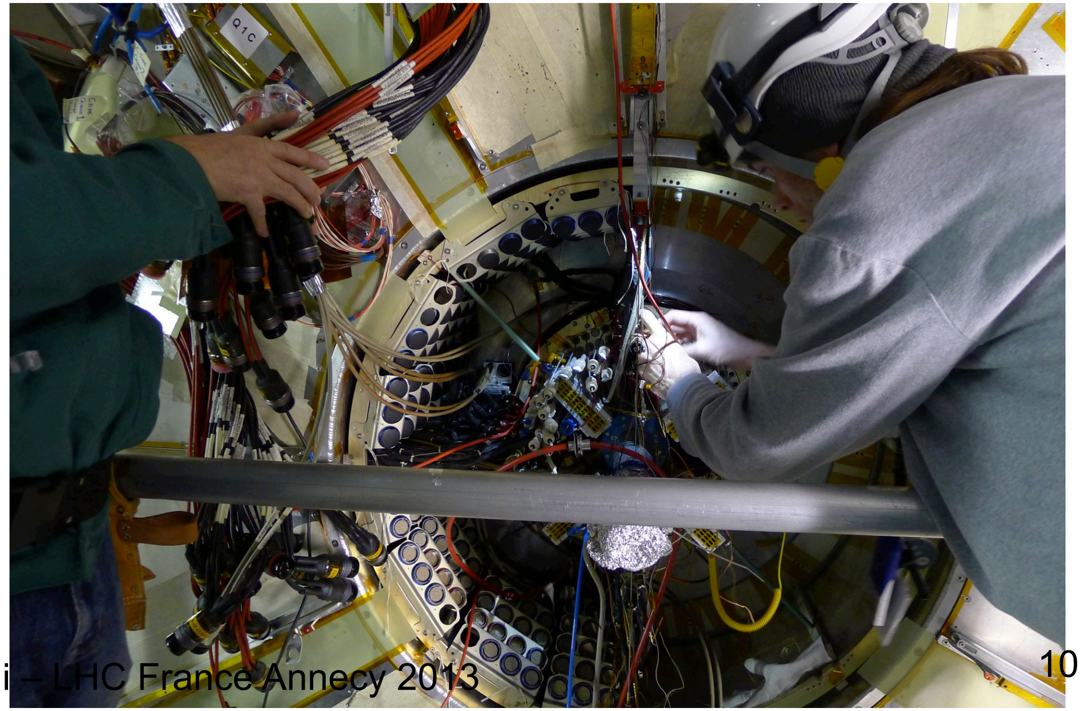
Two staves (0A and 0B) already produced and tested



Now entering 'factory' mode

Access for installation has started

Pixel detector will be brought to the surface and undergo maintenance (4% of dead modules should be hopefully repaired)



# The long-term upgade: 'Phase-II'

## Physics

- Higgs: BRs, self-coupling
- WW, ZZ scattering
- W', Z', quark substructure

## Completely new tracker (more pixels layers + strips)

- LOI in preparation for running after Phase-II (-2030, 3000 fb-1)
- Leveled luminosity of $5 \times 10^{34}$ $cm^{-2}$ $s^{-1}$
- Innermost layers should be rad-hard up to 1 Grad

## Critical R&D necessary

- Sensors
- Electronics
- Strong dependence on the general design

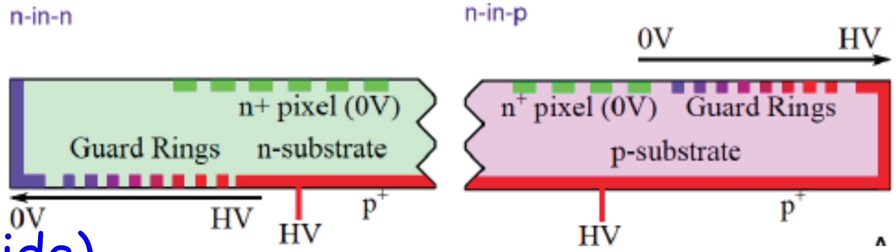
# Sensors

Need to go to radiation hard -> $2x10^{16}$
thin -> < 200 μm
cheap -> n-in-p (?), new bonding techniques ?
efficient -> reduce the inactive region at the edge

As mentioned, a big effort has been made on n-in-n and 3D pixels, already at this time for the IBL construction. This will go on.

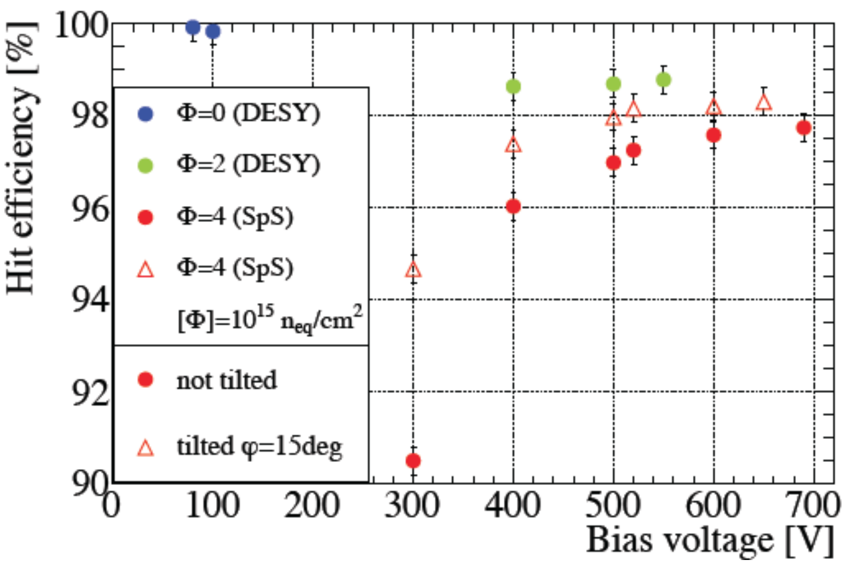
In parallel, n-in-p planar pixels are also being developed

- Promising technology
- p-type doesn't invert with dose
- cheaper (pixel and GR on the same side)

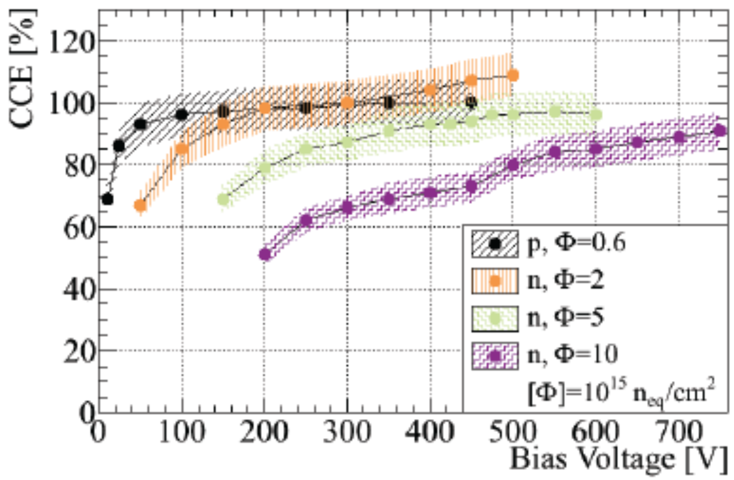



We think n-in-p will become very important in view of tracker replacement

Thin sensors to reduce the material budget and optimize the charge collection efficiency




A.Macchiolo et al, arXiv: 1210.7933



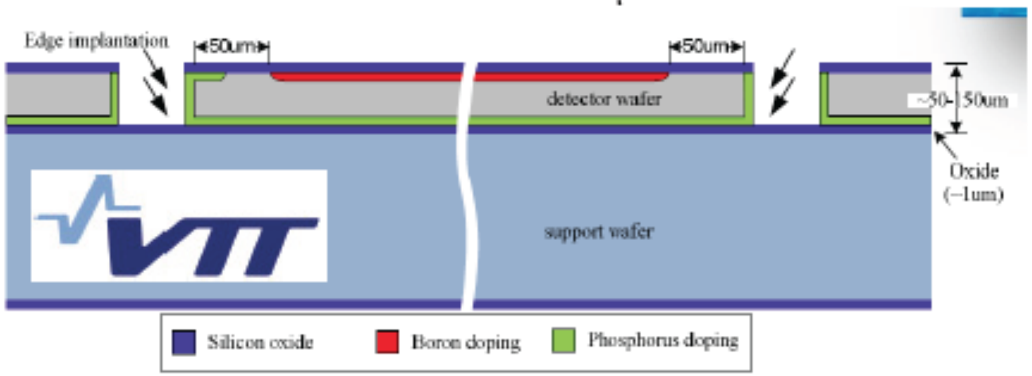

150 um n-in-p sensors

75 um n-in-p sensors

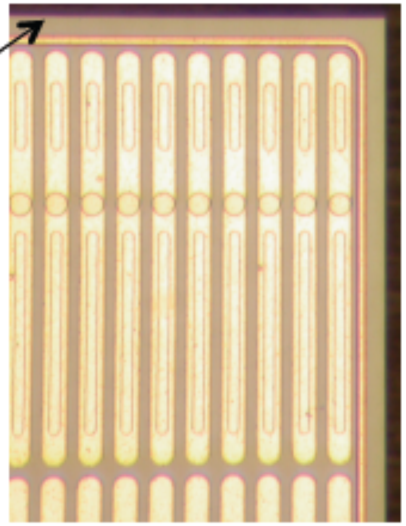
In a partial depletion regime, the undepleted region is just acting as a charge trap

# Active edge planar pixel sensors

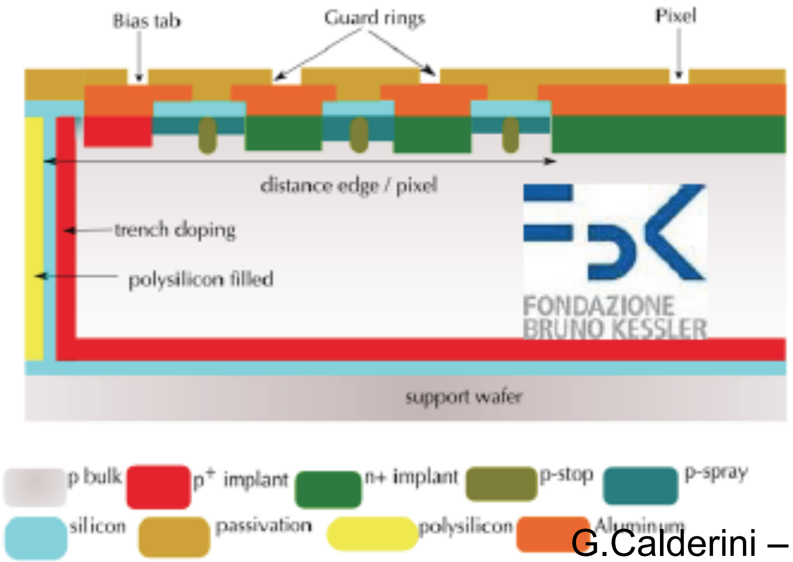
- Trench doped by four-quadrant implantation
- Sensor thickness 100-200 μm



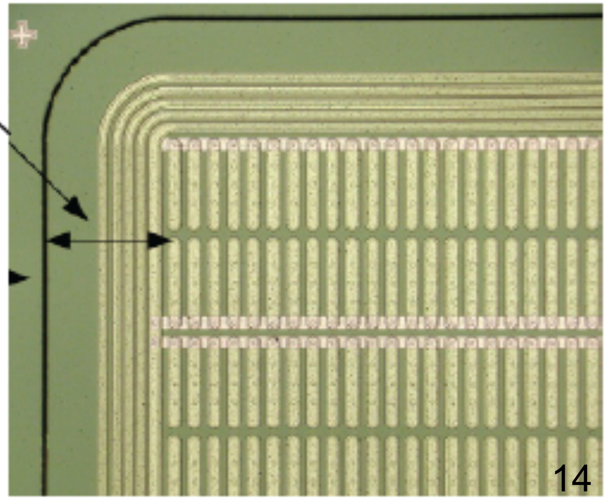

- Pixel-to-trench distance as low as 50 μm



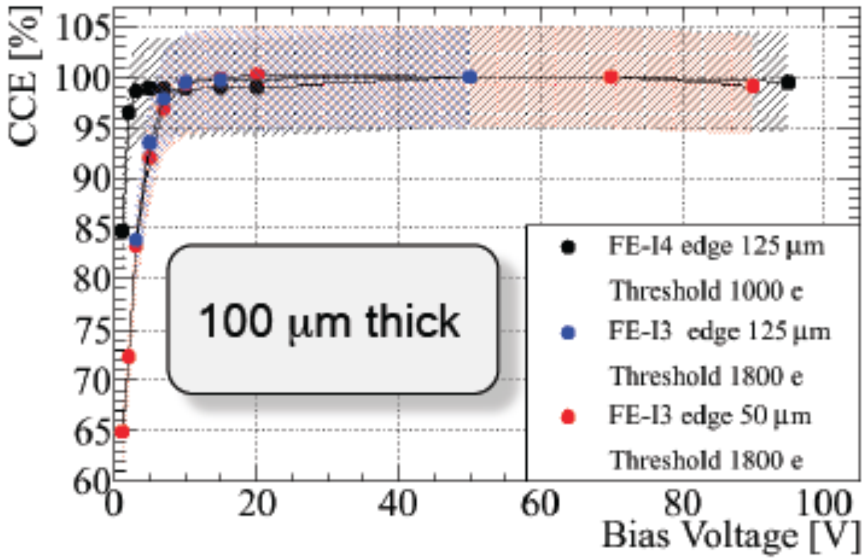
- Trench doped by diffusion
- Sensor thickness 200 μm



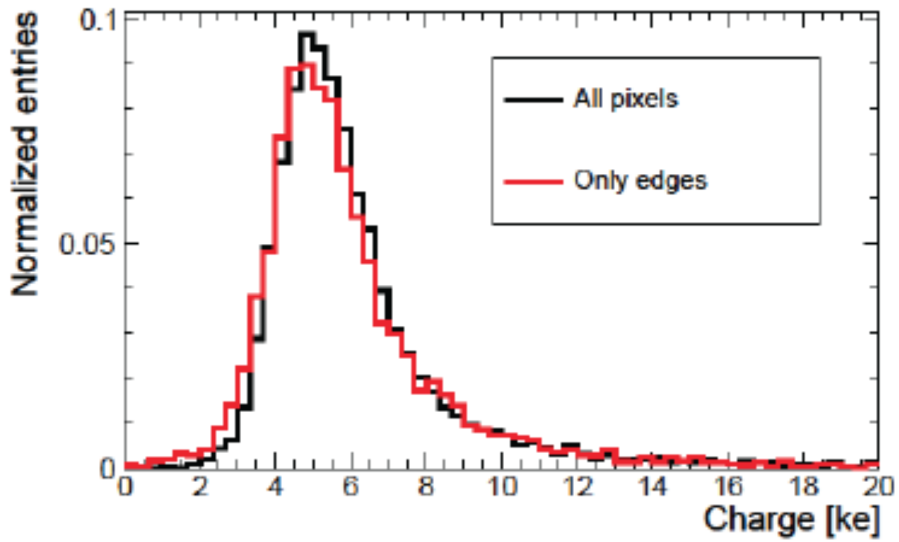

- Pixel-to-trench distance as low as 100 μm



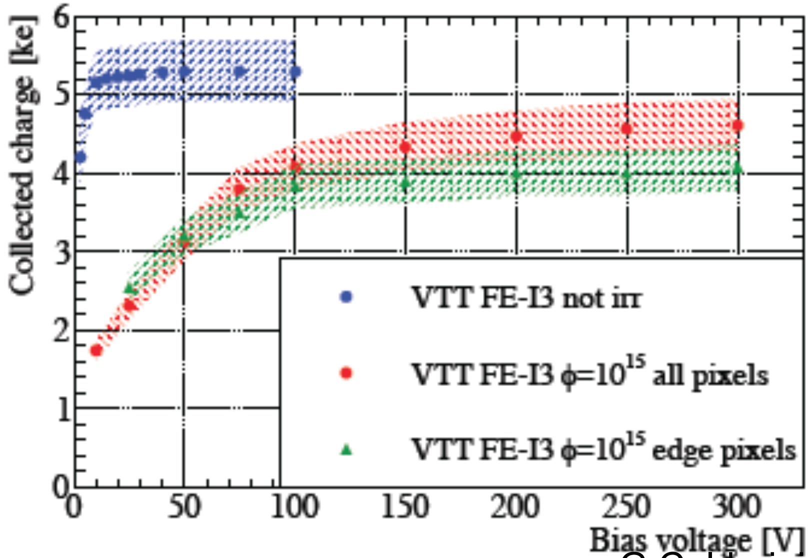
- CCE with $^{90}$Sr scans before irradiation

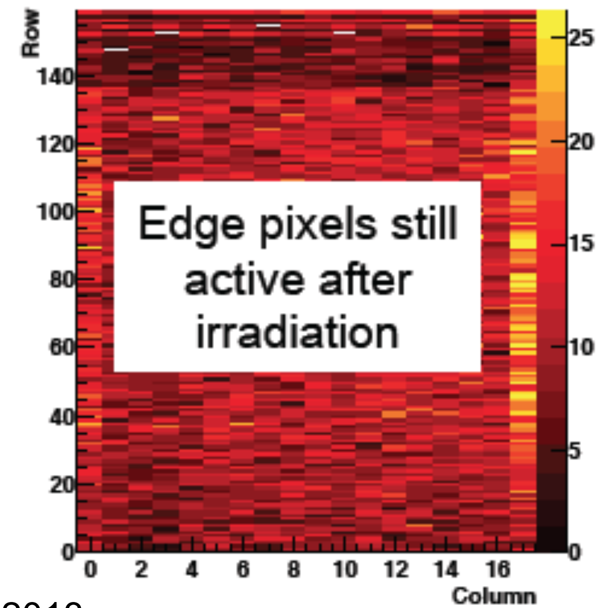



- Edge pixels show the same charge collection properties as the central ones

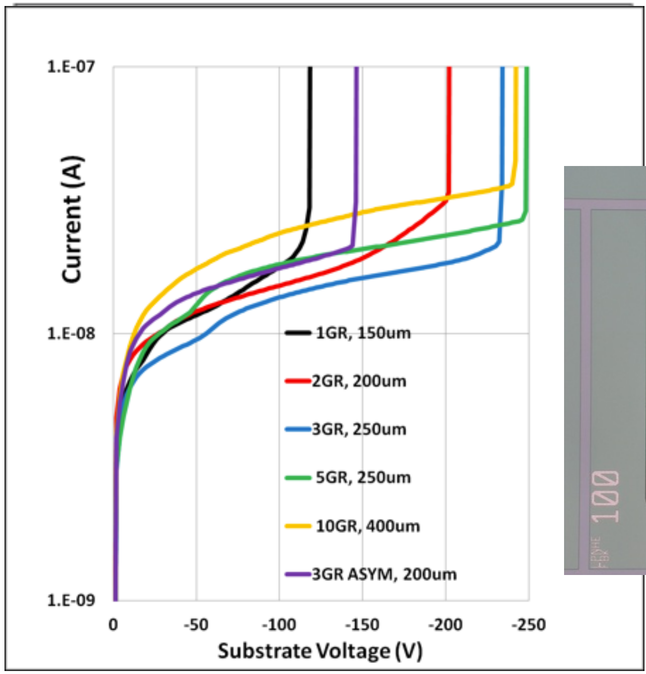



**After irradiation: $\Phi=10^{15}\ n_{eq}\ cm^{-2}$**



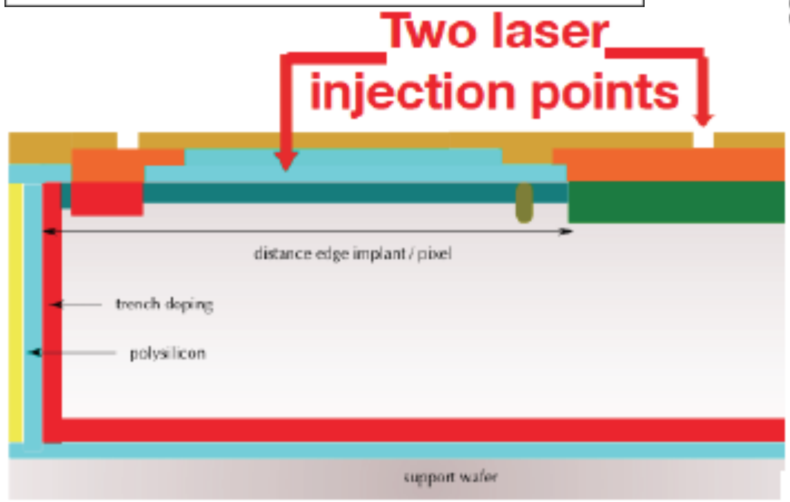
# Active edge pixels – FBK LPNHE

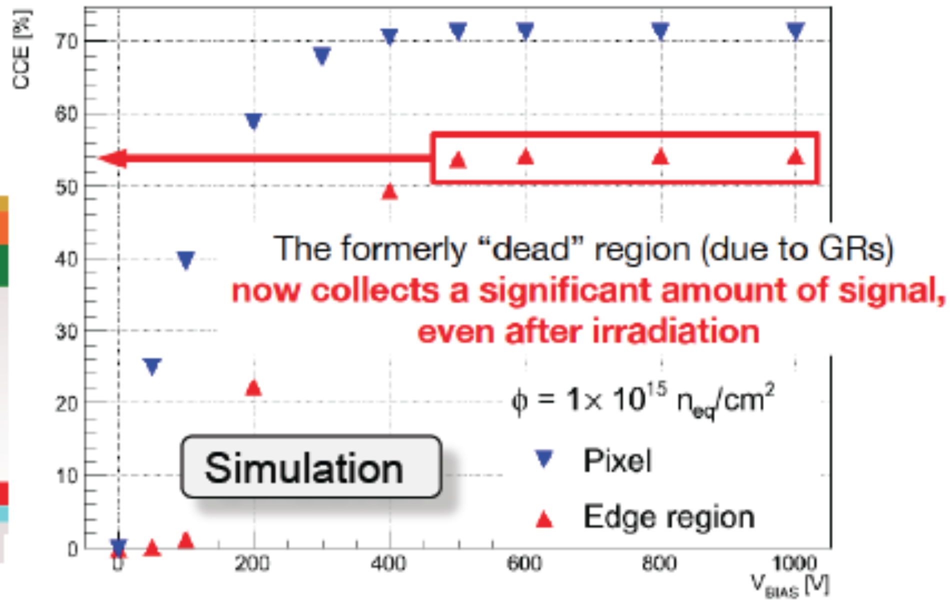



- First IV measurement on test pixels with FE-I4 geometry: all sensor type can be operated in over depletion.

## Simulation

- CCE studied with SILVACO 2D TCAD simulation as a function of fluence and bias voltage.
- 1060 nm laser simulated pulse for charge collection
- CCE defined with respect to the charge collected before irradiation in the "pixel" region




M. Bomben et al., arXiv: 1212.3580

# Electronics

Huge work on the readout electronics to improve performance and radiation hardness

- Going to deep-submicron process (now 65nm, then more)

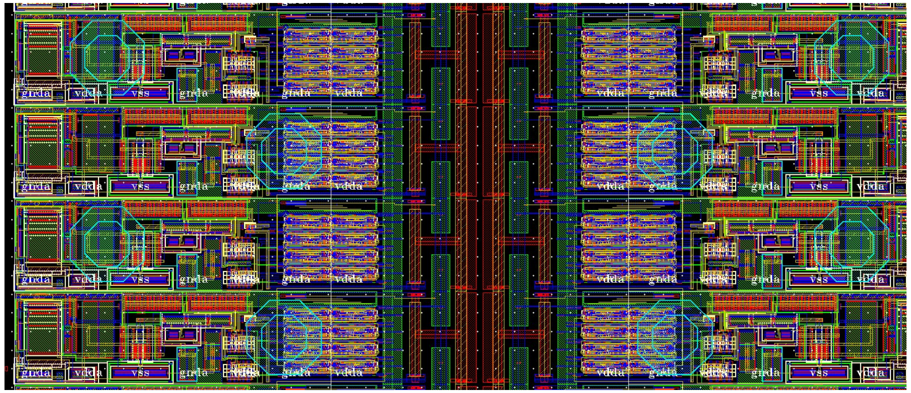
  Intrinsically more radiation hard

  Allows smaller segmentation

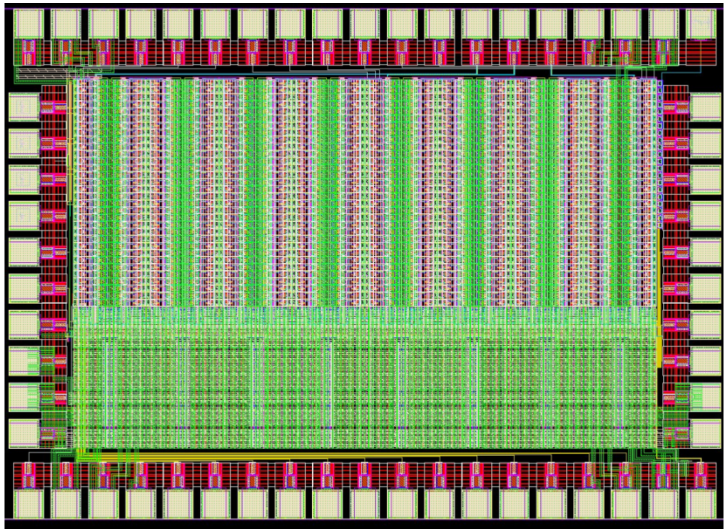
- 3D/Vertical Integration R&D

  Save space

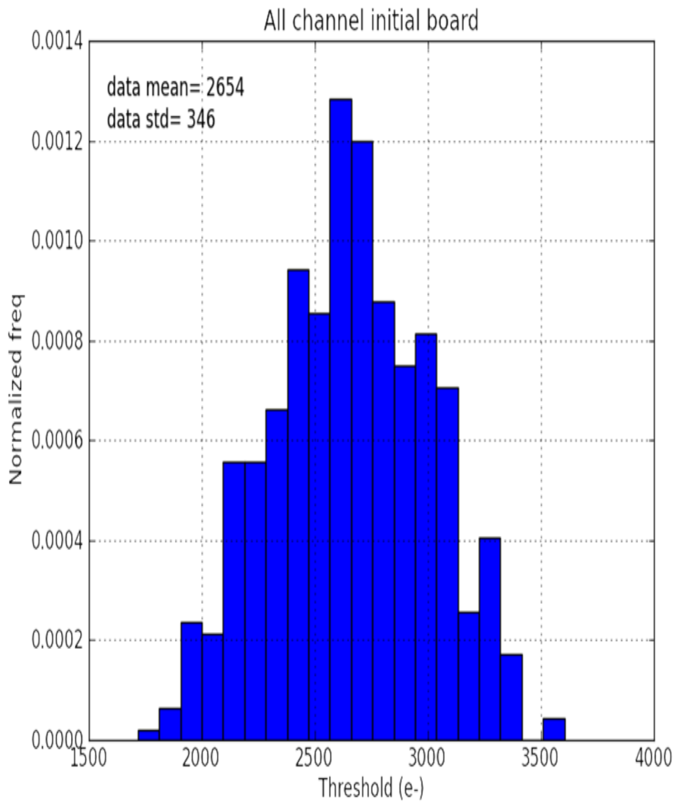
  Allow separation of functionalities (analog vs digital)



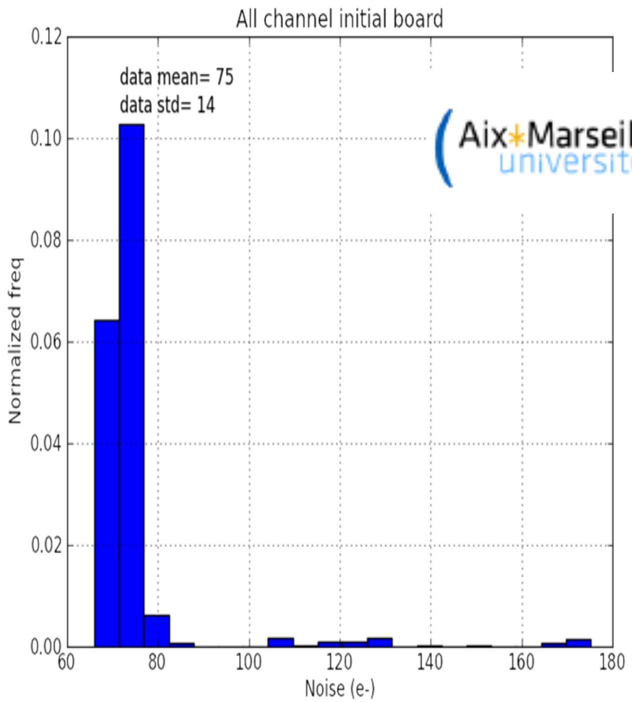
65 nm prototype, 25 x 125



65 nm test pixel matrix 16col x 32 rows



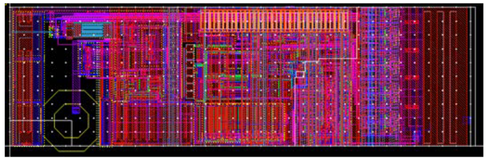

65 nm threshold



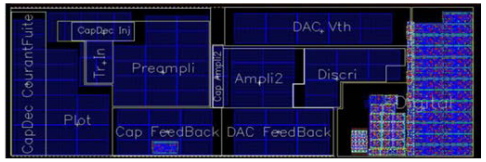

65 nm noise

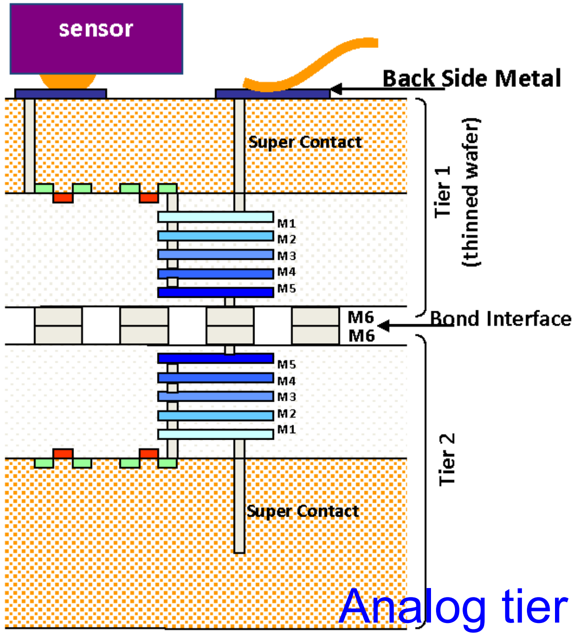
# FE-electronics: 3D 130nm pixel 50x125 $\mu m$

Analog tier



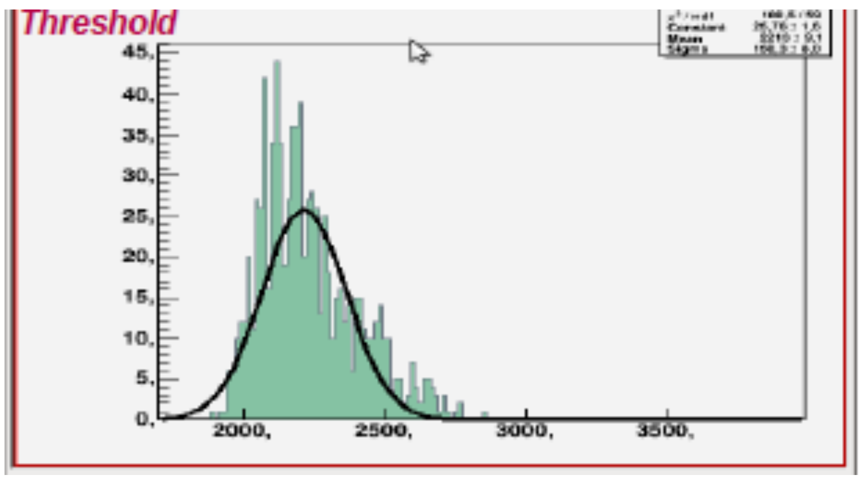
Digital tier

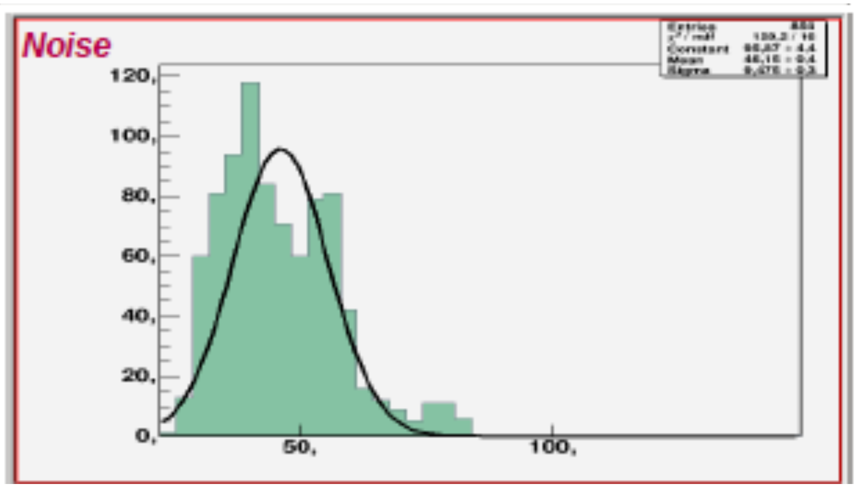



FE-TC4P1
demonstrator

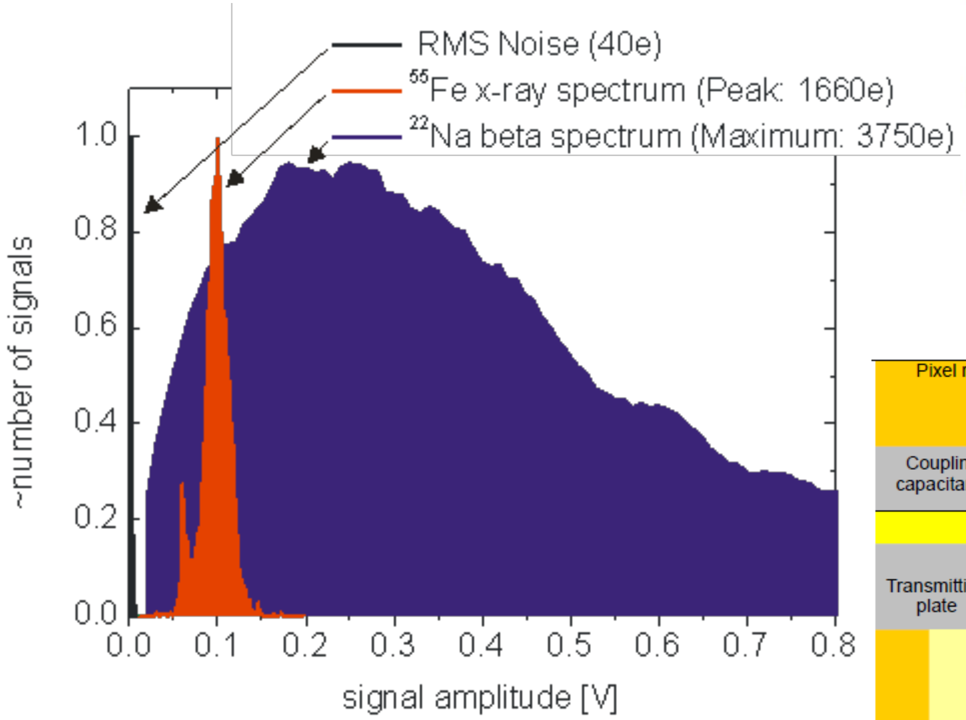
Analog tier
Thr=2200e Sthr=150e noise=46e



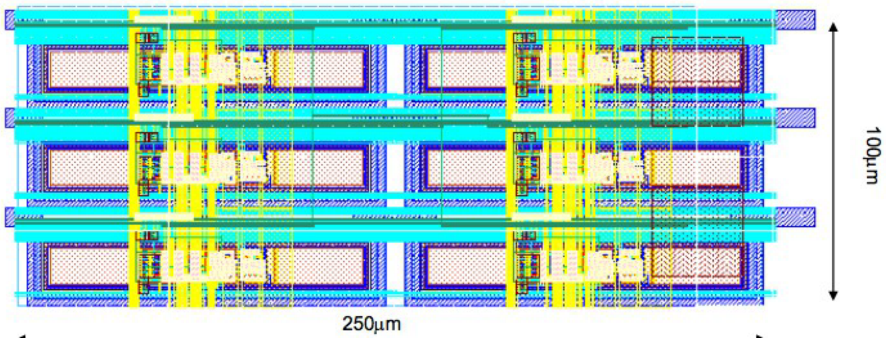



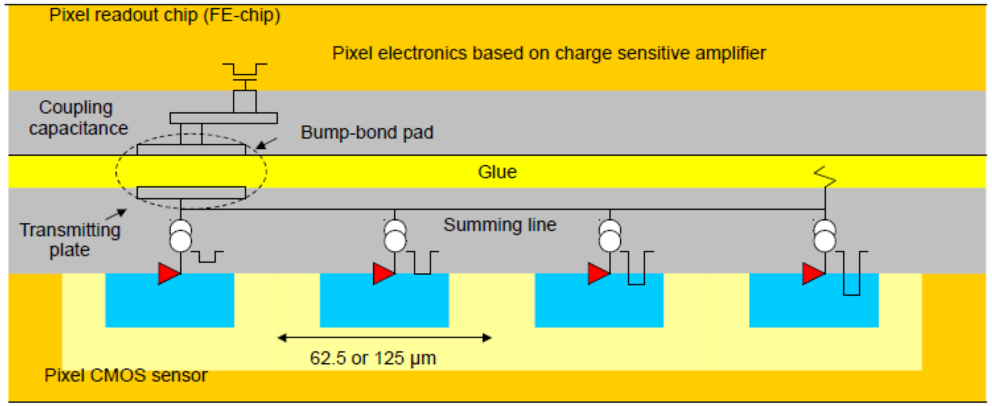
# HV CMOS

Monolithic sensor+electronics 180nm HV2FEI4 ATLAS chip with capacitive coupling to FEI4 subpixel 33x125 µm




irradiated prototype



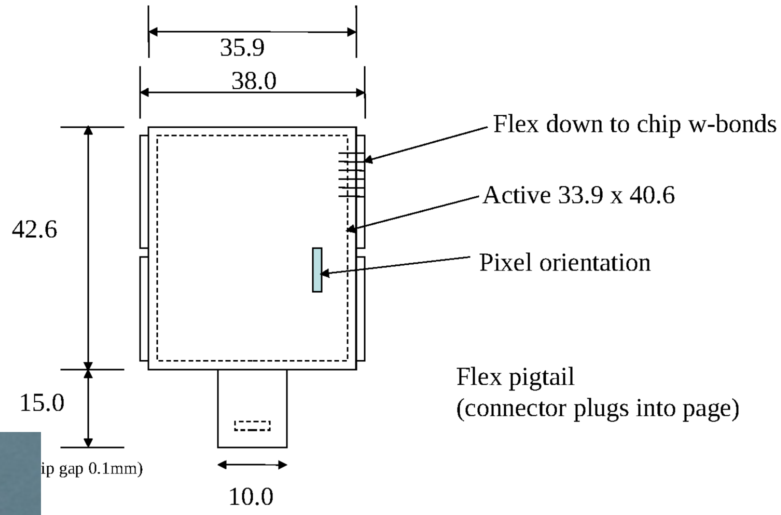

HV2FEI4 demonstrator

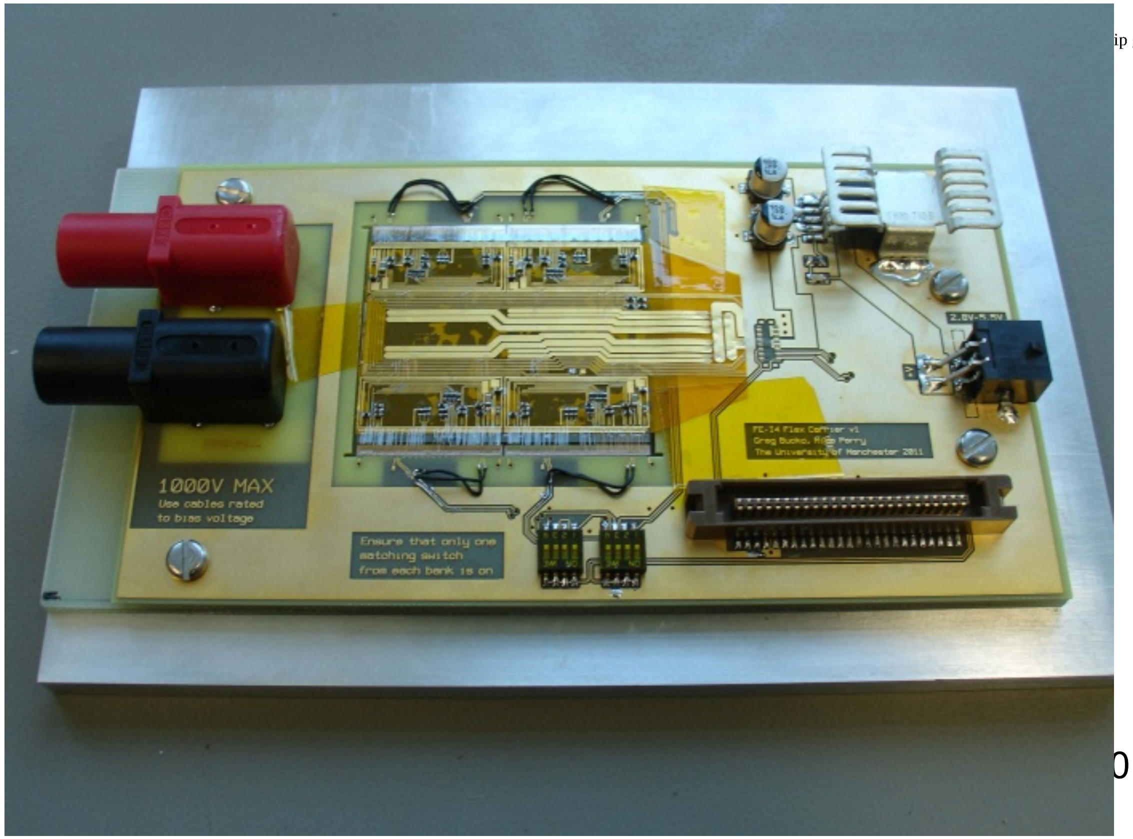
# Outer Pixels

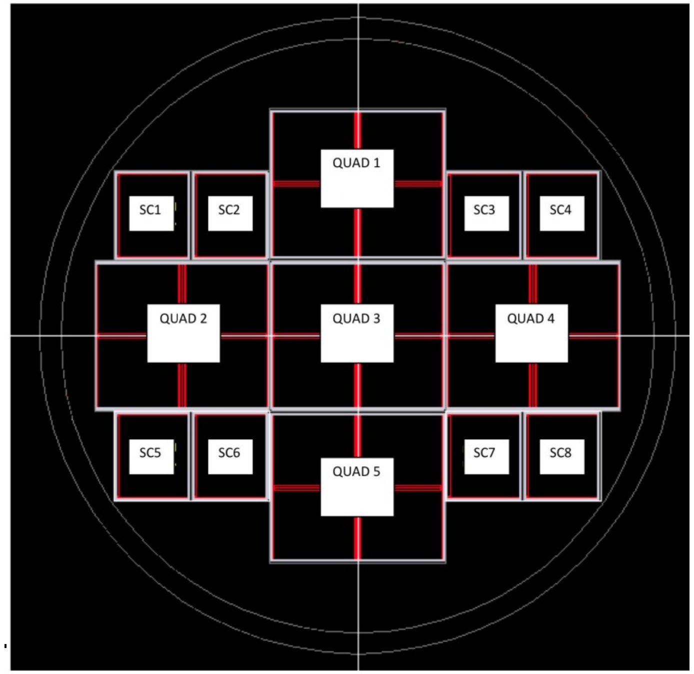
## Most probably planar pixels

## Large area: work on costs

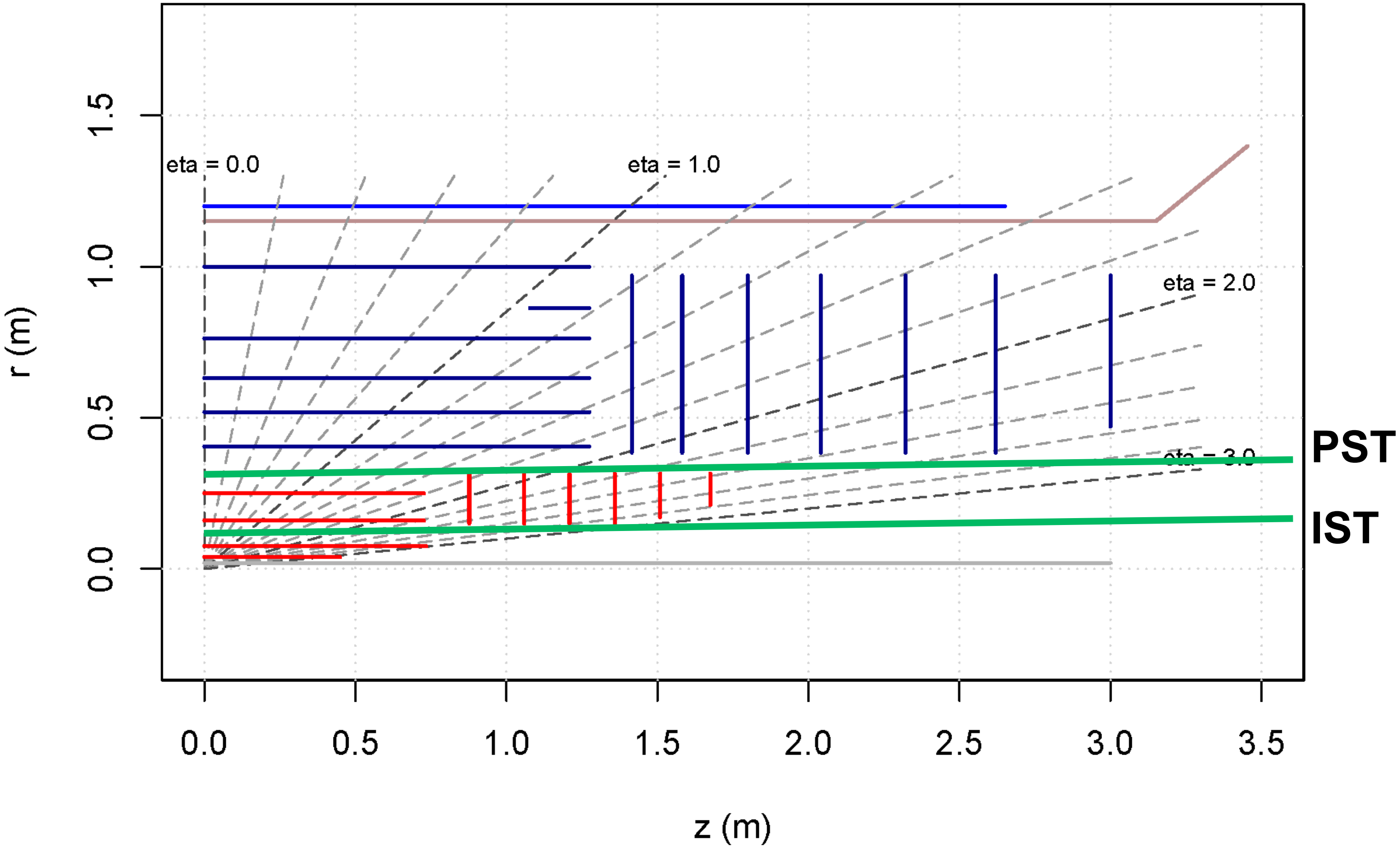
- cheap process (n-in-p?)
- multi-sensor modules
- alternative bonding techniques



# LoI layout



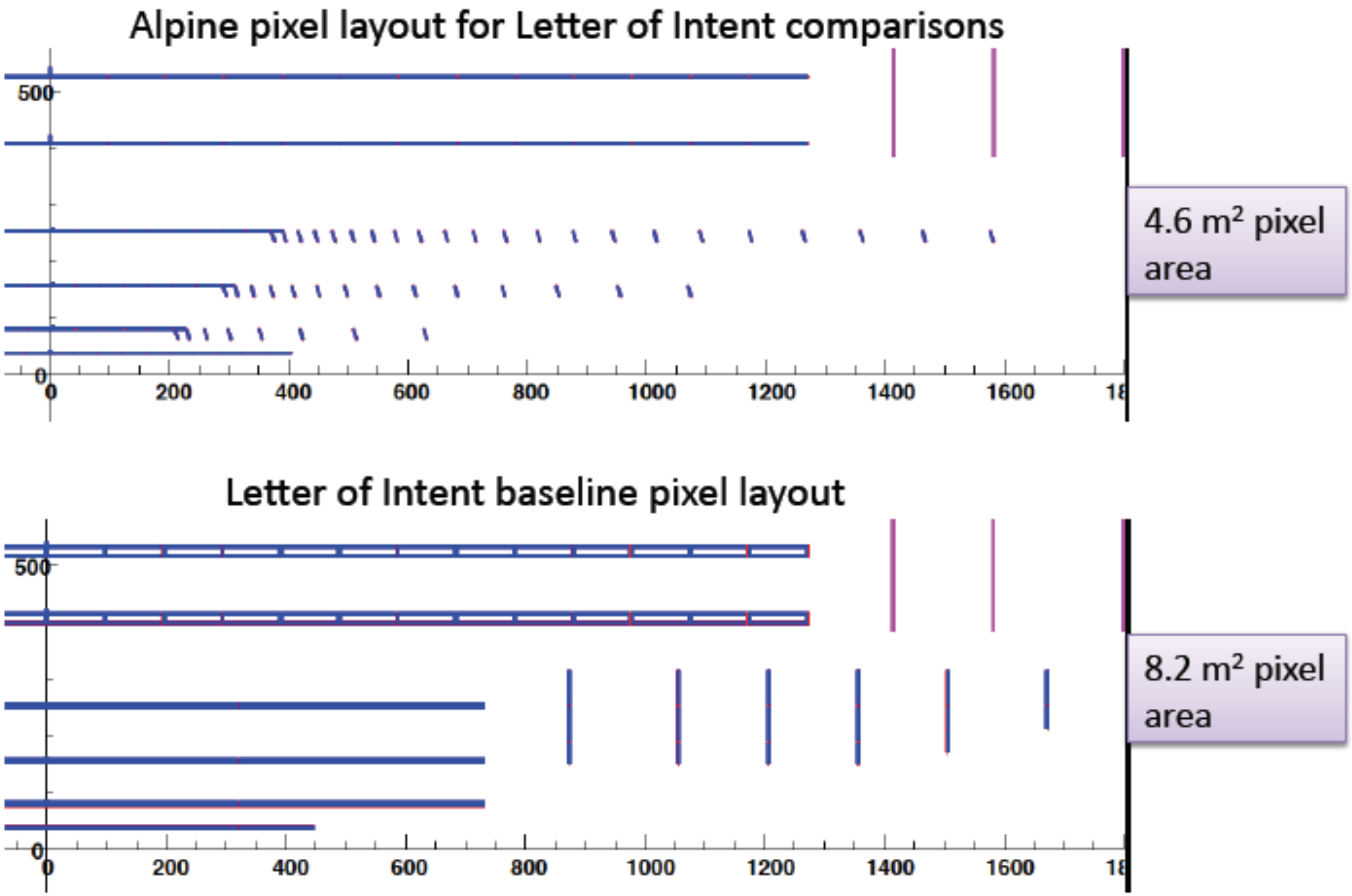

- Classical layout – only barrel cylinders and disks
- Radius of the PST R=34.5 cm bigger than current radius R=24.5 cm
- 2 innermost pixel layers should be replaceable in IST R=11 cm
- Full pixel package should be replaceable

# LoI pixel layout

- Innermost pixel layer: 3.9 cm, second 7.8 cm
- Outer pixel layers at 16 - 25 cm
- Eta pixel coverage up to 2.7 to match muons
- Barrel part of 4 pixel layers
- 6 pixel disks z=88-168 cm
- Up to 8 pixel hits at high $\eta > 2.0$ – reinforced

- Inner+Outer+Disk= 0.8+4.3+3.1= 8.2 $m^2$
- 638 Millions of pixels

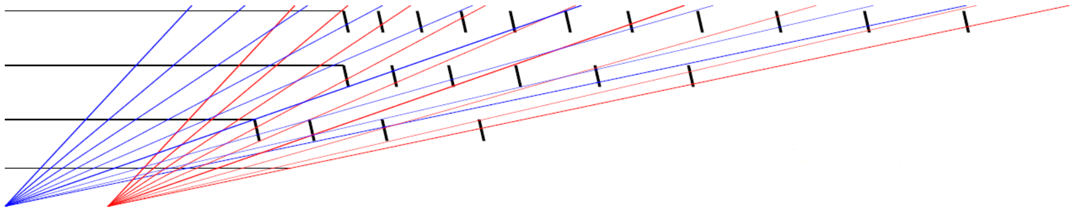
# Some design allows to reduce the surface

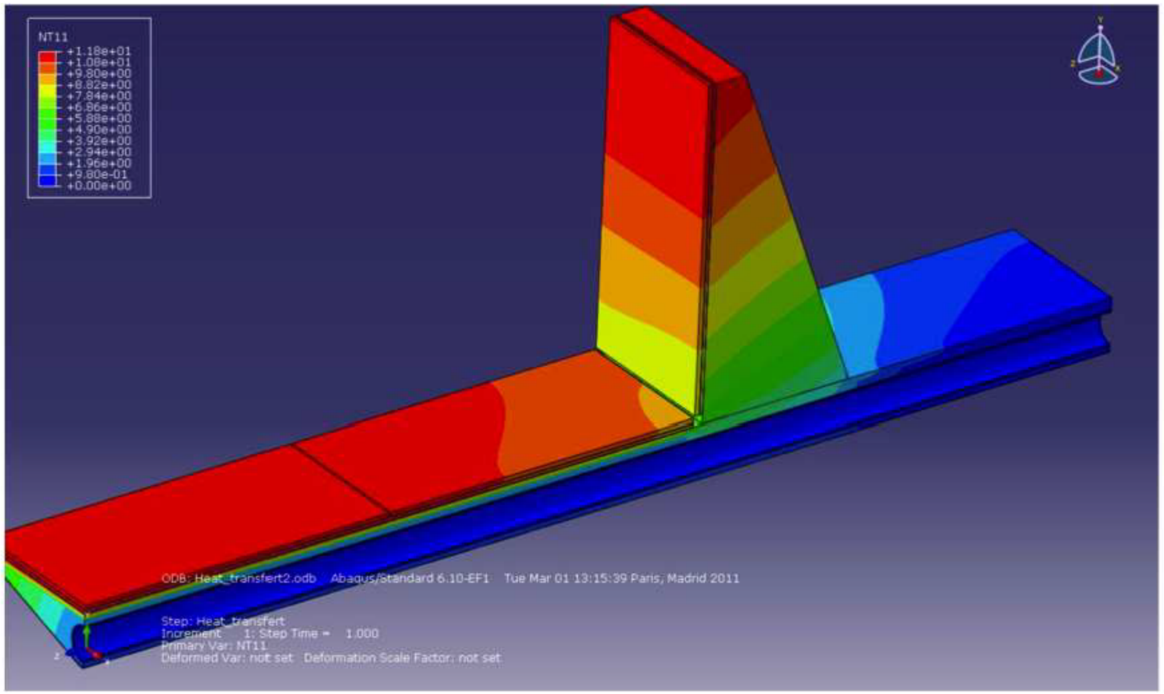



LoI coverage up to n=2.5-2.7

Some aggressive design to extend it to more than 4

- "Alpine staves" in LoI layout
- Possibility to reducing number of disks





# Conclusions

- Remarkable French contribution to the ATLAS tracker upgrade effort
- The calendar between now and 2020 is already very tight and dense. Time flows fast ! Move quickly !
- LHC started in an impressive way

  We cannot afford having detectors which don't keep the pace of the machine !
- In exchange for high luminosity, running conditions could be different from design !

  We need safety margin !
- Most likely not enough funding to have independent CMS and ATLAS R&D programs

  We need to work together !