NECTArCam concept

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List of Abbreviations			
ACS	Advanced Control System	ACTL	array control
AT	analogue trigger	COTS	commercially available off the shelf
DAQ	data acquisition (from camera to ground)	DR	dynamic range
DT	digital trigger	ELEC	electronicstrigger work-package
EMC	electromagnetic compatibility	ENC	equivalent noise charge
ENI	equivalent noise current	FEB	front end board
FPI	focal plane instrumentation	IRD	CTA Industrial R & D workpackage
HV	high voltage	LC	light concentrator
L0	level 0 trigger	L1	level 1 trigger
MST	Medium Size Telescope	MUTIN	Multi Use Telescope INterface
NECTAr	New Electronics for the Cherenkov Telescope Array	PE	photo-electron
PMT	photomultiplier	ROI	Region Of Interest
SLC	Slow Control	WBS	work breakdown structure

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1 Overview of concept

NECTArCam is a camera designed to be operated on the Medium Size Telescopes of CTA. The camera concept is adaptable to other types of telescopes. The section starts with a quick overview of the requirements, then describes the NECTArCam camera concept. Each component of the camera (Front end board, Trigger, Data Acquisition, Focal Plane, Mechanics and Cooling, Slow Control and Calibration) is described in turn.

1.1 Overview of concept for a full camera

1.1.1 Overview of requirements for a Medium Size Camera

The requirements for the camera of the Medium Size telescopes are listed in the Level A [1] and level B [2] requirement documents of the CTA consortium as well as in various preliminary documents (level C requirements [3], reports from the FPI [4] and ELEC [5] work packages.

The camera for the Medium Size Telescopes of CTA should have a weight of less than 2.5 tons. Its field of view should be ideally 8°. The focal plane is a mosaic of 0.18° pixels. The total power consumption of the camera should be less than 5 W per pixel, ideally less than 3 W per pixel. The event trigger rate is $\sim$ 3kHz. The time arrival of photons in pixels should be known to a 2 ns accuracy. The bandwidth of the system before digitization is recommended to be $\geq$ 300 MHz. The trigger time should be known with at least a 10 ns accuracy and ideally with a 1 ns precision. The events should be time-stamped with a 3 μs error. The charge in a 15-20 ns window around the trigger should be calculated. The dynamic range should be at least 1-3000 PE. The relative accuracy of the charge measurement should be less than 35% for a 10 PE signal and less than 6% for a 1000 PE signal. The dead-time of the camera should be less than 5% for a 5 kHz trigger rate and ideally less than 1% for a 6 kHz trigger rate. Further details are given in references [1, 2, 3, 4, 5].

1.1.2 Camera concept

The NECTArCam camera is enclosed in $\sim$ 3x2.8x1.8 m^3 aluminium box and weighs roughly 2 tons (see appendix 5.2 and table 10). It has a field of view of 8 degrees, in accordance with the level B requirements of CTA. It is equipped with 1897 pixels. These pixels are 1.5 inch photomultipliers (PMTs), which are the baseline photodetectors for CTA. They have an angular diameter of 0.18°. The entrance window of the PMTs is located at the focal plane of the telescope. A possible layout of the focal plane is shown in figure 1. The NECTArCam concept

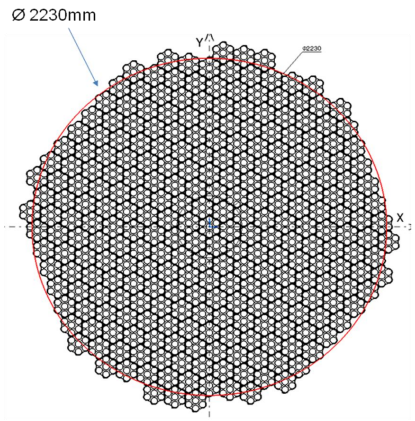

Figure 1: Layout of the focal plane of the NECTArCam camera

is based on the experience gained on the previous generation of Cherenkov cameras, notably the H.E.S.S. and MAGIC cameras, adopting a no-nonsense approach, aiming for reliability and simplicity. The camera is based on pixel modules, allowing for more flexibility in production and repairs. The basic measurement obtained from pixels are the charge and time of arrival of photon atmospheric showers. The charge measurements are linear and easily calibrated. The charge calibration is redundant. The time measurements are done in a straightforward way, minimising the systematic effects from pulse distortion.

- Camera modules

  Cherenkov shower images have a typical extension of about 1° in the focal plane of the telescopes. Following level B requirements, the individual photo-detectors (pixels) have a 0.18° diameter. A typical Cherenkov shower thus creates a signal in on average 25 pixels. The basis of the NECTArCam concept is the grouping of several pixels into a camera module, whose size is a compromise between several factors: While the camera module should be large enough to minimise the electrical connections between modules, there are several points in favour of smaller modules:

  1. The trigger of the camera looks for a signal in a limited number of close-by pixels. The rejection of photon background noise in a large module would imply a complicated combinatorial logic, while a smaller module can use a much simpler multi-stage scheme similar to the telescope trigger used in H.E.S.S. or MAGIC and described in section 1.3.1.
  2. Modules should be easy to produce in the industry and to replace in case of failure.

  Both 7-or 19-pixel modules have very symmetric (hexagonal), easily tessellated shapes, making them natural candidates for modules. The NECTArCam camera uses the smaller 7-pixel ("NECTAr") module; however, the exact number of pixel in the module is not a critical feature of the system. There are 271 modules in the camera.

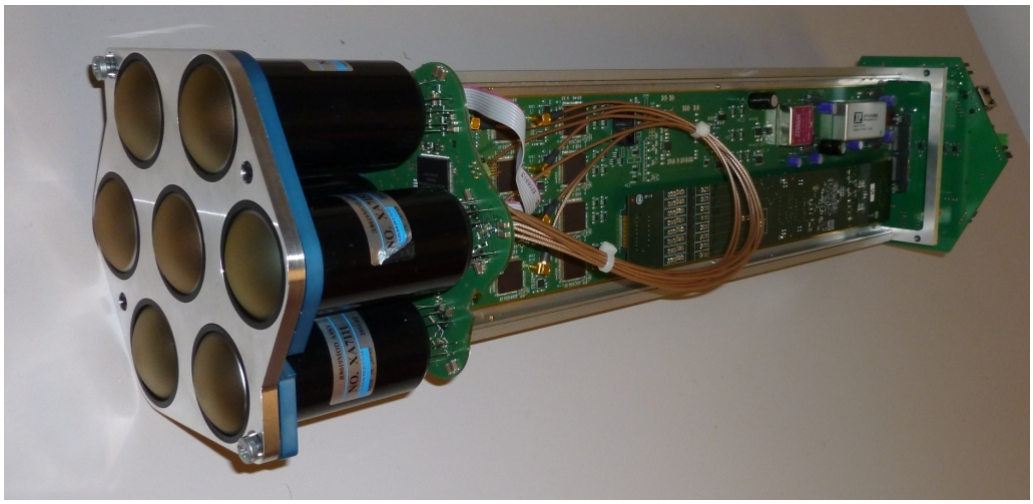

Figure 2: NECTAr module prototype

  NECTAr modules (see Fig. 2) contain several NECTAr chips. NECTAr chips incorporate the switch capacitor array and ADC functionalities. This unique feature allows for a reduction in cost and power consumption compared to e.g. FADC with similar sampling frequency and dynamic range. The internal structure of a NECTAr module is shown in figure 3.

- Charge and time measurements

  The charge is obtained by integrating the signal in each individual pixel over a certain time window. As shown in section 3.1.2. of the level A performance requirement document, the Cherenkov signal in each pixel is generally very short (2-3 ns), while the duration of the signal in the whole camera can be much longer (several tens of ns). It is thus optimal from a signal/noise point of view to use a narrow integration window ($\sim$ 10 ns) for every pixel and a trigger scheme which allows different read-out times for different pixels.

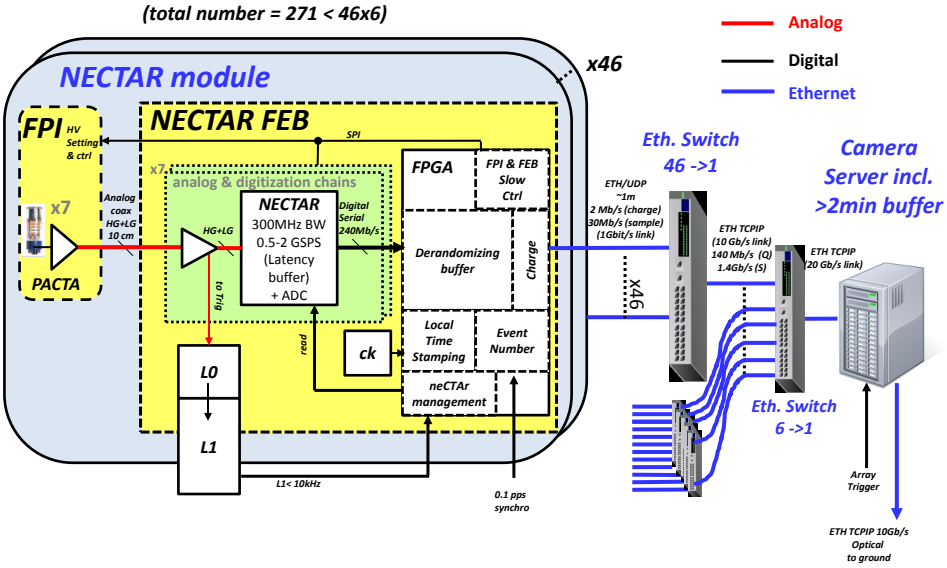

Figure 3: Data flow of the NECTArCam

The time of arrival of the Cherenkov pulses has to be recorded with a 2 ns accuracy (Level B requirements). This requirement allows measurements of time gradients of the order of 1ns/degree (see fig. 8 of level A requirements) by using the information in ~ 5 pixels. Several factors contribute to the accuracy of the time of arrival measurement: intrinsic width of the signal (~ 2 ns), time spread of signal in phototubes (~ 1 ns), diffuse photon background and the distortion of the signal in the electronics. To minimise the latter factor, the bandwidth of the electronics before digitisation has to be ≥ 250 MHz. The time of arrival is better determined if several samples are taken from within the Cherenkov pulse. This implies using a GHz sampler. Special care has been taken in the NECTArCam camera to avoid systematic effects from pulse distortion. The analogue output of the photo-multipliers is propagated only on a 10 cm distance. The chip has the required ≥ 300 MHz bandwidth, introducing only a minimal distortion of recorded pulses. It can sample the signal at GHz rates, allowing for a precise estimate of the time of arrival.

- Calibration of charge

  The required dynamic range is 1-3000 photoelectrons. The calibration of charge can be done on-line, e.g with muon ring measurements. However, a redundant calibration is preferable. One way of doing that is to take dedicated single photo-electron measurements and fit a charge histogram (see for example Fig. 29). Assuming the single photoelectron in bin 10, the required dynamic range is 0.1-3000 photoelectrons, corresponding to 15 bits. This can be achieved by using 2 different gain channels with a 10-12 bits digitiser. Measurements (see table 2) have shown that single channels on NECTAr chips have more than 11 usable bits. It is thus possible to achieve a redundant measurement of charge with the NECTAr modules.

- Read-out strategy

  The standard read-out option for Cherenkov telescope cameras is to read all channels in the camera at once, around the time given by the global camera trigger. Although this approach is simple to implement and has already been successfully employed by the predecessors of CTA, a more flexible read-out scheme has been proposed for several reasons: Firstly, it has been shown that shower images cover on average not more than 10% of the camera area and are highly concentrated, so that the vast majority of channels normally read out contain only noise. Thus, a system that reads only those pixels in a pre-defined region of interest around the shower core will achieve a significant reduction of the data rate and dead-time without losing relevant image information. Secondly, in particular for multi-TeV showers, the development of the shower image over the camera can be slow (up to a few 100ns), much longer than the integration window

proposed for each pixel. An example of a (simulated) photon shower development is shown on figure 4. Thus, in that case, a static read-out of all pixels at the same time will tend to lose important parts of the

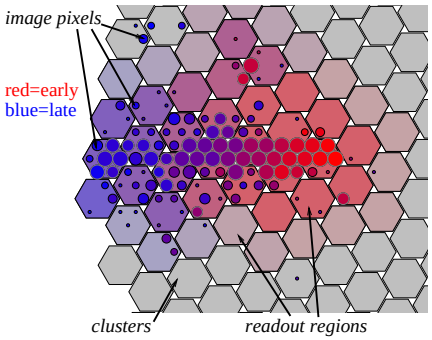

Figure 4: Example for a slowly-developing image of a 15 TeV shower. Colour coding is from red (early) to blue (late), with a total image duration of 55ns. The colours of the clusters (hexagons) indicate the local triggering and readout times, closely following the image development. From [8]

image that could be recovered by instead reading each channel around the local pulse maximum. Different approaches to address these issues are being investigated for NECTAr CAM: An on-board FPGA-based image analysis to determine the pulse maximum and find the optimum read-out window in each channel prior to charge integration, and a definition of regions of interest and read-out times based on local trigger information (Colibri concept [8]). In the latter case, regions and windows are defined without requiring to read out the analogue memory, thus reducing dead-time for unread channels (as opposed to the former case, where first a longer time window is read out of which only a part is kept). However, it requires an additional L1 trigger level to identify the regions of interest.

1.1.3 Architecture of the NECTArCam

NECTAr modules receive photons signals from the photo-detector. When suitable trigger conditions are met, the PMT pulses of a photon event are recorded. The architecture of the trigger system and the data flow are shown in figures 3 and 5, respectively.

The trigger operates on 3 levels. The first level, called L0, is local to each NECTAr module. The trigger path is separated from the data path immediately after the amplification of the signals from photo-tubes. The output of the L0 is sent to the on-module L1 circuitry. The L1 decision is then sent to the L1 distribution board on the backplane. The L1 trigger combines L0 output from adjacent modules and provides the camera level trigger. The L1 accept/reject signal comes back to the modules after a latency of less than 400 ns. On L1 accept, the data are transferred from the NECTAr chips to the on-module FPGA. Data samples (typically 10 to 30 ns around the time of trigger) stored in the NECTAr switched capacitor array are sent to the on-module FPGA. The read-out of the NECTAr chip takes 2-3 μs depending on the number of samples. High level quantities such as the total charge and time of arrival of the signal in each pixel are calculated in the FPGA. The data are then transferred to an event buffer located on an on-board camera server. After being accepted by the array level trigger (third level of trigger), the data are transferred from the camera to the ground. The reduction in trigger rate from the array trigger is expected to be a factor 2-3 in the MST telescopes. The event buffer is designed to accomodate $\sim$ 2 min of data, well above the latency ($\sim$ 5 μs) of the array trigger. Assuming no extra dead-time is introduced by the Ethernet connections, the dead-time of the NECTArCam camera is dominated by the read-out of the data and transfer from the NECTAr chip to the FIFO in the FPGA of the NECTAr module. Assuming a 10 kHz L1 trigger rate (from level B requirements), the dead-time of the read-out is at most 3%.

Assuming 2 gain channels per pixel, 12 bits per sample, and a read-out window of 16 time samples, the amount of data per event transferred from the NECTAr chips of a module to the NECTAr FPGA is 7x2x12x16= 2.7 kbits. In the FPGA, quantities such as the total charge and the time of arrival are calculated. Assuming that the total charge is calculated to 16 bits, the amount of data per module to be transferred from the FPGA to the camera server is 2.7 kbits for the full time samples or 0.2 kbits for just high level parameters(charge, time of the maximum, time over threshold) The connection between the NECTAr module and the

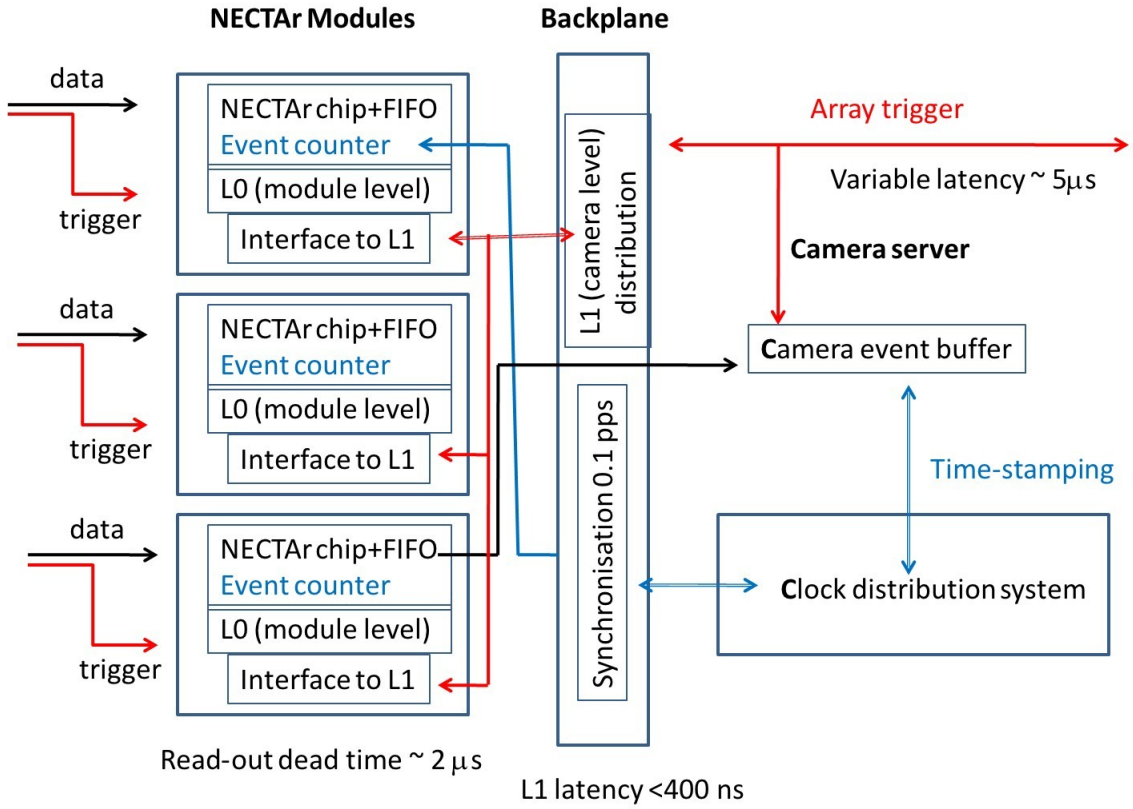

Figure 5: Architecture of the trigger system of the NECTArCam

event buffer proceeds in 2 steps. The data from 46 NECTAr modules are first concentrated on an Ethernet switch. Then the data from 6 Ethernet switches are sent to the event buffer. Assuming a 10 kHz trigger, the transfer rate from the NECTAr FPGA to the switches is $\sim$ 30 Mbits/s (2 Mbits/s) for all the samples (for the charge). This can be easily accommodated with a 1 Gbit/s Ethernet connection. The transfer from the Ethernet switches to the camera server uses also a 10 Gbit/s Ethernet connection. The transfer from the camera server to the central DAQ farm uses a 10 Gbit/s link.

1.1.4 General layout of the NECTArCam camera

In addition to the data and trigger paths, the camera has to incorporate control and monitoring tasks. Examples are the setting and monitoring of the high voltage of each photo-detector, the control and calibration of NECTAr chips, the monitoring of temperature etc. The internal temperature of the camera has to be controlled (especially if SiPM are used as photo-detectors). A safety system has to be implemented (e.g. for shutting down the camera and lowering the high voltages in case of exposure to excessive light). The power has to be distributed to the camera. A list of the functionalities required to run the camera is shown in figure 6. The implementation of these tasks are improved versions of the slow-controlservice tasks of the H.E.S.S. and MAGIC cameras.

1.1.5 Distribution of tasks and organisation of the NECTArCam consortium

The NECTArCam consortium is organised according to the "project management" philisophy. The end-product of the NECTArCam project for the present phase of CTA is to build a camera prototype. In addition, the industrial production of the camera should be prepared. This means preparing the test benches for the various sub-components and the integration of the camera. The organization of the NECTArCam project is shown on figure 7. It is divided into a system and a technical branch. The system branch includes the camera integration and the quality activities. The technical branch is divided into four work packages: focal plane equipment, mechanics and cooling, front end electronics, camera processing and monitoring. The WBS of each work package is described in more details in the appendix 5.4.

As stated earlier, the basic brick of NECTArCam is the NECTAr module. The NECTAr module is composed

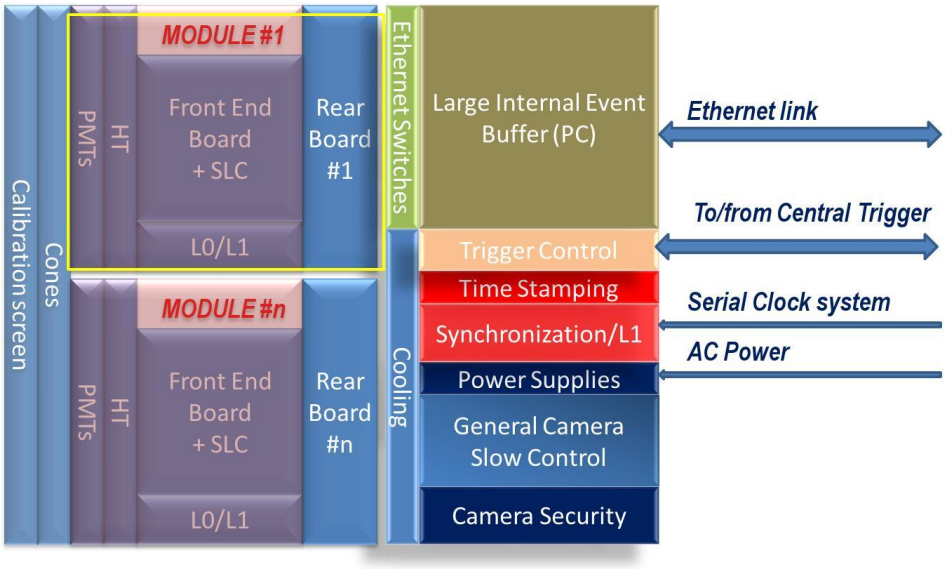

Figure 6: Global layout of the NECTArCam camera

of the front-end electronics board interfaced on one side on the PMTs and their HV, and on the other side on a backplane. The next section describes the front-end electronics.

1.2 Front-end electronics

1.2.1 Global description

The front-end board is the main element of the module, managing read-out and digitisation of the 7 pixels, slow control, monitoring and data transfer via the Ethernet link (see Fig. 8). This board also houses electronics for building trigger primitives. The bandwidth of the components is such that it does not distort the signals. Special care was taken at each step to meet signal integrity and EMC rules.

In order to accommodate a large dynamic range extending from 0.2 to 3000 photoelectrons, the output of each PMT (photomultiplier) is split into 3 linear channels with bandwidth larger than 300MHz: high gain, low gain and trigger channels. The high gain range from 0.2 to 200 PE is dedicated to small amplitude signal and is usable for calibration on single photoelectrons. For cross-calibration purposes, it overlaps by more than a decade with the low gain, which is usable from 10 PE and 3000PE. The trigger channel provides a signal to the L0 electronics on a range limited to few tens of PEs, but with a higher gain. The L0 and L1 electronics, described in dedicated sections of this document and built on mezzanine cards for the existing prototypes, will be integrated into the final front-end board.

The very fast L0 and L1 triggers give a response after a fixed delay of up to 400 ns. During this time, an analogue memory (contained in the NECTAr ASIC) stores the signal, sampling at a frequency predefined between 500 kHz and 2GHz. On arrival of the trigger signal, the sampling of the analogue memory is stopped and its internal reading pointer is moved to the beginning of the region of interest (compensation of the trigger fixed delay).

The local FPGA manages all the necessary control signals and initiates the reading process. The duration of the read-out window is programmable. The Analogue to Digital Converter (12-bit) embedded in the NECTAr ASIC converts and serialises the data for the FPGA. A first level buffer embedded in the FPGA de-randomises the data flow. The FPGA stores the samples on the fly. The equivalent charge and timing information are calculated by the FPGA when it sends data blocks over the Ethernet using the UDP protocol.

1.2.2 Signal conditioning on the front-end board (ACTA)

To minimise PMT ageing effects, it is planned to operate the PMTs of the CTA cameras with a gain as small as 5. 10^4 instead of 2. 10^5, the value used in the H.E.S.S. experiment. Operation of the NECTAr prototype module, comparable to calibration on single PE, has been successfully demonstrated at this low gain using the PACTA [9] pre-amplifier prototype directly connected on the PMT base. The final design of the NECTArCAM

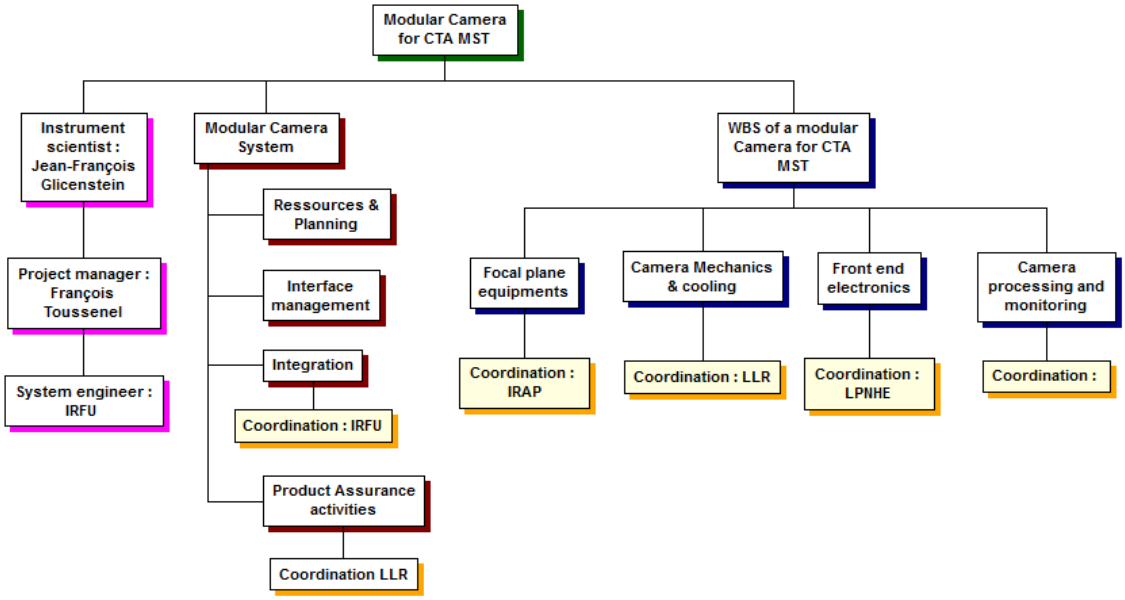

Figure 7: WBS of the NECTArCam camera. The sharing of responsibility reflects the present status.

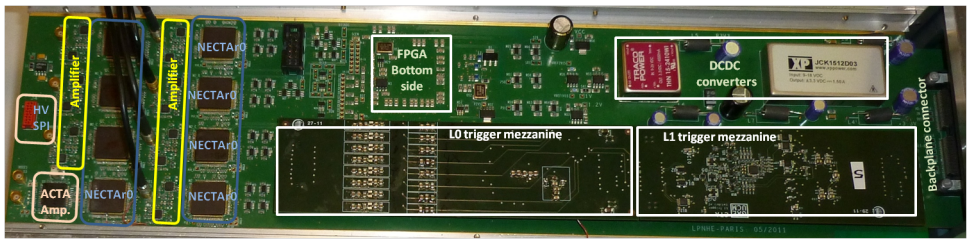

Figure 8: Global architecture of the front-end board illustrated on the FEB of the NECTAr prototype. The output of the PMTs is on the left hand side. The signal is amplified. 8 NECTAr0 chips are implemented on the FEB. The signal on 7 of these channels are equipped with commercial amplifiers. The remaining channel is equipped with an ACTA amplifier. On trigger, the data are sent to the FPGA, then to the DAQ through the backplane (on the right).

is based on a PACTA type pre-amplifier with outputs providing high gain and low gain. Nevertheless, since the final PACTA pre-amplifier(see section 1.5.3) is not available at the present time, the signal conditioning on the current NECTAr module prototype is only based on the ACTA amplifier located on the front-end board. These amplifiers at the input of the front-end board are needed for impedance isolation to adapt the dynamic range of signal and to provide differential signal to the digitiser. Prototypes of the amplifier ACTA [10] have been designed in AMS CMOS 0.35μm technology, in the framework of the NECTAr collaboration, optionally to be integrated inside the NECTAr chip. Test results and specifications are shown in Table 1.

ACTA has been successfully validated in a stand-alone version as a special test channel on the NECTAr module prototype. The use of the ACTA ASIC with 3 amplifier sections (High Gain, Low Gain and Trigger) is the baseline for the next NECTAr front end board design, because its power consumption is significantly lower and its level of integration higher than equivalent COTS solution.

1.2.3 Analogue pipeline NECTAr0

The NECTAr0 chip, depicted on Fig. 9, is the first prototype of an analogue buffer and digitiser chip specifically designed for the CTA experiment. It is based on the architecture of the SAM chip [6] designed for the H.E.S.S.-II telescope and uses the same well-known and high yield CMOS 0.35 μm technology from AMS. It is packaged in a very compact QFP128 package (16 mm x 16mm footprint).

NECTAr0 includes 2 fully differential channels of analogue memory - 1024 cells depth each - used as circular

Parameter	Value	Units
Gain	5 to 20	V/V
BW	400	MHz
Slew Rate	1 to 1.5	V/ns
Linearity (VoD<1Vpp)	< 1	%
Linearity (VoD<2Vpp)	< 3	%
Input ref. noise (en)	< 3	
DC offset (output)	0 to 1.5	V
Gain Temp. Coef. (TC)	0.06	%/C
Power consumption	20 to 30	mW

Table 1: ACTA performances

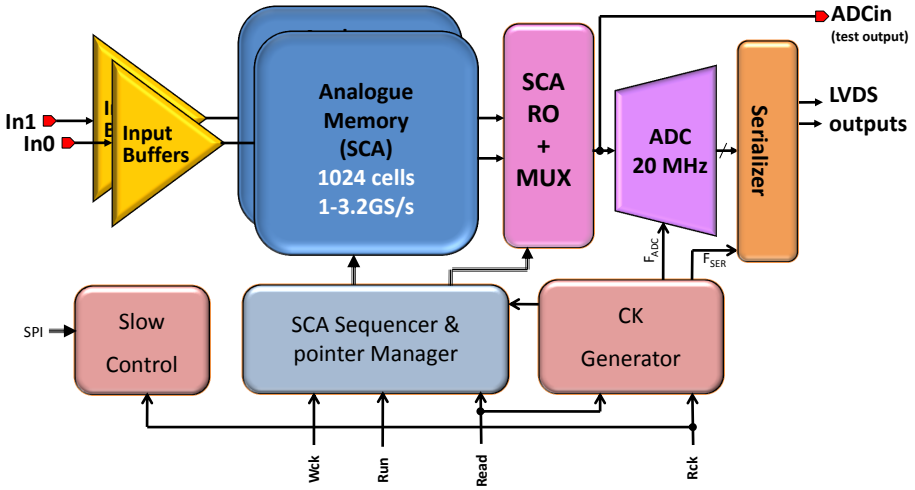

Figure 9: Block diagram of the NECTAr0 chip. It includes the dual fonctionnality of Switched Capacitor Array (SCA) and ADC.

buffers, which are written in parallel. The two channels are continuously sampling and storing the analogue data from the 2 gains of a PMT at a rate in the range of 0.5 to 2 GSPS (the chip has been tested successfully from 0.2 to 3.2 GSPS). The sampling is stopped when an L1 trigger arrives, and the read-back operation of a zone of interest of the memory corresponding to the triggered event starts immediately. The position of the first sample to read in the memory is computed by the chip itself, without any dead time, taking into account the trigger latency. The data of the two gains are multiplexed towards the on-chip 20 MHz, 12-bit ADC which converts and serialises them to the FPGA at a 240 Mbit/s rate. The time required to read back and digitise the data from the two gains is 100 ns per sample plus an overhead of 400 ns, corresponding to the ADC latency, and 100 ns each 16 samples (2μs for 16 samples, 3.7μs for 32 samples). The 1024-cell depth corresponds to 512 ns and 2048 ns for sampling rate of respectively 2 and 0.5 GSPS, more than enough to accommodate the camera trigger latency. Due to its architecture, the data provided by NECTAr0 do not need any correction and can be used directly by the FPGA for computation. The capacitance of its analogue input is very small, so that it can be driven very easily by low cost low power amplifiers as the ACTA ASIC. The main performance parameters of the NECTAr0 chip (measured in a realistic environment on the NECTAr prototype board, supplied with DC-DC converters) are summarised in Table 2. Further details on the architecture and performances of this chip can be found in references [7] and [8].

A new nectar chip (NECTAr1) will be prototyped during summer 2012. It will be nearly identical to the previous version but to reduce cost will integrate twice as many channels. Its read-out will also permit to decrease the dead-time to $\sim 1\mu$s for high gain only events.

	Feature or Performances	Initial Requirement	Unit
Nb of Channels	2		Differential Channels
Memory Depth	1024		Cells
Input impedance	4		pF
Power Consumption	210	≤ 300	mW
Analog Bandwidth	410	≥ 300	MHz
Sampling Frequency	0.4 to 3.2	0.5 to 2	GSPS
Deadtime/event (16 samples)	2	5	μs
ADC LSB	0.5	0.5	mV
Total Noise	≤ 0.8	≤ 0.8	mV RMS
Maximum signal	2	2	V
Dynamic Range	11.3	≥ 11	Bit RMS
Crosstalk	0.4		%
Relative NonLinearity	≤ 3	≤ 3	%
Sampling Jitter	≤ 40	$\leq$50	ps RMS

Table 2: Summary of the NECTAr0 performances

1.2.3.1 Chip Cost and Yield

The production yield of the SAM chip - 6000 chips produced and tested in 2007- using the same CMOS technology, was 90%. This excellent yield is confirmed by the fact that all the 20 NECTAr0 chips soldered untested on the NECTAr board prototypes were properly working. Taking into account the packaging, the test and the yield, the cost of a good chip is estimated to 10 Euros for NECTAr0 (1 PMT channel) and 13 Euros for NECTAr1 (2 PMT channels).

1.2.4 Read-out scheme, FPGA

To optimise the cost of the overall module, a single low cost, low power, ALTERA CYCLONE III is used for each module to perform all the digital operations required: slow control, analogue memory control, data buffering, calculation, read-out and interface to DAQ. Its code, written in VHDL, is optimised for speed. It communicates with the DAQ using a single ETHERNET UDP link used both for read-out and control. The FPGA generates the control signals of the 7 NECTAr chips of the board and performs the read-out of their digitised output data in parallel. These data, associated with an event number generated inside the FPGA by counting the L1-triggers and a local time stamp, are then fed to the embedded FIFO system able to store up to 10 events and used as a de-randomiser. Each module uses a free running clock, but to keep synchronisation of events at the camera level, the event number and local time stamp counters are periodically reset by a signal distributed synchronously to all the modules. Charge, timing calculation, and possibly gain selection are optionally performed by the FPGA when the data are read back from the FIFO and sent to Ethernet through a special optimised UDP core able to sustain 1 GB/s. The code allows interleaving data and slow control with different destination IP/MAC addresses. This useful facility allows an automatic data messages routing. A special mechanism is used to define the MAC and IP addresses of each module in order to have exactly the same code in each FPGA. It is possible to remotely reprogram the FPGA through the Ethernet link.

The total dead time of the system is dominated by the read-out time of the NECTAr chips (i.e. 2μs for 16 samples), all the other operations are pipelined and do not generate extra dead times. The system has been successfully tested with various trigger rates up to 150 kHz. The FPGA allows the control of the SPI interfaces used to set and read the HV board parameters, the NECTAr chip settings, the L0/L1 trigger parameters and to monitor parameters such as on-board temperature.

1.2.5 Backplane

The backplane is the electronic board fixed on the mechanical structure that provides the electrical interface (DAQ, slow control, power, safety, trigger) between the camera body and the front-end modules. The interface is

made by one connector per camera module, which mechanically connects all signal lines of each camera module to the signal lines of the camera body. Related to this is the mechanical structure of the camera modules and the corresponding support structure in the camera body, where mechanical guides are needed to ensure correct insertion of each module in the camera body and the seamless connection of the module without damaging the connector. The backplane could be consist of individual boards for each camera module, or boards supporting several modules.

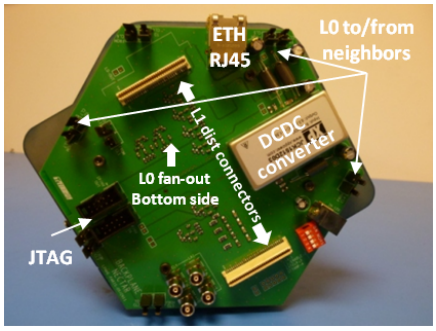

Figure 10: Backplane of the first NECTAr module prototype.

On the camera body side, the first prototype backplane board developed for the NECTAr module (Fig. 10) contains the following connectors:

- Power supply : 12V
- Data acquisition (Ethernet link to desktop computer)
- L1 distribution mezzanine correctors
- L0 connections to/from neighbor modules
- JTAG connector to download FPGA firmware

The backplane is now redesigned in a working groups including members of other camera projects. The next version of the back plane will include the L1 distribution functionnality, as described in section1.3.

1.2.6 Power

The front-end board power is supplied with a single low voltage supply, from which all the different voltages required for the various electronics components are derived using DC-DC converters.

This concept has been demonstrated on the prototype module build in 2011, using a 12V voltage supply. Moreover, tests on the module have proven that it is possible, without any penalties, to supply all of the electronics, including the amplifiers and the NECTAr0 chip, by directly using the output of the DC-DC converters. The power consumption is consequently 25% smaller compared to options with extra linear regulators. The final value of the low supply voltage, between 12 to 48V, is still under investigation. The detailed measured power consumption of the module is given in table 11.

1.3 Trigger of the NECTArCam camera

Several schemes to trigger the NECTArCam camera are possible at the present stage. The first scheme, called analog trigger, is based on the experience of H.E.S.S and MAGIC. It is described in section 1.3.1. The output of PMTs of a single module is compared to a threshold (possibly after a local summation). This constitutes the L0 trigger. Then a camera trigger (L1) is issued whenever neighbouring modules have issued a L0 trigger. However, the trigger of the CTA telescopes has an important difference with the trigger of H.E.S.S and MAGIC. Due to the larger field of view, the probability of having gammaray events lasting several tens of seconds is non-negligible (see fig. 34). This can be accommodated by the Colibri trigger scheme, described in section 1.3.3.

The second sheme, called digital trigger, is a new concept, described in section 1.3.2. In this scheme, the output of the PMT are sent to a comparator on the L0 board. Then the digitized signals from neighbouring modules are used to produce the L1 trigger.

The different trigger schemes are implemented on the NECTAr read-out board according to a ”standard” interface setup defined by the groups involved in the camera trigger (IFAE, UCM-GAE, CIEMAT, DESY, INFN

Pisa and NECTAr). This interface uses common trigger mezzanines, namely L0 trigger, L1 trigger and (in the case of the analogue trigger) L1 distribution. The latter is plugged onto the backplane card and manages L1 triggers coming from adjacent module and the distribution of the L1Accept signal to all the modules within the region of interest. The backplane of the first NECTAr module prototype was only compatible with the analogue trigger scheme. The next module prototype will also be compatible with the digital trigger scheme.

As explained in section1.1.3, the coincidence in time of the camera trigger of several telescopes has to be examined before the data are actually read-out. To do this, one has to distribute a clock over the whole array. The concept for clock distribution is described in section 1.3.4.

1.3.1 Analogue trigger scheme

The Analogue Trigger (AT) scheme implements the Analogue Sum Trigger concept for the trigger of CTA telescope cameras [11], already proven on the MAGIC Telescopes.

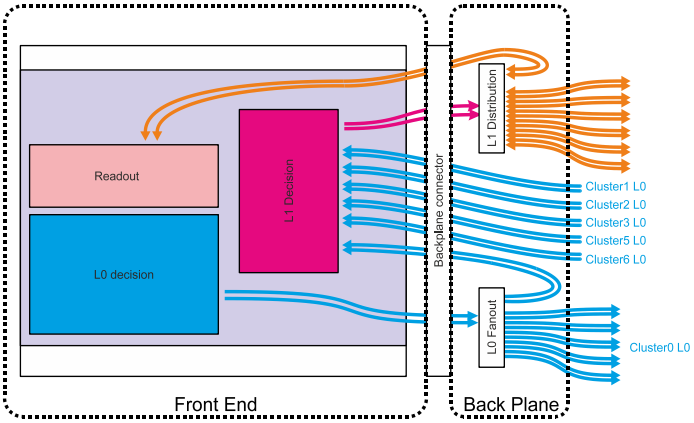

Figure 11: Layout of the analogue trigger system

The AT concept is implemented in three stages. The first one, the level 0 trigger, built in each front-end board, performs the analogue sum of pulses from the individual pixels in a module. Prior to the summation, each signal is fed into an adjustable analogue delay line (allowing for pulse shifts between 100 ps and 5 ns), in order to cope with the varying transit times that the CTA PMTs might suffer when different HV setting are required. The signal then passes through attenuator and clipping circuits (both slow-control adjustable), the former allowing to equalise all pixel gains and the later cutting signals greater than a given value, and therefore limiting the influence of after-pulses from the PMTs. The L0 signal from each module must be distributed to all 6 adjacent modules so that the level 1 trigger decision can be taken (see below). Such L0 distribution is performed by making 6 exact copies of the L0 signal in the backplane of a given module, and then interconnecting this backplane with its 6 neighbours. The second stage, the level 1 trigger, which is the final camera trigger and is also built in each front-end board, calculates the analogue sum of the L0 signals for all possible compact trigger regions of a given geometrical size, thus guaranteeing their full overlap in the whole camera. The level 1 trigger generates the L1Accept signal if the output of such an analogue sum exceeds a given threshold. The current design is able to work with trigger regions of 2, 3 or 4 modules (14, 21 or 28 pixels respectively), slow control selectable. There is one level 1 trigger subsystem in each module, which is in charge of all the required analogue sums, so that all possible combinations of compact clusters are covered in the whole camera. This subsystem also includes the on-line calibration scheme for the analogue delay lines placed at the entrance of the level 0 trigger. The scheme is based on minimising, for each individual pixel, the difference in arrival time between the output of the level 1 trigger signal corresponding to a calibration event and the digital signal corresponding to the external trigger signal driving that event.

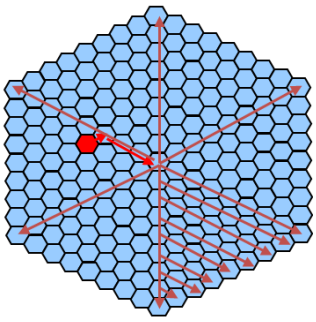

Figure 12: Example of L1 distribution paths in the camera

The level 1 trigger signal feeds the third stage, the Level 1 Distribution subsystem, placed on the module backplanes, which isochronously (within 1 ns) distributes the L1Accept signals to all modules, thus fulfilling a requirement of the NECTAr digitisers. The proposed distribution system is based in a non-centralised distribution network, which includes a set of distribution modules, one per NECTAr module, based on a low-cost FPGA, with each distribution module connected only to its 6 immediate neighbours. In order to perform the isochronous distribution, once a given NECTAr module produces an L1Accept signal, it is sent to the required neighbours so that, after specific delays, it reaches the central module (see example shown in Fig. 12). Once there, it is distributed to all the camera modules after appropriate delays, so all L1Accept signals reach all NECTAr boards within 1 ns of each other (see Fig. 11). Additionally, when the L1Accept signal arrives to the central module, it is also delivered to the central trigger and clock module. The L1 distribution subsystem can also be used, with no additional hardware, to distribute all the relevant clock and external trigger signals to all the NECTAr modules. Finally, in order to tag regions of interest (ROI) in the camera for autonomous read-out (like in the Colibri concept), the level 1 trigger subsystem is able to produce two L1Accept signals based on two different threshold levels. In turn, The level 1 distribution subsystem is able to handle these two signals, with their appropriate delays, so that ROI read-out is possible.

1.3.2 Digital trigger scheme

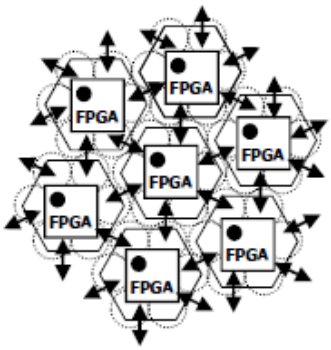

Figure 13: Grouping of 7 different NECTAr modules in the digital trigger system

The digital trigger (DT) scheme is based on the L0-signal processing of overlapping 49 pixel regions. The L0 signal, in the digital trigger scheme, is the output signal of the PMT pulse discriminators. A single low cost FPGA distributes the 7 discriminator output signals of a module to its 6 surrounding modules (see fig. 13). In parallel, it receives the corresponding signals from the 6 surrounding modules.

The digital trigger board, mainly hosting the trigger FPGA and cable connections, is plugged to the modules backplane. Flat cables of about 35 mm length are used for the bidirectional connections to the surrounding NECTAr modules.

The trigger factory, main part of the FPGA firmware, processes 49 L0 signals. Various trigger algorithms can be used. For simple ones, e.g. 3NN, the FPGA can be run in an asynchronous mode. This way a signal overlap of 1 ns is sufficient to produce a trigger. More complex modes, like time distributed trigger, require the

FPGA to run in a synchronous mode. In this case the FPGA clock is 400 MHZ.

The L1 trigger signal can be passed into three directions. Firstly, to the FPGA of the NECTAr front-end board, initiating the analogue pipeline read-out. Secondly, the L1 trigger information (up to 3 bits) can be transferred to a central trigger board via a low cost cat5 Ethernet connection. From there a loop back connection (same cable) would initiate the module's analogue pipeline read-out either for all or for a certain number of modules. Thirdly, the signal pairs $\text{trig}_{in}[]$ / $\text{trig}_{out}[]$, part of the cable connection to the surrounding NECTAr modules, can distribute the trigger information to the neighbour modules in a daisy chain way. Similar to the AT scheme, regions of interests can be defined.

After power on, the trigger scheme gets loaded into the DT FPGA from a serial PROM (Programmable Read Only Memory). However, the trigger scheme can be updated within less a second by the on-NECTAr-module FPGA, using the available Ethernet connection, at any time.

Beside its simplicity and flexibility, the FPGA approach of the digital trigger has another advantage: Each of the 49 L0 signals has to pass its individual delay line, as shown on Fig. 14, before entering the trigger factory. In case of a XILINX Spartan 6 or 7 FPGA, the individual delays can be adjusted in steps of 50ps. Provided a periodically pulsed central laser diode is available, the DT FPGA can run an auto calibration cycle, initiated by the NECTAr module FPGA.

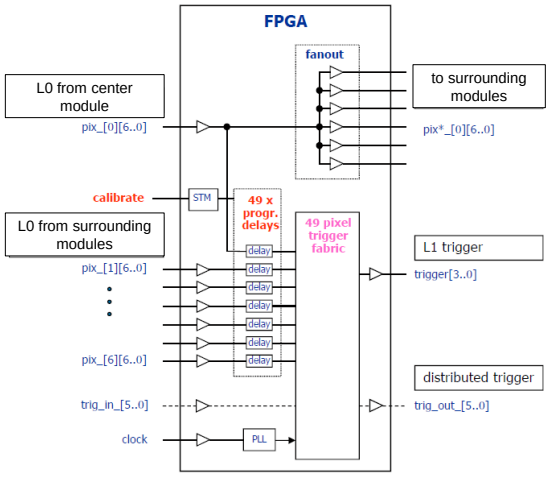

Figure 14: Layout of the FPGA used for the digital trigger system

1.3.3 Colibri scheme

Colibri (Concept for an Optimised Local Image Building and Readout Infrastructure) is a proposed alternative readout concept for CTA cameras, with a flexible readout control based on local triggering information. Here, instead of reading the whole camera at the same time after a camera trigger event, local triggers are used to control the readout behaviour of the camera's clusters independently and to define if and when each channel is read. The performance of this flexible readout is being studied with Monte-Carlo simulations; a possible technical implementation for NECTAr-based cameras is under development.

1.3.3.1 General concept

In the Colibri concept, readout regions are defined locally: A local trigger above a certain threshold tags the surrounding clusters for readout, and defines its readout time. Readout is only performed in case of a sufficiently strong "camera trigger" from the same event, distributed to all clusters; in the absence of a camera trigger within a certain time period, the clusters are not read, and no dead-time occurs. The two-level trigger system (either using a second threshold or a combination of local triggers for the camera trigger) allows separate control of the camera triggering rate (global trigger) and the image coverage (local triggers).

1.3.3.2 Possible implementation

Depending on the choice of camera electronics, implementations can vary, as long as it is possible to define the readout region and charge integration window without actually reading the sampled image charge. One

possibility is shown in figure 15 for a two-level threshold system: Here, high-level triggers (L1) enable readout in the whole camera for a certain period of time, during which triggered clusters (at a lower threshold, L1') can initiate readout of the surrounding clusters around their own triggering time. To compensate for the latency and the distribution time of the enable signal to all clusters in the camera, the local L1' triggers are being delayed by a programmable amount.

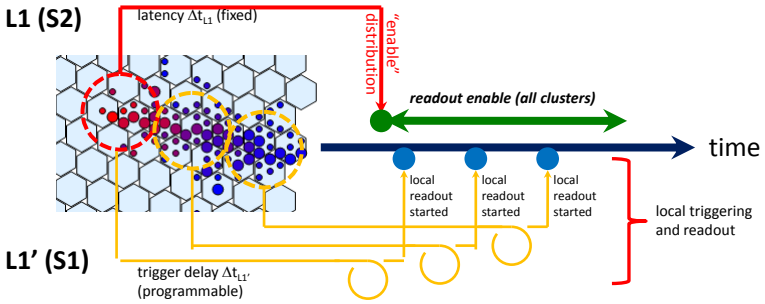

Figure 15: Sketch of a possible implementation of colibri readout in a two-threshold system, showing the local (yellow) and global (red) trigger distribution.

1.3.4 Central trigger, clock distribution

1.3.4.1 Introduction

The flexible concept for the array trigger of CTA presented in this section is based on the distribution of a clock from a central point, the time-tagging of the telescope events at the telescope level, the sending of the time-tags to a central crate where the correction of the differential delays due to the pointing direction can be carried out and coincidences be determined flexibly using software routines. This concept also allows for an easy reconfiguration of the coincidence strategy, to allow for the use of sub-arrays for CTA. Communication between the central array trigger hardware and logic are handled by serialiser-deserialiser pairs (SerDes) over dedicated fibre-optic links (10 MHz), with similar "MUTIN"[1] (multi-use telescope interface) cards at each end of the links, with two bi-directional links for each telescope, one for clock and the other for trigger. This can be implemented either with a bi-directional link (preferentially) or with two separate optical fibres.

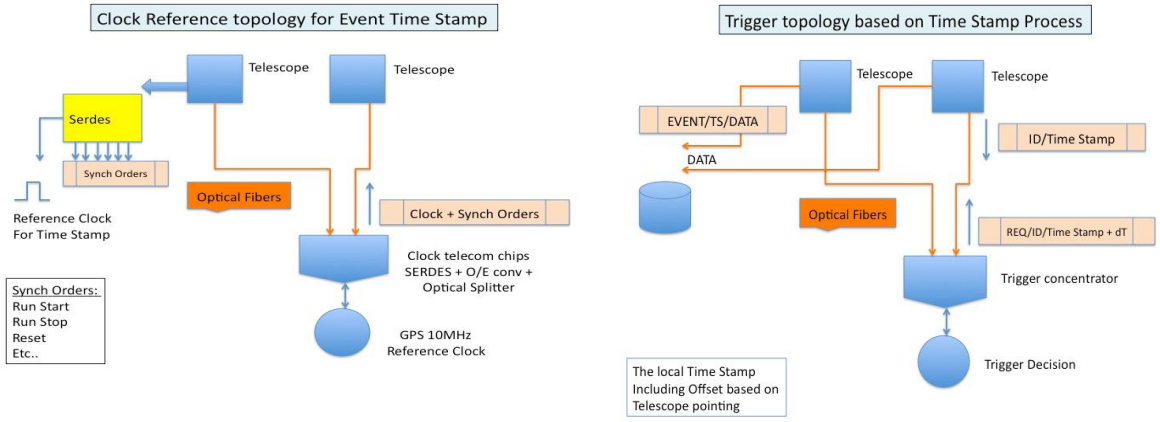

Figure 16: (a) the topology of the clock reference transmission from the central reference clock (b) the topology of the trigger concentration, in which the telescopes send ID/timestamps for each event, and the trigger decision module returns orders on which event data are to be transmitted (rather than being skipped)

[1] developped in the context of the GATE project, a prototyping platform for CTA in France

1.3.4.2 Summary of architecture

The scheme consists of two parts, firstly the reference clock distribution and secondly the trigger collection and distribution, which should be implemented in two crates co-located at the central part of the array (control building). The reference clock is a GPS in the central clock crate, from which the 10 MHz signal and 1 PPS are distributed continuously to all telescopes over the clock link. The array trigger crate collects the streams of event time stamps from each telescope, which it communicates to its CPU. The CPU determines the coincident events, and provides the stream of time stamps of the events which are to be retained, which it sends back to the telescopes over the trigger link. The telescope side card receives the clock signals from the central side, and passes these on to the camera DAQ (in particular, the local trigger module) to allow time stamps to be formed. It receives from the local trigger module the stream of time stamps of local event triggers, which it sends to the central side. From the central side, it receives the stream of time stamps for events to be retained, which it passes on to the Camera DAQ. The overall schematics for the reference clock and trigger distribution are shown in figures 16 (a, b), respectively.

1.4 Data acquisition system

The data acquisition (DAQ) system shown in Fig.17 fits the basic assumption of 271 front-end electronic modules (for 1897 pixels in one camera), which are providing data to a UDP server over an internet protocol (IP) connection.

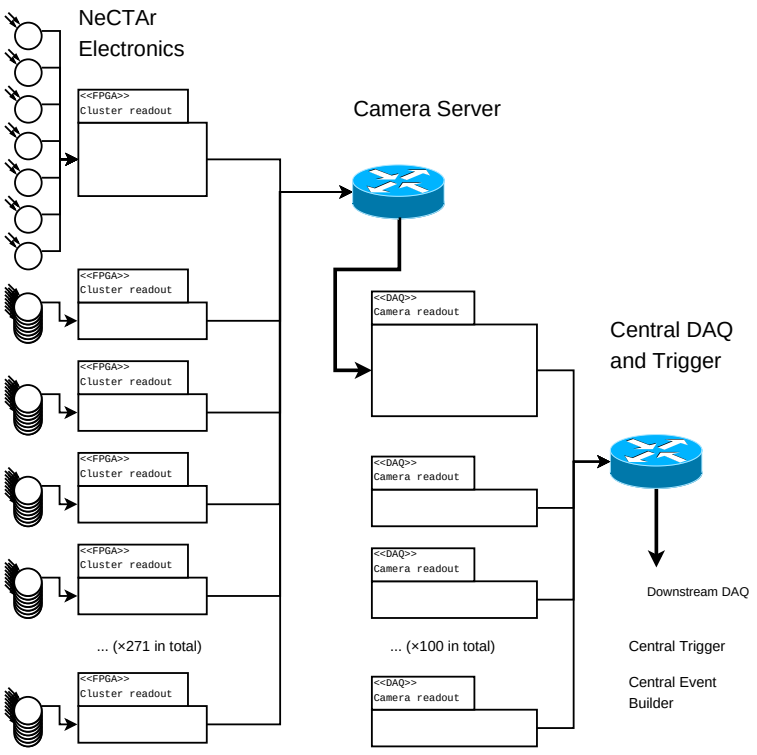

Figure 17: Software architecture between the front-end (left) and the central downstream DAQ (right), connected by means of fast switches and the camera server PC

The same IP connection is used for data transfer in the slow control (SLC) domain, which is negligible in size with respect to the DAQ data. In order to keep a vital minimum of computing power in proximity of the telescope, the present approach assumes:

- Concentration of IP connections from groups of ca. 46 NECTAr modules in multi-1-Gb[2] switches inside the camera
- 20 Gb interconnection of several level-3 switches with fast interlinks
- IP downlink from the switches inside the camera to a camera server used also as an event buffer.
- 10 Gb downstream connection from the camera server to the central DAQ.

[2]Gb = 1 Gigabit (implicitly read: “per second”)

Although this requires rather sophisticated types of hardware, it is assumed that COTS (commercial off the shelf) systems can be used to achieve the system's needs at lowest cost. Connections between the front-end electronics and the switch(es) are carried out in 1000baseT Ethernet technology, whereas two parallel uplinks to the server are realised as SFP+ (10 Gbps) wire connections.

Downstream DAQ has been developed by ISDC Geneva and presented in the CTA ACTL working group. The DAQ software will be interfaced to this software as well as a central array control scheduling system via ACS. Tests have been carried out with COTS elements (DELL T7500 server and DELL PowerConnect 6248 switch) in order to verify their usability at the nominal rates as well as evaluating their maximum performance with the current software design. Up to 300 UDP clients have been simulated with simulator programs (called "DAQ stimulators") generating data of any format in general and data in the format expected from the NECTAr front-end electronics in particular. The event-builder code can switch dynamically from one data format to another, not only for maximum compatibility between different front-end hardware types, but also to correctly handle different event types on the fly, for example compressed and full-sample format for gamma-ray and calibration / noise events respectively.

1.5 Focal plane

This section deals with the collection of light and transformation into photo-electrons. The light collected by the mirrors of the Medium Size Telescopes is focused on the focal plane. The light is collected by light guides before reaching the photodetectors (section 1.5.1). The photodetectors convert the light into a current (section 1.5.2), which is amplified before reaching the FEB (section 1.5.3). The HV of the photodetectors is controlled by an independent board, described in section 1.5.4. This board is plugged directly into the FEB.

1.5.1 Focal plane optics

Each PMT is equipped with its own light concentrator (LC), whose main functions are to maximise the amount of energy collected by the non-contiguous photo sensitive areas of the PMTs, and to block stray light originating from the terrestrial environment. Fig 18 shows simulation results for 2 types of light concentrators: a Winston cone and a less standard plano-convex lens.

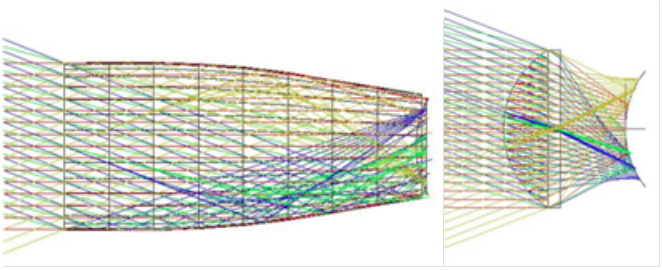

Figure 18: Optical simulations (ray tracing) for two different types of light concentrators: a Winston cone (left) and a plano-convex lens (right). The entrance/exit windows have 5cm/3cm diameter respectively. The rays of light shown in each case cover an entrance aperture angle of $\sim$ 20 deg. i.e. the aperture angle expected for a MST telescope

1.5.2 Photodetectors

The baseline photo-detector for the NECTArCam camera is a high quantum efficiency 1.5 inch PMT, such as the R11920-100 from Hamamatsu, operating at low gain (5 10^4 compared to 2 10^5 for H.E.S.S) to minimise the ageing effect. The choice of this photo-detector was suggested by the CTA FPI workpackage (see reference [4]).

1.5.3 Pre-amplifier (PACTA)

The fast read-out option needs a wideband, high dynamic range and low noise pre-amplifier, attached to the photosensor and connected by a cable or transmission line to the front end electronics. Table 3, summarises the pre-amplifier requirements. Since the PMTs operate at low gain, achieving good SPE resolution imposes strict low-noise requirements.

Noise	ENC $\leq$ 5 ke
Dynamic range	From $\leq$ 1/10 of SPE to 3 kSPEs: $\geq$ 15 bits with $\leq$ 3 % nonlinearity
BW	500 MHz. Total BW including FE must be 300 MHz
Input impedance	$\leq$ 20 Ω Low pick-up noise and high BW:
Low power	About 100 mW with low impedance driver (cable)
Reliability/compactness	Mass production, Integrated circuit, ASIC

Table 3: PACTA requirements

Current mode circuits, based on super common base or regulated cascode stages, are well suited to fulfil most of those requirements. These circuits usually offer multiple gain paths using a current mirror to replicate the input current with different scaling factors. However, large currents saturate the input branch of the mirror, and DR is in practice limited to 14 bits or less. A novel current division scheme at the very front end part of the circuit is used to split the input current in two or more scaled output currents which are connected to independent current mirrors. The mirror of the high gain path comprises a dedicated saturation control circuit needed to assure an accurate current division. Two ASIC prototypes have been designed in AMS SiGe BiCMOS 0.35μm technology.

The PMT input current is split in the common base input stage into two (or more) output scaled currents. Then each current is read out with a dedicated current mirror, which can be optimised for different performances. Finally, the current signal is converted to voltage by a closed loop trans-impedance amplifier. Figure 19 shows the block diagram of the complete pre-amplifier for CTA (PACTA) ASIC [9], for the differential implementation. Table 4 summarises test results of the second version of PACTA. Good single photo-electron resolution is achieved with a PMT candidate for CTA, at a nominal gain of 4 10^4.

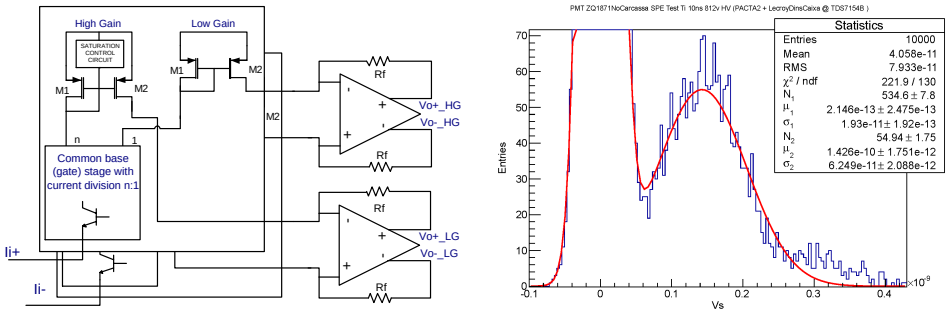

Figure 19: Left: block diagram of PACTA. Right: single photo-electron spectra obtained with PACTA and a calibrated PMT candidate (R11920-100-01) operated at nominal gain (4 10^4)

1.5.4 Concept for generation, control and monitoring of HV

The baseline high-voltage (HV) power supply of the PMTs is derived from the system that has been developed and is employed for the H.E.S.S. experiment. Having (by definition) a TRL of 8 (defined in table 7), the H.E.S.S. HV power supply shows a very low failure rate (few/1000 over several years) and an excellent stability (see appendix 5.3). The NECTArCam HV concept has been developed in the framework of the NECTAr project, in collaboration with ISEG (http:www.iseg-hv.de), an industrial partner specialised in high voltage systems, who has provided the HV power supply for H.E.S.S. I and II. The main drivers behind this development were the production of a cost efficient, reliable (in terms of stability and low failure rate), testable and maintainable HV system.

Starting from the individual HV boards employed on H.E.S.S. for each pixel, a single-board 7-channel design was devised, which integrates HV supplies for all 7 PMTs of a camera module. The board also integrates control and monitoring of the HV supply for each of the 7 PMTs through a dedicated micro-controller that is accessed via a SPI serial link. This concept allowed a reduction by more than a factor of 14 of the number of boards, connectors and cables required to power and to control the PMTs, considerably improving the simplicity and

Parameter	Result	Comments
BW	500 MHz	
Noise (ENC). Dif.	5 ke	10 ns int. time
Noise (ENI). Dif.	400 nA rms	
Trans-impedance HG	1.2 kΩ	
Trans-impedance LG	75 Ω	
Input impedance	<20 Ω	Adjustable
Dynamic Range	16 bits	
Relative linearity error	≤ 2 %	(Charge meas.-fit)/fit
Output swing over 50 Ω (AC coupling)	1.4 Vpp	Differential output
Output swing over 50 Ω (AC coupling)	0.8 V	Single ended output
Power consumption 3.3 V operation	120-150 mW	2 diff outputs. (HG/LG)
Power consumption 3.3 V operation	80-100 mW	2 S.E. outputs. (HG/LG)

Table 4: PACTA performances

maintainability of the system with respect to H.E.S.S. In addition, the production costs with respect to H.E.S.S. are divided by a factor of 2 (from currently 60-70€per channel for H.E.S.S. to 34-38€per channel for CTA, assuming production for 130k channels). Figure 20 shows the current version of the HV board together with the integrated PMTs and mechanical support structure. The specifications of the ISEG board are summarised in Tables 5 and 6.

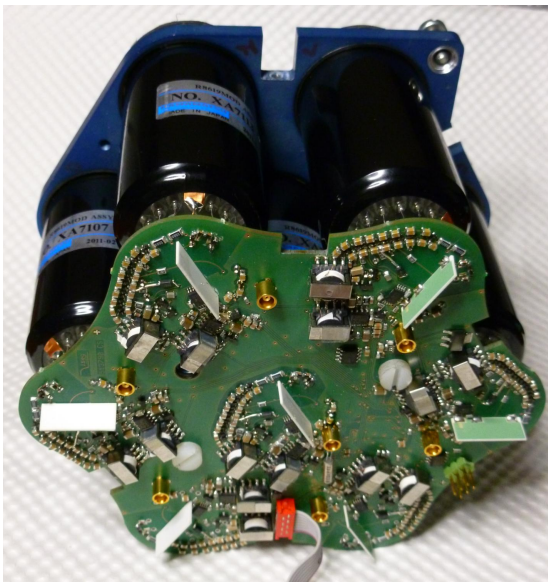

Figure 20: ISEG HV board integrating the 7 HV power supplies

1.6 Mechanics and cooling concepts

This section describes the mechanical structure of the camera. As explained previously in section 1.1.2, the NECTArCam camera hosts 271 modules of 7 pixels, to meet the 8° field-of-view requirement of the level B specification document[2]. These modules are supported by a "sandwich" structure. The mechanical support of the modules, described in section 1.6.2 are threaded in the sandwich structure. The cooling of the electronics, described in section 1.6.3, gives additional constraints on the mechanical structure.

Parameter	Type	Specification
High voltage	/ pixel	0 to 1600 V
HV stability	/ pixel	$\leq 10^{-4}$
HV variation with T	/ pixel	$< 5\ 10^{-5}$ / °C
Ripple	/ pixel	≤ 10 mV
Max power	/ pixel	400 mW at 1600V
Power supply		Single 12V DC
Slope		$\sim$ 5V / ms
Anode signal	/ pixel	MCX connector for coaxial cable

Table 5: Parameters of the ISEG HV board

Parameter	Type	Specification
Usoll / pixel	/ pixel	0 to 4 V for 0 to 1600V (via serial link)
HV on/off /pixel	/ pixel	SPI serial link
Uis (HV value)	/ pixel	Via serial link
Iis (Current value)	/ pixel	Via serial link
HV status	/ pixel	Via serial link
Over Current protection	/ pixel	YES
Over Voltage protection	/ pixel	YES
HV man : Force HV to 0	/ 7 pixels	Separate pin of the connector

Table 6: Controls, monitoring and safety of the ISEG HV board

1.6.1 Camera mechanics

The mechanical design of the NECTArCam camera aims at meeting the desired specifications, such as the weight, stiffness and reliability, and to facilitate an industrialised production. It is based again on the experience gained in designing and building the H.E.S.S cameras. One difference with the H.E.S.S camera is the requirement that the camera be sealed.

Fig. 21 shows the main elements:

- the skeleton
- the sandwich
- the skin (including lids)
- the front-end modules
- the electronics rack

The optimisation tasks are naturally grouped into two types of mechanical work, the first in design and calculation, and the second in implementation and prototyping.

The calculation results will be tested by building prototypes; if necessary, a re-design might be initiated following the experience gained by the tests.

The structure of the cameras must be designed to meet a number of mechanical goals, such as protecting the delicate optical elements from the harsh environment or having sufficient rigidity to allow the full camera to be removed. The type and the amount of material used to build the cameras must be optimised to ensure its resistance to mechanical or thermal stresses to which it is submitted.

In the latest designs, the technique of aluminium profiles has been used for designing easy-to-implement solutions that meet the requirements. Many functions can be integrated into a section facilitating the machining and the assembly. The spinning of aluminium provides solid sections with many different shapes, tubular or semi-tubular, or even more complex.

The proposed simple architecture is made with a tubular structure, the sides being covered by a skin, and lids are available at each edge. The front part includes the entrance window, the funnels plate and the

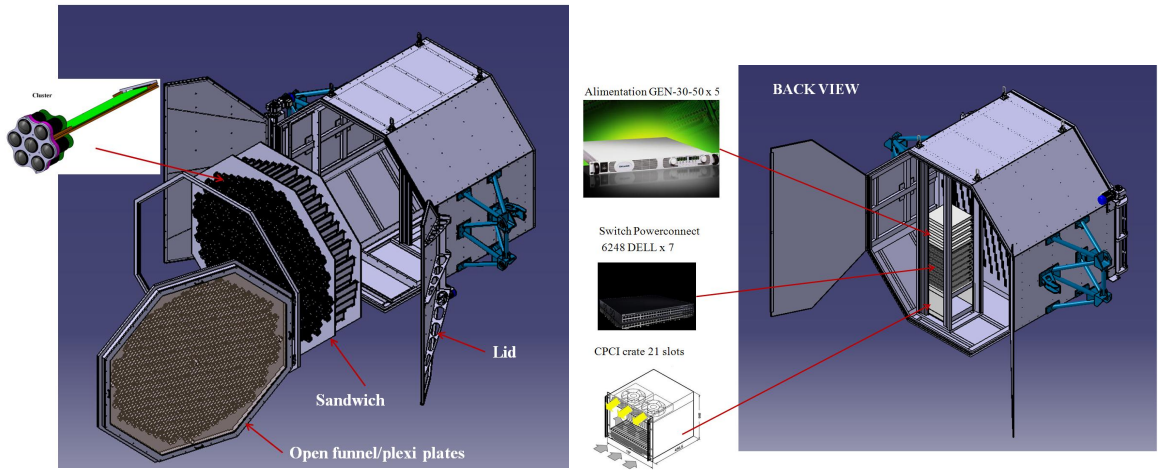

Figure 21: General camera layout. Left panel: Front view showing the sandwich and one module. Right panel: Rear view with the SLC/DAQ electronics.

sandwich structure housing the modules. At the rear a single rack, placed in the central part, houses the rest of the electronics made of a cPCI crate (for slow control, safety, optionally camera server and event buffer), 6 switches of 48 ports and power supplies. Additional space is still available for auxiliary systems such as power distribution, lightning protection or others. More detailed drawings are given in the annex 5.2.

1.6.1.1 Maintenance

The reduction of the maintenance (regular and repair) places a serious constraint on the design and the cost estimates. The regular maintenance could be done while mounted on the MST telescope with an angle of ~ 20 degrees. The repair maintenance is either done on the telescope (but in this case a shelter might be needed), or the camera is removed and a spare one is used as replacement. In both cases, the impact on design and cost of both solutions for the maintenance scheme has to studied.

1.6.2 Module mechanics

As stated in section 5.2, the general concept of the NECTAr module involves a single read-out board for 7 pixels including the amplifiers, sampling and read-out electronics, a standard Ethernet interface for data transfer, a single power supply and an integrated trigger.

This modularity implies a structure which allows an easy splitting of the PMTs and HV part and read-out part, allowing an easy replacement of each part for maintenance or future upgrades. The first NECTAr module prototype is shown in Fig. 26.

An improved design with the required CTA photo-multipliers spacing of 50 mm (from level C requirements [3]) is now available and is shown in figure 22. The total weight of the module is 1.64 kg (see table 10.

1.6.3 Cooling system

The temperature of the camera is recommended to be less than 50° (see reference [5]) to avoid a rapid aging of the electronics components. A preliminary thermal study has been performed with a finite element method including a 3D model for a drawer module and thermal characteristics of NECTAr electronic components (sizes, temperatures). The reference external temperature used for this simulation is 22°C and the model is taking into account the influence (radiative heating etc) from surrounding modules. The results of this first simulation, assuming no specific cooling, show that the temperature of the structure is below 36°C and in good agreement with what is observed experimentally on the NECTAr test board and on a scale 1 model. This first check validates the simulation set-up and the approach used here.

Other thermal simulations are done to study the effect of radiative, conductive and convective cooling on the camera module and to define the most efficient cooling system.

First studies show that the most efficient cooling is convection with low air flow (h=10W/m.°C). The convective cooling reduces the temperature of the components, board and the module structure. The structure

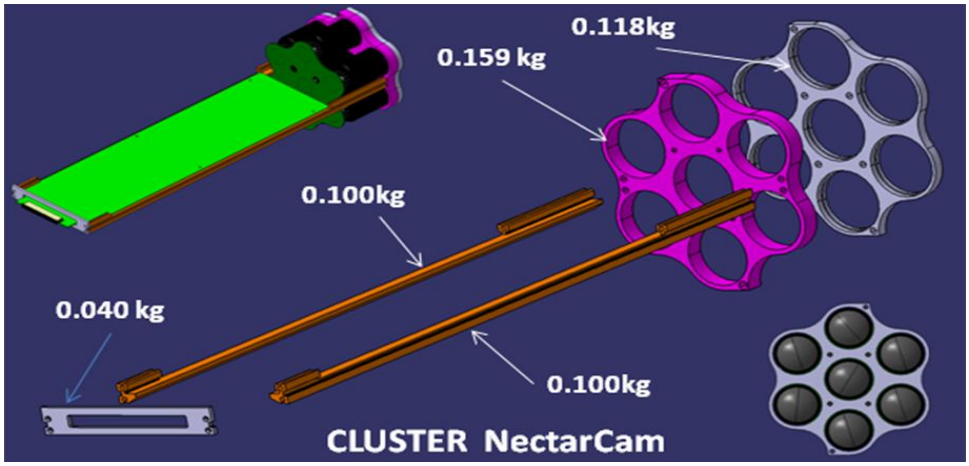

Figure 22: Module mechanical layout

temperature is 25°C and the temperature of electronics components remains below 40°C. The convective cooling would thus be sufficient to meet the recommendations of the ELEC WP. More complete simulations should be performed before starting a detailed implementation study.

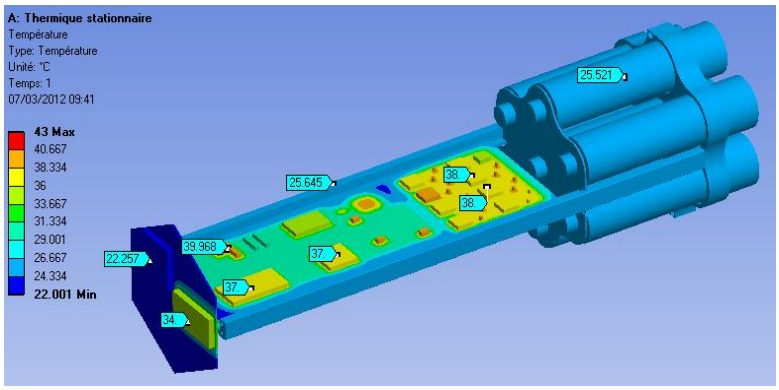

Figure 23: Simulated temperature map of components, cooled down by air flow

1.7 Slow control and monitoring

The safety and slow control aspects of the NECTArCam camera mainly consist of:

- Monitoring of the camera temperature, pressure and humidity
- Cooling of the camera (using fans, water ...) according to the ambient temperature.
- Monitoring of the ambient light, if too strong, HV will be quickly shut down to protect the PMTs.
- Control and monitoring of the camera parameters (doors, HV, Power supplies, CPU reset . ..)

Critical decisions (safety aspects) will be taken as closely as possible to the device in a standalone local FPGA and then reported to the global safety system. This FPGA will have the possibility to be independent of the DAQ and to switch the power supply off. Concerning cooling and humidity control, a quick response is less critical and will be driven either locally or from remote system in the ACTL framework.

The calibration system of the camera also includes several LEDs for focal plane positioning. The light of each LED will be individually adjustable through digital to analog converters (DAC) and seen as a point source from the CCD system located in the centre of the telescope mirrors. This set-up will be used to calibrate precisely the position of the Winston cones relative to the telescope. Indeed, the camera position depends, among others factors, on mechanical deformations varying with the pointing of the camera, external temperature and wind.

The calibration part will also include:

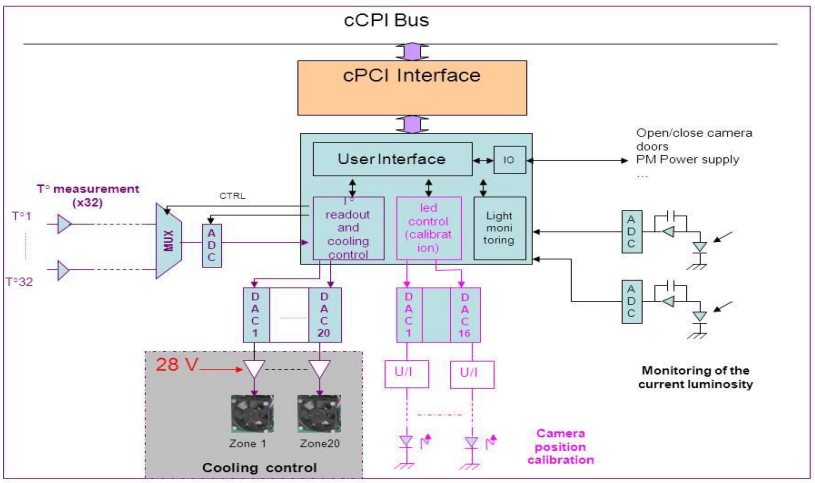

Figure 24: Functional diagram of the safety and slow control solution used for the H.E.S.S. 2 Camera

- The control of the LED obstructing system placed on the doors
- The control of the mylar film (position either on the lid or the camera front doors) for the single photo-electron measurement (gain calibration).
- The control of the reference external PMT for the single photo-electron measurement (gain calibration).

The safety, slow control, monitoring and calibration electronics can be placed in a crate, as done for the H.E.S.S. 2 experiment. In this case, the crate will be chosen with respect to the collaboration standards. The hardware implementation of the safety and slow control system done for the H.E.S.S.2 camera is shown in Fig. 24. The humidity part is not shown since it was not included in the H.E.S.S. 2 camera.

The system proposed for the NECTArCam is thus based on what was designed and built for the H.E.S.S.2 camera.Indeed, its architecture is flexible enough to accommodate new developments or new devices.

1.8 Calibration

The major parameters that are critical for camera performances from the calibration point of view are pedestals, flat-fielding, gain calculation and single photo-electron pulse height spectrum.

The most cost-effective and reliable solution to perform these calibrations is probably to use a multiple light level calibration unit. This is a system of several LEDs, using a simple gate, regenerative switch or bipolar driver/pulse-shaping circuit design. This light source should be relatively bright ($> \sim 30$ pe per pixel) to minimise the influence of shot noise. The system proposed for the NECTArCam camera has the advantage that it can also, with slight modifications, be used for other telescope types (LST, SST) by adjusting the angular coverage and brightness as needed.

The key element is a modular system where any of the individual measurements can be done in a dedicated manner. The base element is shown in Fig 25. An appropriate LED is mounted in a shielded support. The baseline characteristic of the LED should be:

- UV Range : 300-500nm
- low consumption (few mW)
- nominal brightness >3000mcd
- power angle > 40% at 6 degrees

Depending on the final design, different wavelengths could be used in different individual housings. To accommodate all calibration modes described above, a series of these modules would be mounted on a circular structure. Each of these individual modules would operate in a dedicated mode: either flat-fielding, single p.e. or gain mode. There are three possible scenarios to trigger the camera for calibration: a dedicated PMT, a camera PMT or an external trigger sent to the camera via an optical fibre.

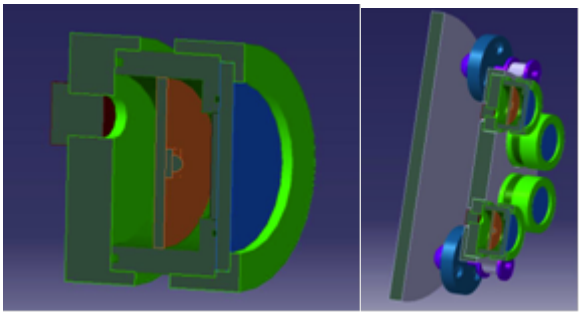

Figure 25: LED module (right), incorporating a single UV LED, externally triggered. On the left a complete calibration source providing a total of six possible measurement combinations.

TRL	Definition
1	Basic principles observed and reported
2	System concept formulated
3	Characteristics proof of concept
4	Component validation in laboratory environment
5	Component validation in relevant environment
6	System prototype demonstration in relevant environment
7	Actual system completed and qualified through test and demonstration
8	Actual system proven through successful operations

Table 7: Definition of Technology Readiness Levels employed in this document

2 Status of the development work

2.1 Overview of components to be developed

2.1.1 Definition of Technological Readiness Levels

The status of the NECTArCam development work is estimated with the help of the technological readiness, defined in 8 specific levels (TRLs), which are summarised for reference in Table 7. The NECTArCam concept derives from the existing and well-proven camera concepts deployed for H.E.S.S. I (TRL 8) and H.E.S.S. II (TRL 7), and components are being adapted and/or optimised to meet the needs of (industrial) mass production and reliability required to operate a large research infrastructure, such as CTA.

2.1.2 Technological readiness of NECTArCam components

The TRLs of all NECTArCam components are summarised in Table 8. The legacy of each component is also identified, specifying from which existing product the actual component is derived.

2.2 Status of implementation work on components, including firmware and software development

2.2.1 Focal plane optics

Work is currently under way to provide specification document concerning the light guides. A first version has just been submitted to members of the consortium for validation. In parallel, ray-tracing simulations are being done at IPAG. Two different options are currently being studied (see Fig. 18): hollow Winston cones and lenses. The former solution is well known and already used for Cherenkov telescopes cameras, and will be optimised for CTA (cone/lens design, cone coating). The addition of an entrance window (e.g. in optical quality transparent polymer like PMMA or others) in front of each cone or each drawer (to protect the camera from dust) could also be envisaged. The 'lenses' concept is a new concept that should have the advantages of a good transmission and durability. Moreover, the lenses system would isolate, by itself, the camera from dust. Preliminary simulations

Item	TRL	Legacy
Focal plane equipment		
Light guides	4 to 5	Similar concept used in MAGIC and H.E.S.S. I
Entrance window	4 to 5	Concept validated by MAGIC
Photo-detectors	3 to 4	CTA candidate
Pre-amplifier (PACTA)	4	Integration work with HV under evaluation
HV power supply (ISEG)	4	HE.S.S. I and II HV boards
Front-end electronics & trigger		
Front end architecture		H.E.S.S. cameras
Analogue pipeline (ASIC)	4 to 5	Similar chip used for H.E.S.S. II
Front-end board	4 to 5	Tests done with full chain from PMT to GUI
NECTAr Backplane card	4	Discussion ongoing to design common CTA BP.
Analogue trigger (AT)		Similar concept used in MAGIG and H.E.S.S. l
AT L0 trigger	4	6 prototypes functional
AT L1 trigger	4	5 prototypes fully functional
AT L1 distribution	4	12 prototypes fully functional (incl. Firmware)
AT CLK distribution	4	12 prototypes fully functional (incl. Firmware)
AT backplane	4	Concept of super backplane under evaluation
AT delay lines	3	Concept under evaluation
Digital trigger (DT)	3 to 4	prototypes available
Camera processing & monitoring		
Camera DAQ	3	
Camera slow-control & monitoring	4	
Camera trigger	2 to 3	
Power	2 to 3	
Calibration systems	3	
Safety	5	Similar design implemented in H.E.S.S. II
Camera mechanics & cooling		
Embedded camera concept		H.E.S.S. cameras
Camera telescope connection	4	
Camera body	4	Similar concept used in H.E.S.S.
Camera inside	4	Similar concept used in H.E.S.S.
Module mechanics	4	Similar concept used in H.E.S.S.
Module cooling	2	
General cooling	2	
Humidity control system	2	

Table 8: Technology Readiness Levels of NECTArCam components

give encouraging results but more precise studies have to be done to conclude on the feasibility or not of these different light concentrators options. The cost should be of the order of 20 € per channel in the case of cones. The cost for the lens concept is currently under investigation.

2.2.1.1 Future work

The plans for future work are the following

- Finalising the ray tracing simulations: 3 months.
- Contacting industrials in order to subcontract the production of prototypes + tests: 9 months
- Validation/qualification of the industrial process for mass production: 9 months

2.2.2 HV generation

Initial tests of the first prototype board have been performed in the laboratory, showing results that satisfy the CTA requirements in terms of voltage range, stability, control, and monitoring. What remains to be validated is the SPI serial link (initial tests have been performed using the inCAN-Bus interface available via USB/CAN adaptor of the HV board). The first prototype board has been equipped with 7 CTA PMTs candidates (Hamamatsu: R11920-100 R20), and single photon-electron spectra have been taken successfully.

The first HV board prototype shows a power consumption of 170 mW per pixel, which could be judged relatively large, while still being within the specifications of < 5 W per pixel when combined with the overall power consumption of the NECTAr camera modules. Additional 200mW/pixel are produced by the use of a dedicated micro-controller for slow control and monitoring, which however has the benefit of alleviating the need for additional components on the read-out board (such as ADCs, DACs, etc.) for this purpose. Nevertheless, a possibility to considerably reduce the power consumption down to 70 mW per pixel for HV and 100 mW/pixel for slow control and monitoring has been identified. New prototype boards with reduced consumption have already been delivered by the ISEG company and are currently being tested.

Further development steps will address:

- the adaption of the pixel pitch from currently 52.8 mm to the nominal value of 50 mm for CTA
- the integration of the PACTA pre-amplifier on the HV board
- the improvement of the electric interface with the PMTs in order to facilitate production, testing and integration

Note : Alternative HV power supply systems are currently developed within the CTA collaboration, and could be adapted, if required, to the current NECTArCam design. Before such an adaptation should be undertaken, however, the benefits of an alternative power supply with respect to the present baseline concept need to be clearly identified. Furthermore, any alternative solution should present an equivalent technological heritage compared to the baseline solution, to avoid taking any unnecessary technological risk.

2.2.3 NECTAr module, firmware and software

The module prototype has been assembled in January 2012 with 7 PMTs and ISEG HV board, front end board and backplane board prototypes. The integrated system was then connected to the computer running a Linux operating system and hosting the Java general user interface developed for controlling, monitoring and reading out the module. First tests using a pulsed light source and an external trigger demonstrate that the system is working and able to provide single PE measurements on each channel.

Measurements undertaken in last January show that the ACTA dual channel amplifier should be used for the mini camera demonstrator as it gives a good linearity connected to the NECTAr0 chip up to 2000 PE (see Fig. 27) with lower power consumption than commercial amplifiers. The required 3000 PE can be obtained by lowering the ACTA low gain by a factor of two. Note that commercial H.E.S.S II type preamplifiers are used on the linearity plot of figure 35. A single photoelectron spectrum measured with ISEG HV, CTA candidate PMT and ACTA amplifier connected to the NECTAr0 chip is shown on Fig. 28

First integration tests with the whole analogue trigger system have validated the hardware and software interfaces. More tests still have to be done to measure the performance of the system.

Finally, tests have been done using a CTA PMT equipped with PACTA pre-amplifier and connected to the ACTA channel of the Front end board. Single p.e. spectra have been measured at the expected CTA nominal gain of $5\ 10^4$ validating the full read-out chain (see Fig. 29).

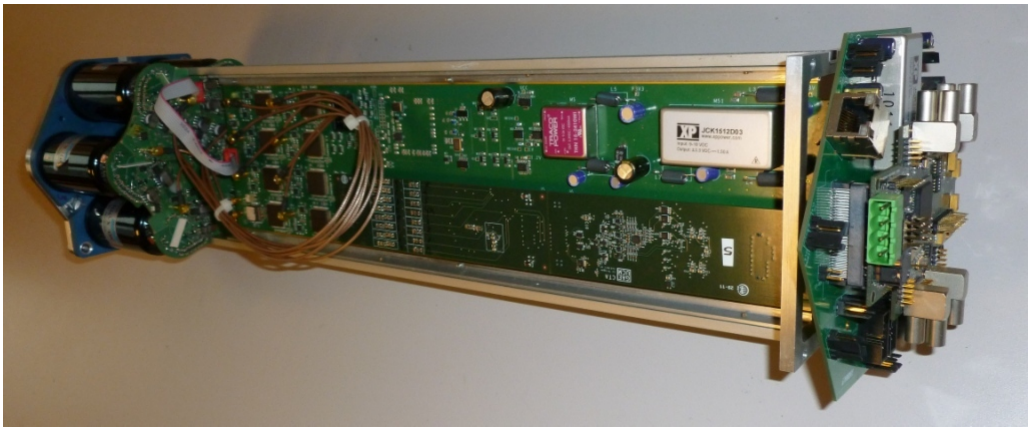

Figure 26: NECTAr module prototype

2.2.4 Trigger

In January 2012, integration tests of the analogue trigger were performed, which validated the interfaces (connectors, slow control and software), power supplies and the trigger path from L0 input signal to the L1-accept distribution. Further tests are foreseen using PMTs and light sources to characterise trigger performances at different NSB levels. As explained before, similar tests will be done in a near future with the digital trigger system.

2.2.4.1 Status of development of analogue trigger components

Most of the subsystems of the AT scheme have been fully developed, with several prototype boards already produced and tested, meeting the requirements. Only a small fraction of the elements is still under development, as shown in the following list:

- L0 Decision: 6 prototype boards fully functional meeting requirements.
- L1 Decision: 5 prototype boards fully functional meeting requirements.
- L0 Distribution: 6 prototypes fully functional meeting requirements.
- L1 Distribution: 12 prototype boards fully functional meeting requirements, including firmware, emulating the full CTA camera operation conditions.
- Clock Distribution: 12 prototype boards fully functional meeting requirements, including firmware, emulating the full CTA camera operation conditions.
- Analogue trigger backplane: key elements (L0-dist, L1-dist, Clk-dist) individually developed and tested. Design of the backplane layout, including all final components and connectors, under development. For the current prototypes, a Samtec QFS-052-04.25-L-D-A front-end-to-backplane connector has been tested and meets the electric requirements, but doubts arose concerning its mechanical stability. Tyco Z-PACK HM-ZD connectors are investigated for enhanced mechanical properties. The construction of a model to evaluate the mechanical tolerances of a "multi-module" backplane is on-going.
- Analogue delay lines: design nearly worked out, once conceptual design is finally fixed.

Current prototypes of the different AT subsystems have been produced as separate mezzanine boards, to ease testing. The next step is the design and prototyping of the AT subsystems integrated in the front-end and backplane boards.

2.2.4.2 Tests of analogue trigger components

All the subsystems of the AT scheme have been fully tested in standalone mode (except for the analogue delay lines and backplane, still in design phase), and also interconnecting all subsystems, showing a latency of 200 ns from the entrance to the L0-dec to the distribution of the L1 trigger to any module in the camera, and a trigger noise of 0.3 photoelectrons. The subsystems have also been tested in connection with NECTAr boards for hardware and firmware compatibility. A test of the full concept with 3 NECTAr boards and all the required AT subsystems will be performed before the end of 2012.

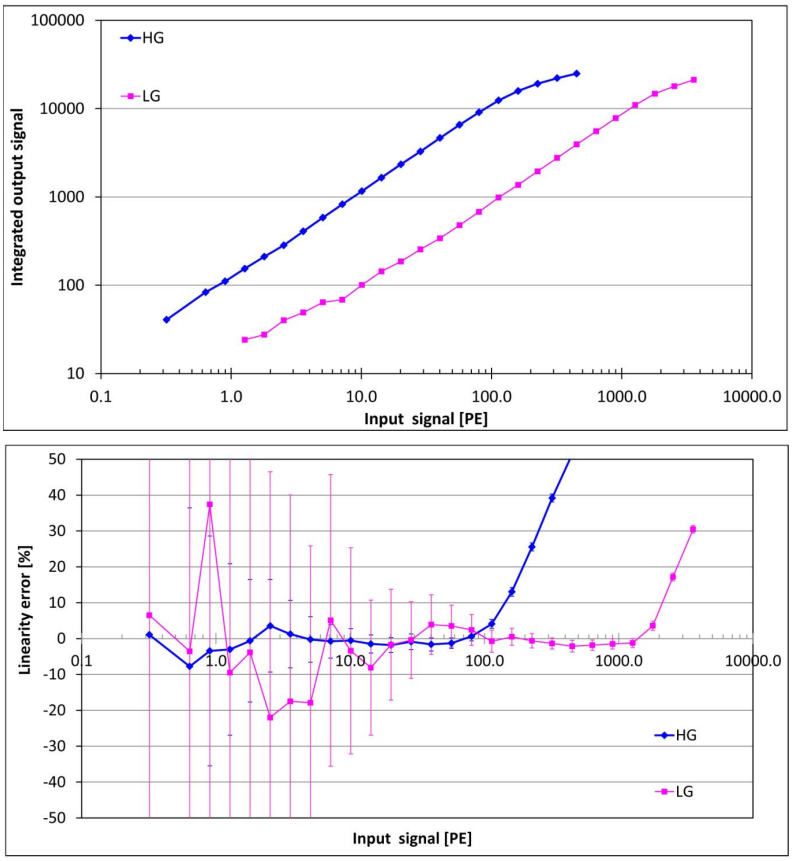

Figure 27: High gain (HG) and low gain (LG) output as function of the input signal. The ACTA preamplifier was used. The required 3000 PE can be easily obtained by lowering the ACTA low gain by a factor of two. The charge is computed as the integral of 16 samples.

The Clk-dist has been tested in standalone mode, measuring a jitter increase of 5ps from input to output in the 10 MHz clock, complying with NECTAr requirements.

2.2.4.3 Digital trigger components

A prototype of the digital trigger card is available and tests are ongoing. The next step will be to validate hardware and software interfaces with the next NECTAr module prototype and then start tests of the whole system in order to evaluate the performance.

2.2.5 Array trigger, clock distribution

The implementation for the tests has been made using MUTIN cards in standard PXI format, placed within a PXI crate from National Instruments, including CPU and GPS modules (see Fig. 30). The MUTIN card has two FPGAs for carrying out its computational and control functions, and an EPLD for timing and clock functions. In this implementation, the MUTIN card with the optics daughter cards should use 4.2 W of power, powered solely by 3.3 V, and for a unit cost of $\sim$ 1 €. The communication is carried out over optical fibre using optical daughter cards currently custom-built using discrete components and mono-directional fibres (100 MHz, 850 nm), but in the next step with commercial bi-directional modules with a single multi-mode fibre per communications link.

2.2.6 Mechanics

A "dummy" camera (that is not instrumented) is being designed for the first MST prototype and built in the framework of the GATE project. The interface between the camera mechanical structure and the telescope quadrupod is shown in Fig. 31

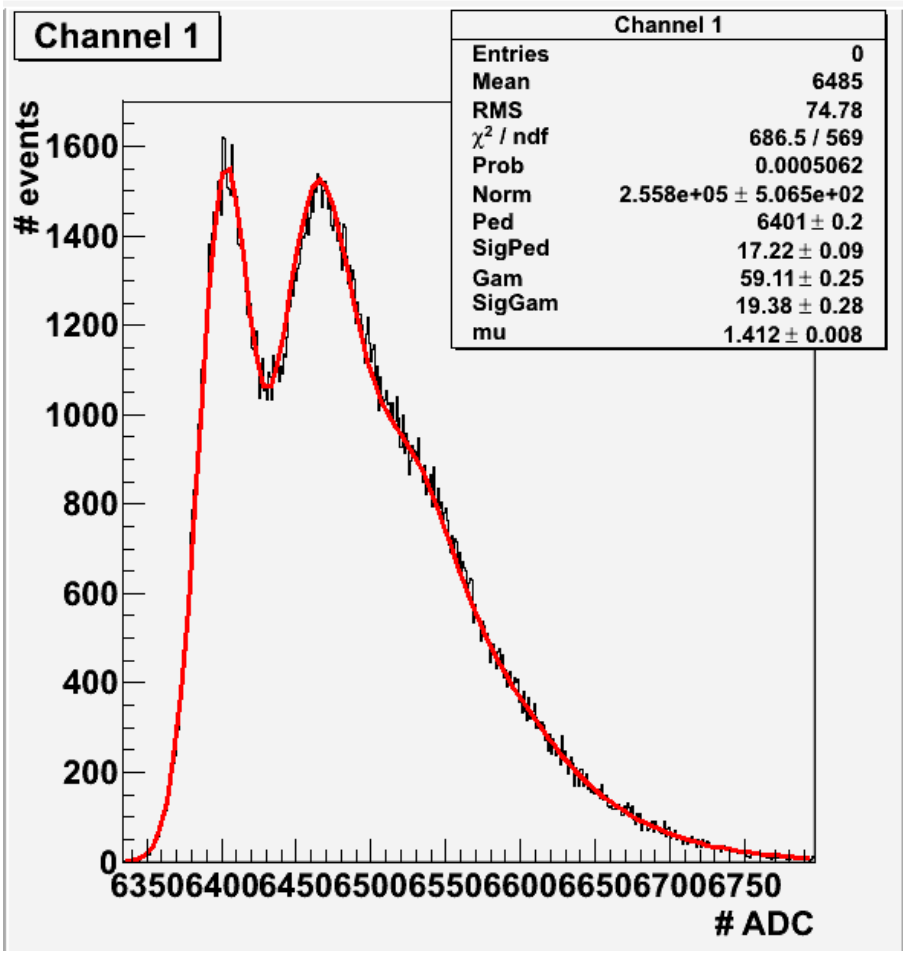

Figure 28: Single PE spectrum with ISEG HV board, CTA candidate PMT using ACTA channel on the NECTAr module prototype

2.2.7 Data acquisition system

In a first series of tests, 300 stimulator software agents have been developed on ten servers, each of them equipped with two 1000baseT Ethernet switches respectively. The test setup is shown in figure 32.

With the use of JumboFrames, the theoretical limit of throughput could be reached without any problem at 19.2 Gbps, while the receiver software generates a CPU load of 1.6 among the 12 available cores. The use of regular maximum size Ethernet packets (1024 bytes) yields a similar CPU load, but 60% less performant throughput (8 Gbps), albeit largely sufficient for the needs of the present read-out scheme of the NECTArCam. No data losses have been observed in sustained running. Within the CTA ACTL activities the purchase of a complete system on an IRD project with six switches and 300 physical Ethernet nodes has been requested, which constitutes a full camera simulator and DAQ stimulator system. In order to optimise cost, power consumption and space occupancy, the front-end nodes should be done as multi-Ethernet SBC (single-board computer) cards (less than 50 €/port). Two sample cards have been received at CPPM beginning of 2012.

Although enough headroom exists for the implementation of the read-out according to the present specifications on data rates derived from simulation studies, improvements in several directions are being explored. By exploiting possible higher data transfer rates between front-end and camera server, an on-line calibration and improved fit of "raw" data (full-sample) could be performed within the camera server with better quality than in the front-end electronics itself. Assuming higher data rates due to lower thresholds, the possibility to obtain better performances for low signals with a software trigger generated inside the camera server is being explored.

The observation of an important loss of performance (60%) with regular size or smaller IP packets has triggered a continuing study of the mechanisms of network interfaces and drivers in the Linux kernel. Recent projects exist which are still using standard calls for hardware access to the network interface controller (NIC) but avoid the implicit memory copies (and dynamic allocations!) of the standard drivers for each incoming

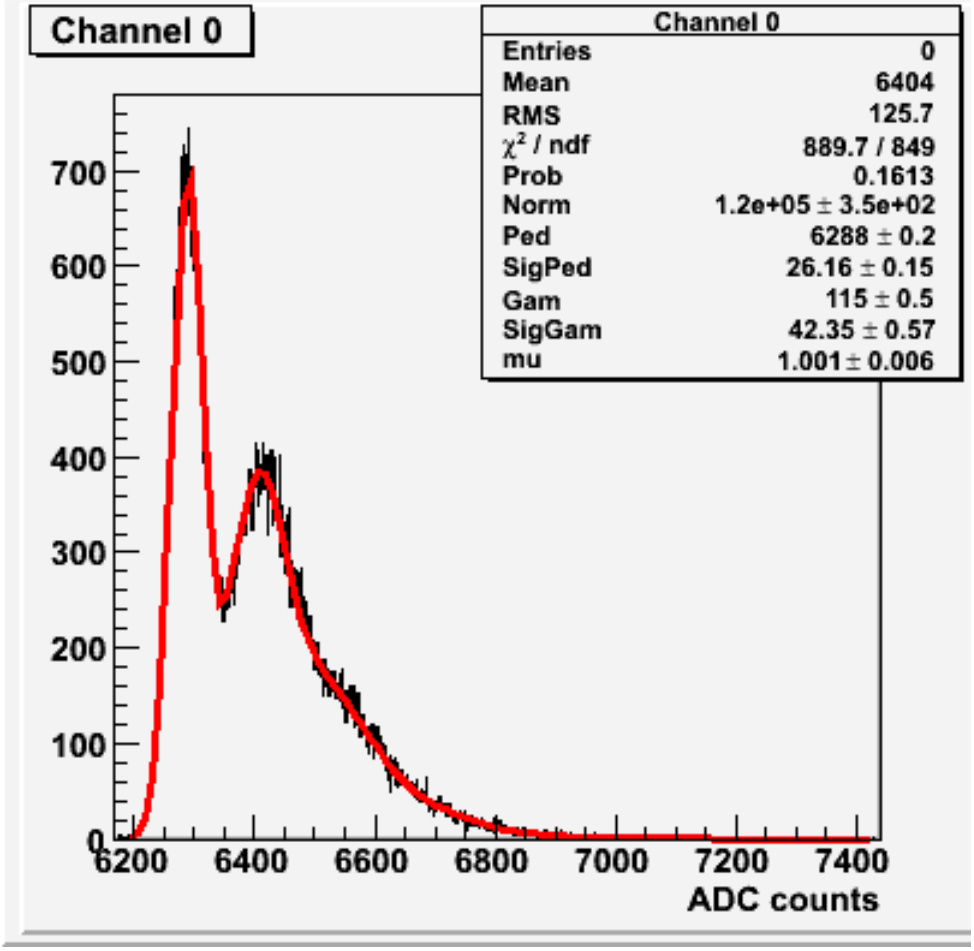

Figure 29: Single photo-electron spectrum obtained with the NECTAr module prototype. One channel of the NECTAr module prototype was equipped with PACTA and ACTA preamplifiers. The photomultiplier gain was set to the nominal value of 5 10^4

packet. This technology looks very promising (and low cost) to circumvent the shortcomings of traditional network driver software with respect to modern high-speed networks.

2.2.8 Calibration

The conceptual design described in section 1.8 is still ongoing and expected to reach its final version around the end of June 2012. The first prototype will be built and initial tests should take place until late 2012, aiming for building a more complete prototype towards the end of 2012. Presently there are two active test-bench (SLAC/CPPM-LUPM) for prototype testing. Although not identical, their characteristics are the followings:

- Dark box
- Laser diode UV
- VERITAS flasher cycle the number of LEDs from 1 to 7, external (TTL) or internal trigger(10Hz), UV LEDs
- ANTARES flashers 1 LED each, external trigger only, blue LEDs, intensity controlled by external power supply
- H.E.S.S.-II flasher system
- H.E.S.S.-II Optical Calibration bench
- MaPMT 64 channels
- Target1 camera module 4chips, 1 FPGA, total 64 channels
- Read-out board to read data from module with in/out optical fibre connections

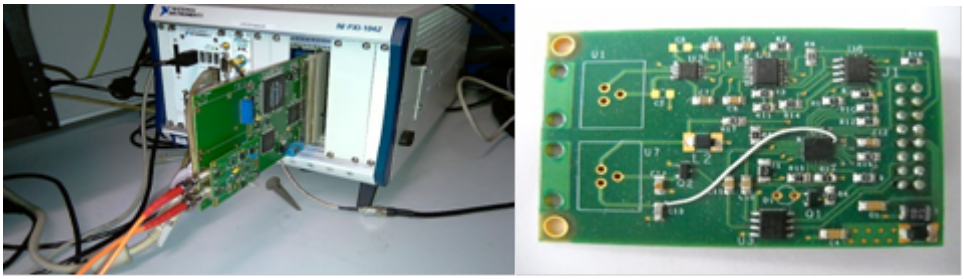

Figure 30: Left: The PXI crate with a MUTIN card on an extender board. Right: the layout of one of the optical daughter boards.

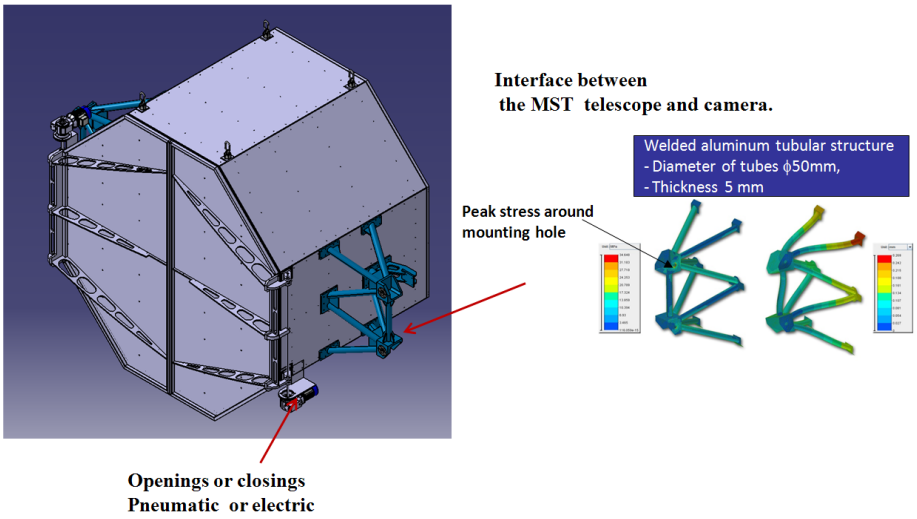

Figure 31: Interface of the camera mechanical structure with the quadrupod of the MST telescope prototype.

2.2.8.1 Perspectives

A working prototype could be envisaged for the end of 2012. Since the proposed solution could also fit the requirements for other type of cameras (with light modifications), a production scenario is not possible as of today. A price estimation of the final production model is situated actually under the 2.5 k€ /source, based on a scale-down model of the H.E.S.S.-II Calibration source.

2.2.9 Photo-detectors and front-end electronics possible upgrades

As stated in section 1.5.2, he baseline phototubes for the NECTArCam are the CTA candidate PMTs. However, it is logical to anticipate the fact that PMTs could be replaced by other photodetectors in the future. Plans in this direction are described in appendix 5.1.

3 Performance

3.1 Verification of concept through simulations

3.1.1 Situation

The camera should be verified by simulations in order to evaluate their performance before building any prototype of a full camera. However, even if the performance of individual cameras have to be determined precisely, the strength of the CTA concept is the large number of telescopes that allows multiple views of atmospheric showers, giving all together the scientific performance of the CTA arrays. So, the individual camera performance can only be evaluated through a simulation of a full CTA array. One should emphasise also that the

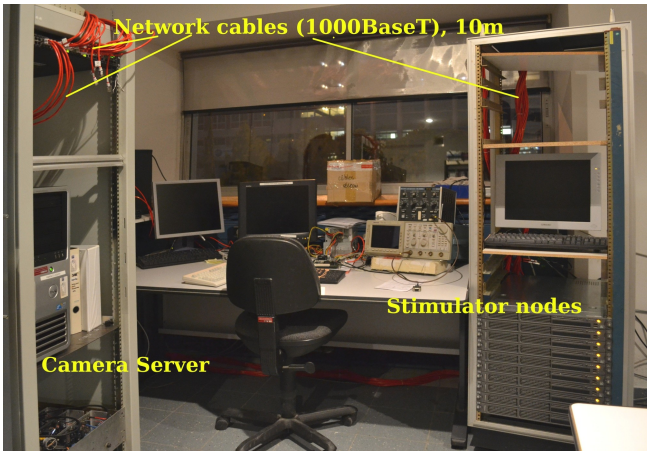

Figure 32: Test setup of the data acquisition system.

MST cameras contribute mainly to the performance of the energy core range of CTA, which will address most of the consortium scientific targets and provide the guaranteed high-energy astrophysics results.

The performance criteria have been defined at a higher level by the Monte-Carlo Working Package (MC WP) such that any concept can be compared in an objective way. These criteria are based on the sensitivity, the energy resolution and angular resolution of the array. We have then followed these recommendations in our past and future work.

The verification of the current camera concept is done with simulations performed by the MC WP few years ago (the production Prod1), which are available for the whole consortium. While the simulated parameters of the hardware components differ slightly from the current ones, the principal characteristics are very similar: the instrument optical efficiency, the electronics scheme (based on a high bandwidth instrumentation and a digitisation at 1GHz), the noise, as well as the optical properties of the MST telescope. As the update of the parameters will likely lead to even better performance, these results can be considered conservative and give a robust baseline.

The simulations have been analysed with different types of reconstruction algorithms and gamma/hadron separations. Here, the results of the algorithms developed by Paris groups (the so-called Paris-MVA analysis) for the shower reconstruction, energy determination and γ/hadron separation are presented. About two billion gamma events have been simulated, about two billion electrons and about 50 billion protons. The resulting sensitivity relative to the Crab flux is presented in Fig 33 for the sub-array E and for only the MST part of the sub-array E. For comparison, the results from the standard analysis made by K. Bernlöhr, so-called MPIK-HD, are also given.

The sensitivity of the CTA array is evidently dominated by the one of the MST in the core range, and the milli-Crab sensitivity is reached by the MST array. The CTA goals in term of sensitivity but also in term of angular resolution and energy resolution (not shown here) are reached with an electronics based on high bandwidth, fast digitisation and with a camera optical throughput of about 12%, as is the case for the NectarCam project.

3.1.2 Plans

The next steps of verification will take into account the latest hardware developments. The telescope simulations will include the optical layout of the DESY MST prototype. The camera simulations will contain the properties of the CTA best candidate of PMT (Photo-detection efficiency, pulse shape) and will compare different modes of read-out, in particular the colibri scheme, which allows to better recover the Cherenkov light from showers with a large time gradient while at the same time reducing the amount of data read out (by reading only pixels around the triggered modules). Large time gradients are expected for a non negligible fraction of high energy gamma rays (see figure 34). The tests and comparisons of the different trigger schemes (analogue and FPGA-based triggers) will be made elsewhere within the MC WP, as the impact of the digitisation rates relative to the performance variations with the NSB rate (currently there is no shared data concerning this topics within the consortium). These new parameters and improvements are expected to improve the collection area above 1 TeV, as well the energy and angular resolutions. Their impact on the energy thresholds will be also studied.

The other aspect to simulate is the impact of the NSB on the performances once the read-out and trigger

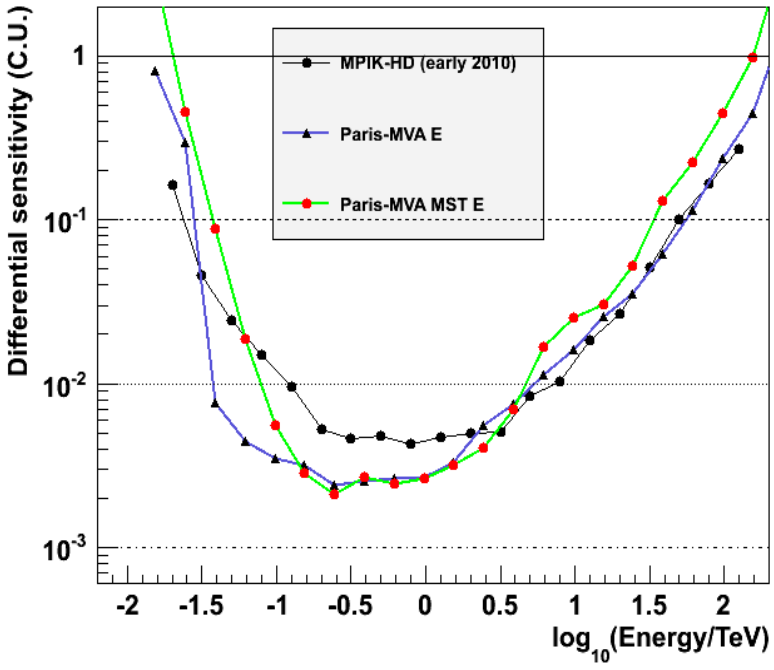

Figure 33: Differential sensitivity in 50h at 5σ for the sub-arrays E and and E with only the MST

schemes are studied. It should be emphasised that this impact should be evaluated with the same analysis parameters (e.g. with the same level of image cleaning). Indeed, while during the observations of the central parts of the galaxy, the NSB levels will change smoothly but significantly, the analysis parameters will not be changed accordingly in order to keep the same Instrument Response Files of the MST array. This work is already well under way: The Colibri scheme has already been implemented in the electronics simulations, as have most of the hardware parameters. The production tools are currently under tests on the EGI Grid via the VO cta.in2p3.fr. This production will be used also as a test bench for the CTA use of EGI grid for massive productions and for analysis computing. A new set of preliminary results is expected for this summer.

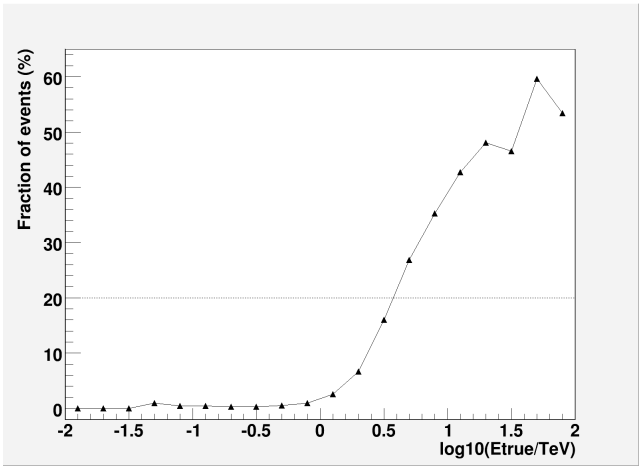

Figure 34: Fraction of gamma rays with a time gradient larger than 10 ns per degree as function of energy.

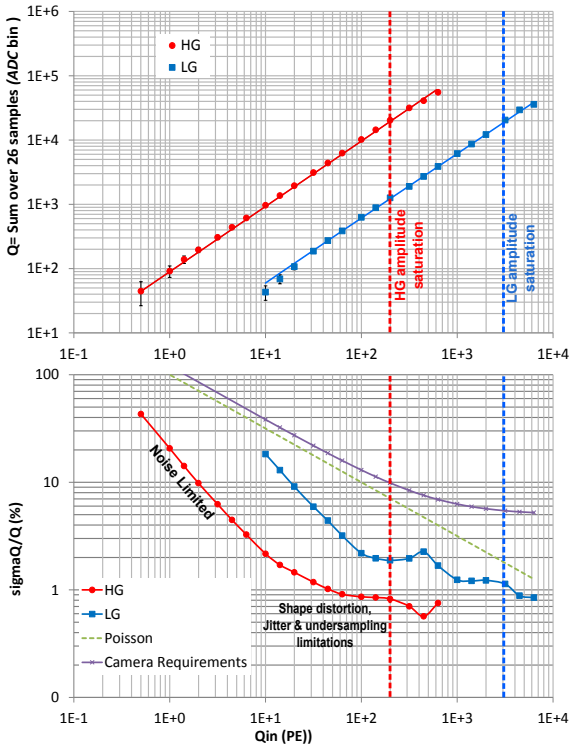

Figure 35: Linearity and charge resolution obtained with the NECTAr chip and commercial amplifiers

3.2 Comparison of expected properties with key requirements

3.2.1 Dynamic range and charge resolution

The dynamic range of the NECTAr FEB was extensively tested with the NECTAr test board. In this test board, the signal from PMTs was amplified by H.E.S.S-like preamplifiers, then sent to the NECTAr0 chip. It was then digitized, the time samples were summed on the on-board FPGA. The results are shown in figure 35. The top panel shows the reconstructed charge as function of the input charge. The charge measurement using the 2 gain channels is linear over 4 decades, as required. As shown on the bottom panel of figure 35, the resolution on the measured charge is better than the requirements over the whole charge range.

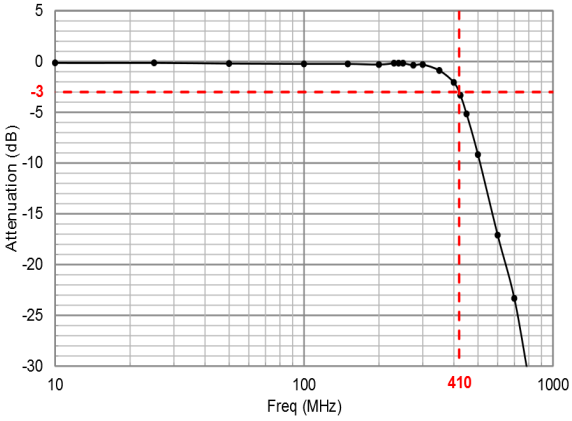

Figure 36: Bandwidth of the NECTAr0 chip

3.2.2 Bandwidth before digitization, timing properties

The Bode diagram of the NECTAr0 chip is shown in figure 36. The bandwith of the NECTAr0 chip is $\sim$ 400 MHz. The bandwidth of the camera system before digitization includes contributions from the PMTs, PACTA and ACTA amplifiers and the NECTAr chip. Since all these elements have a bandwith $\geq$ 400 MHz (see tables 1 and 4), the expected overall analogue bandwidth is $\geq$ 300 MHz, in agreement with the requirements listed in section 1.1.1.

3.2.3 Maximum trigger rate, dead time

The aualct deadtime of the NECTAr prototype module will be measured soon with Poisson distributed random pulses. Some tests already performed are giving information on it. Periodic bursts of two consecutive triggered pulses (50 PE charge) separated by a time of only 2.5 μs were delivered by a generator first at low frequency to the NECTAr prototype module with FPGA operating in "charge mode" with 16 samples. The 2 pulses were acquired without any loss of data and their charge resolution is equivalent to the one of a single pulse proving thus than the readout deadtime of the NECTAr chip is less than 2.5 μs. Then, the burst period was progressively decreased down to 20 μs, corresponding to a trigger rate of 100 kHz (limited by test acquisition software). In these conditions, no data loss (100% efficiency) was noticed nor any charge resolution degradation. This proves that, as expected, the FPGA read by the UDP link can sustain a rate of trigger and data of 100 kHz. Assuming that the deadtime is only due to the NECTAr chip, we can estimate a deadtime of 2.5% for a 10 kHz trigger rate which satisfies the requirement.

3.2.4 Power dissipation

The power consumption and temperature have been measured for the module prototype. Since this module is fed by a single 12 V power supply, the power consumption is simply obtained by measuring the current in the supply. The measured values have been used as starting point for estimations of the whole camera power consumption listed in table 11. This table, corresponding to an embedded camera server scenario (worst case for power consumption) gives a heat dissipation of 3.2W/pixel, less than the required 5W/pixel and close to the recommended 3 W/pixel.

3.2.5 Performances of the AT trigger system

Although the approval of CTA specifications is still ongoing, preliminary specifications on the trigger system exist. A set of functional and performance requirements have been defined in [1, 2, 3].

The functional requirements include the need to provide camera trigger information to the array trigger even when the readout is busy, the monitoring of pixels contributing to the trigger and their sensitivity and finally the possibility to initiate the acquisition of the photosensor from its own trigger as well as from an external trigger. The AT system described in section 1.3.1 was designed based on the experience with present Cherenkov telescopes and fulfills all the functional requirements.

The main performance requirement ask that a gamma ray image illuminating a compact region located in any region over 90% of the area of the camera, which triggers at least with 50% probability, should have a total minimum intensity no larger than 100 photoelectrons. From Figure 6 of reference [1] and assuming a 12% photon throughput, 100 photoelectrons correspond to a $\sim$ 70 GeV gamma ray. Preliminary Monte Carlo simulations indicate that the AT scheme do fulfill this requirement. Although more detailed simulations with the actual characteristics of the hardware should still be done, no critical point has been identified that could prevent the system to fail this requirement, which is standard for H.E.S.S type telescopes. Additionally, the requirements on the minimal rates to support (10 KHz) as well as the dead time and latency ($<$ 300 ns) are also fulfilled.

3.3 Cost, weight and power overview

Cost, weight and power overview are respectively shown on tables 9, 10, 11. The camera is assumed to have a field of view of 8 degrees and 1897 pixels. The camera server is assumed to be hosted by the camera. However, while the event buffer has to be in the camera, the server itself could be on the ground. This would reduce accordingly the cost and power dissipation of the camera. The production cost per channel is less than 600 €, with contributions of 110.7 €from front-end electronics, 244 €from photo-detectors and focal plane instrumentation, 175 €from mechanics and 48 €from slow control, DAQ and power supplies.

Item		Unity cost	Qty / camera	Total / camera
Photodetectors & optics	**462,949.50 €**	244.04 €		
Entrance window	FPI estimate	20,000.00 €	1	20,000.00 €
Light guides	FPI estimate	14 €	1897	26558.00 €
PM Tube	FPI estimate	170.00 €	1897	322490.00 €
Preamplifier + HV	estimate + offer	45.00 €	1897	85,365.00 €
Mechanics	**331,975.00 €**	175.00 €		
Module mechanics	estimate	385.00 €	271	104,335.00 €
Camera mechanics	estimate	120.00 €	1897	227,640.00 €
Front end electronics	**210,025.00 €**	110.71 €		
read-out board	estimate	550.00 €	271	149,050.00 €
Trigger	based on AT estimate	100.00 €	271	27,100.00 €
Backplane	estimate	125.00 €	271	33,875.00 €
Camera processing & monitoring	**91,500.00 €**	48.23 €		
cPCI crate	estimate	10,000.00 €	1	10,000.00 €
CPU	estimate	3,500.00 €	3	10,500.00 €
Safety cards	estimate	20,000.00 €	1	20,000.00 €
DAQ (switch + server + cables +...)	estimate	20,000.00 €	1	20,000.00 €
Power supply	offer	2,200.00 €	5	11,000.00 €
Auxiliary systems	estimate	10,000.00 €	1	10,000.00 €
cables	estimate	10,000.00 €	1	10,000.00 €
			Total 1 camera	1087913 €
			cost / pixel =>	573.49 €

Table 9: Production cost estimates for large production. The camera has a 8 degree field-of-view and 1897 pixels.

4 Plans and future

4.1 Suitability for mass production

Suitability for mass production, together with guaranteeing the reliability of the system, were the main motivations that led to the NECTArCam project. From the experience gained from developing, building and operating the H.E.S.S. cameras, it was known what was needed to build a successful camera. Yet, the H.E.S.S. cameras had been primarily built in the laboratories, and it was clear that some adaptation of the concept was needed to enable also the mass production of Cherenkov telescope cameras by industrial subcontractors.

The approach taken in the design of NECTArCam for improving the reliability of the full system and for enabling mass production is

- to reduce as much as possible the number of elements, and
- to have interfaces as simple as possible between all subsystems.

Furthermore, some components are developed in close cooperation with industry (such as, e.g. the HV boards), so that suitability for mass production is incorporated in their design already from the beginning.

The full camera is assembled from well-defined subsystems (modular concept), allowing separate subsystem validation in laboratory or simulated field environments. This approach is applied for mechanics (module structure, camera body) as well as electronics (reduction of PCBs, use of integrated electronics - such as the NECTAr ASIC that include the ADCs). This approach is illustrated in Fig. 37. The H.E.S.S. II module (left), which is composed of 32 PCBs for HV generation and 3 PCBs for read-out and control, is compared with the NECTArCam module (right), composed of 2 PCBs, one for HV generation and one for read-out. Although each NECTArCam module covers only 7 pixels compared to the 16 pixels handled by the H.E.S.S. module, the

Item		Unity weigth	Qty / camera	Total / camera
Camera mechanics				
	Skeleton	420	1	420
	Skin	60	1	60
	Sandwich	250	1	250
	Funnel plate	140	1	140
	Automatism	100	1	100
	Entrance Window	80	1	80
	Lids	70	1	70
	Interface Camera/Telescope	100	1	100
	Others	50	1	50
Module : prototype		1.64	271	444.44
cPCI crate		30	1	30
CPU		1.3	3	3.9
Safety cards		10	1	10
DAQ switch		70	1	70
Power supply		10	5	50
Auxiliary systems		20	1	20
cables		30	1	30
Others		30	1	30
		kg/pixel	Qty / camera : 1897	kg/camera
	Total	1.03	<=	1958.34

Table 10: Weight estimates for the NECTArCam camera. Modules have the following components: PMTs + HV+ Front-end board + Trigger + module mechanics + Backplane + L1 distrib.The camera has a 8 degree field-of-view and 1897 pixels.

substantial simplification gained by NECTArCam, allowing easier production, handling, and replacement, is obvious.

The validation of each subsystem needs the development of a dedicated test bench, accompanied by the specification of test procedures that describe the parameters that need to be validated and the methods that should be employed to perform this validation.

The approach taken for NECTArCam is to develop the test bench and the associated software for each subsystem using the same environment that is currently envisioned by the CTA consortium for array control within the ACTL work package. This development will accompany the prototyping of each subsystem, and will provide at the end a product with its associated software (and user manual) that allows easy subsystem integration at the camera level. The same software will be subsequently used by the subcontractor for the CTA production phase, and later by the operators for testing and diagnostics during CTA operations. This enables a coherent testing and validation strategy and procedure during all phases of the project.

This philosophy has proven very successful in the context of the camera development for H.E.S.S. II. Tests benches for the 6000 SAM ASICs, for the 2500 PMTs and the 450 electronics boards have been developed using the software environment of the H.E.S.S. experiment. Thanks to these test benches, the failure rates of the electronics boards dropped to zero, all PMTs have been validated, and the ASICs have been efficiently selected, producing considerable savings in time (and consequently money) during production phase.

For NECTArCam, the test benches developed for H.E.S.S. were adapted to the industrial environment and the possible tighter production time schedule. For illustration purposes, figure 38 shows the fully automated test bench used for the H.E.S.S. II cards production.

To assure the reliability of the produced cameras and its parts, Highly Accelerated Stress Screening (HASS) will be employed during the production of the cameras. Depending on the product, these tests will be either done on 100% or on a partial sample of the components. This approach will allow to stay on schedule, while

Item		Unity power	Qty / camera	Total / camera
Automatism		50.00	1	50
Module	Estimate (with 85% DC/DC eff.)	16.3	271	4417.3
Front-end board	Using ACTAlow power amp.	9.65		
Analog trigger	Estimate AT scheme	5.25		
HV + PMTs	Reduced power on the new prototype	1.40		
cPCI crate	estimate CPU, + SLC + Safety	300.00	1	300
DAQ (all)	max	1,200.00	1	1200
Others		75.00	1	75
		W/channel		W/ camera
	Total	3.19	< =	6042.3

Table 11: Power estimates for the NECTArCam camera. The camera has a 8 degree field-of-view and 1897 pixels. Note that the power estimate takes into account the contribution from the camera server.

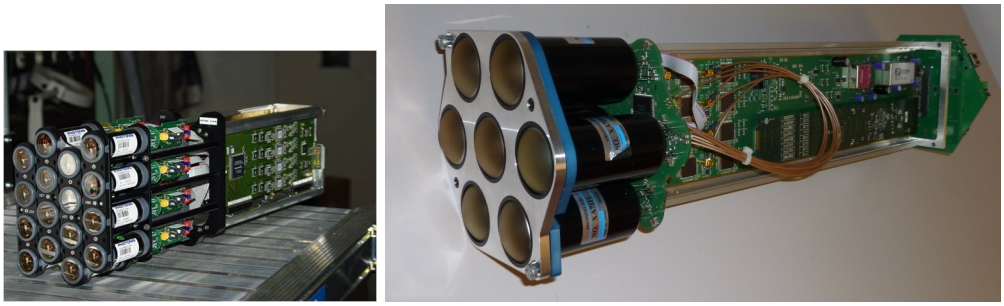

Figure 37: Comparison of the H.E.S.S. II camera module (left) to the NECTArCam module (right)

reducing at the same time the product failure rate after only a few months of operations. A typical test cycle consists of:

- passive temperature cycling on 100% of the electronics boards (24h cycle with temperature varying between 0° and 70°)
- Takaya test (control of all the nets and passive component values on each board)
- Basic functional test

with the the product being rejected if either the Tayaka or the functional test fails. This type of procedure has proven very successful for the development of the H.E.S.S.-II camera, which led to a reliability of 100% of the delivered boards, with respect to 96-97% for H.E.S.S. I (where no such procedure had been implemented). In addition, the complete duration of the production (including product validation) had been divided by a factor of 2 compared to H.E.S.S I due to the earlier identification of problems. After five years since production, 100% of the H.E.S.S. II boards are still operational. We note that the same principle has been applied for the mechanical parts of the H.E.S.S. II camera, such as the module structure, the sandwich supporting the modules, or the Winston cone plate.

In order to optimise the production and to simplify the assembly, the NECTArCam mechanical parts have been designed as simple as possible. Thus, the mechanics of the NectarCam module, based on return of experience from H.E.S.S.-II, is composed of 5 parts (for 7 pixels) whereas the H.E.S.S.-II one is composed of 27 parts (for 16 pixels). This new design reduces the numbers of parts by 58% (percentage calculated for an equivalent number of pixels). It will facilitate the production management and reduce the module cost. Moreover the number of assembly steps is significantly reduced.

For mechanical parts, all metrology control can be done by the subcontractors with a sampling or a full control depending on the criticality of the dimensions, as has been done for the H.E.S.S.-II mechanical parts. Almost H.E.S.S.-II mechanical parts (170 modules, sandwich supporting the modules, camera skeleton, light guides plate (support)) have been produced, controlled and partially assembled by the subcontractors. For

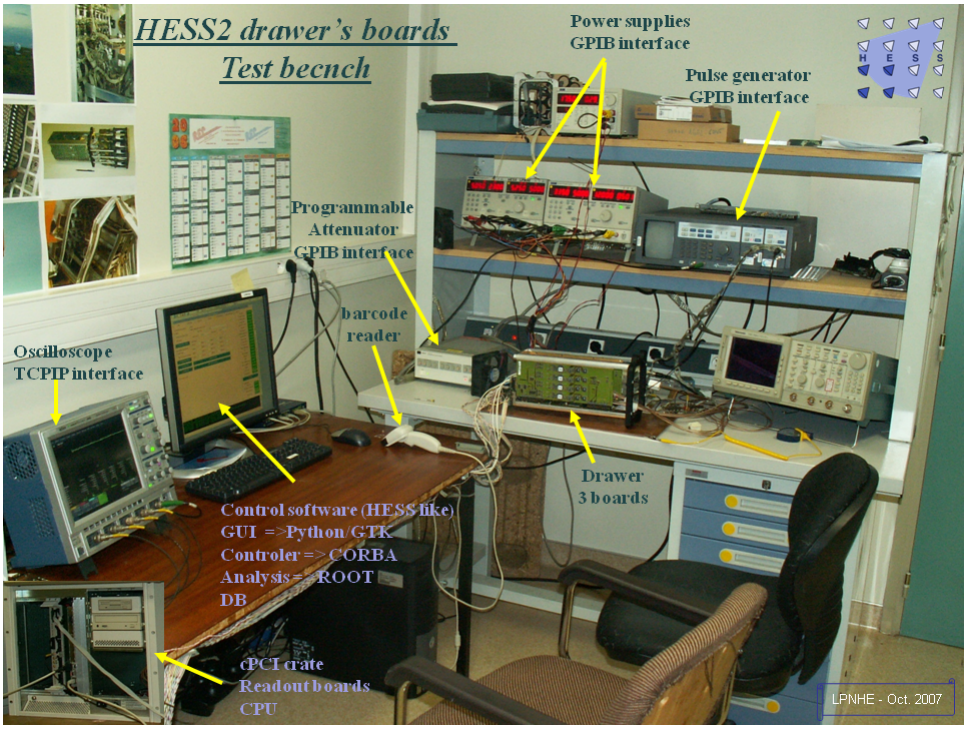

Figure 38: Automated test bench for the H.E.S.S-2 experiment

example, for the H.E.S.S.-II 170 modules production, all the parts have been controlled and partially assembled by the subcontractor's facilities. The production and assembly has been validated by producing and testing a prototype and then a series of 19 modules.

4.2 Further plans, prototyping, time line

4.2.1 Component testing

The first NECTArCam camera module prototype is available since January 2012. The module has been successfully tested and the comparison to the relevant requirements defined for CTA, given in section 3.2 seems promising. The goal of producing an operational module for CTA that derives from the H.E.S.S. camera module, which is considerably simplified (3 PCBs for 7 pixels instead of 35 PCBs for 16 pixels on H.E.S.S), allowing for industrial mass production, testing and integration together with cost optimisation has been achieved.

Highly Accelerated Life Tests (HALT) are planned for all relevant NECTArCam components (e.g. PMTs, HV power supply, read-out board, backplane board), as well as on the NECTArCam prototype module to fully qualify the module in the relevant environment. For this purpose, climatic chambers available in the participating laboratories will be used to subject the module to extreme temperatures and humidity conditions. This will help identify weak components, unstable connections, or any other problem with the module, allowing adapting the design if necessary. The tests will furthermore determine the operating limit of the system that are to be compared to the nominal CTA environment conditions. Based on these tests, the tests specifications and procedures for the camera production phase can be defined.

4.2.2 Partial camera

The next step will be to produce a camera demonstrator composed of 19 to 37 modules to validate the trigger scheme, the DAQ scheme, the mechanical structure and interfaces with other systems (such as the power supplies, central/array trigger and cooling system)[3]. As the system is modular, this approach will permit the full validation of the NECTArCam camera concept, without any need for building a fully-fledged prototype. In this respect it has to be re-emphasised that the NECTArCam camera is derived from an existing system: the cameras of H.E.S.S., which have demonstrated their viability and reliability since 10 years in the Namibian desert.

[3] This will be done in part in the framework of the GATE project

The camera demonstrator will also serve to establish and validate all relevant testing and integration procedures. In particular, during this phase, it will be established which parts of the camera will be built, tested and integrated by industry, and which part of the work will be contributed by the participating laboratories. It is expected that mainly mechanical pieces, electronics boards and some subsystem assembly will be subcontracted to industry as they have the required knowledge and infrastructure for mass production and assembly. Integration work, such as camera module integration and testing, as well as camera integration, will be done for the first camera by the participating laboratories. For the subsequent cameras, knowledge could be transferred to the CTA observatory team on site and/or to other labs inside the CTA consortium. Cameras should then either be assembled on site or camera assembly could be shared over few laboratories, depending on which way is the most cost-effective.

4.2.2.1 Timeline for building the demonstrator

Several milestones have already been validated:

- Milestone1: 01/2011 7 pixels HV board available
- Milestone2: 03/2011 NECTAr0 test board available
  - validation of NECTAr0 chip with in-ADC, Eth link for readout, java GUI & Power strategy
  - first Single photoelectron spectrum with PACTA + NECTAr0 at a gain of 5.10^4
- Milestone3: 10/2011 : NECTAr module prototype available
- Milestone4 : 01/2012 : Preliminary tests with ACTA+PACTA, analog trigger integration tests
  - Validation of the full read-out chain with the final preamplifiers (CTA PMT + ACTA + PACTA + NECTAr0)
  - Successful integration of the AT mezzanines

The next milestones for building the camera demonstrator are:

- Milestone5: 12/2012 Several modules available, software development, mechanical structure
- Milestone6: 03/ 2013 Assembly of a 19 module demonstrator with associated DAQ, Trigger system, Slow control, Calibration and mechanics.
- Milestone7: 09/2013 Demonstrator test and validation
- Milestone8: 03/2014 Concept fully worked out, ready to start camera production.

4.2.3 Full camera

As mentioned in section 4.2.2, there is no need to build a full-fledged camera prototype since all components of the system and their interplays will be validated using a camera demonstrator.

4.3 Risks

The risk management aims at reducing and even eliminating the risks. It enables problem anticipation and ensures the success of the project. The risks management described below relates to risks affecting the project development. The failure modes that may have impact on the reliability, availability, and maintainability of the final product are treated by the dependability management.

A program for risk management has been defined and implemented in NECTArCam consortium (see NECTArCam risk management document MST-CAM-20120309). The main steps of this program are to

- Identify and prioritise potential sources of risks (scientific and technical risks, risks associated with the sub-contractor, resource and organisation)
- Assess their impacts on cost, schedule, performance (severity and probability of occurrence)
- Determine and evaluate approaches to mitigate moderate and high risks Take action to avoid, reduce and control each risk

- Ensure that risks are factored into decisions

The identification and assessment of the NECTArCam project risks have been carried out by NECTArCam management and technical teams, based on a typical risks list combined to the lessons learned from past experiences (in particular H.E.S.S.-I and H.E.S.S.-II) and from expert knowledge. The main identified risks are listed in appendix 5.5. This list will be updated according to the progression of the project and the actions taken.

4.3.1 Organisation and resource risks

These are important risks, but outside of the scope of the present document and thus will not be addressed here.

4.3.2 Scientific and technical risks

There is no scientific and technical risks classified as high risk. The main medium risks concern interface risks with HV and pre-amplifier board. The design is not yet completely satisfying yet and needs more time to be developed. The other high medium risk is about the technical innovative solution for the light guide (lenses) which can have a big impact on the cost. Presently, there is not enough information about the cost of this kind of light guide. More information should be available in April 2012. In any case, another technical solution (cone) is available in case the price of the lens solution is too high.

4.3.3 Subcontracting risks

There are three high risks on the subcontracting. The first one is about the monopoly of the Hamamatsu company for providing PMT tubes. The main impact is on the PMT cost. The second is due to the global economic context which cannot assure that industries are sustainable. The third concern the time delay to obtain a public procurement. This has an impact on cost which could be as high as 20 000€. The time for public procurement should be taken in account in the production schedule.

5 Appendices

5.1 Photodetectors and front-end electronics possible upgrades

Geiger mode avalanche silicon photodiodes (SiPM) are a very attractive alternative to standard photomultiplier tubes for an upgrade of the MST camera. The main advantages of SiPMs are low voltage operation (40-70V), good single pe resolution, high detection efficiency, insensitivity to magnetic field, light weight and finally ability to support high illumination (daylight). The main drawback is the limited linearity: few 100 p.e. for 1 mm^2 devices. Temperature sensitivity should not be an issue for CTA because of the high level of NSB noise. The cost is presently comparable to a PMT and should decrease taking benefit of high volume production of silicon devices.

5.1.0.1 Status of the work

A characterization work on commercial SiPMs has already started. Spectra showing single p.e. resolution have been measured (fig 39). The dark count noise has also been studied, as well as the temperature behaviour between -10and +40 degrees Celsius. It appears that temperature control is mandatory to keep the gain constant, but no cooling is necessary.

In order to replace a 1 inch diameter PMT by SiPMs, it is planned to use a 16 pixels matrix (fig 40). Each pixel is 3x3 mm^2 and made of 3600 50x50μm micropixels. This arrangement will allow to match the MST required dynamic range. Tests of this issue are in progress. A specific light guide is necessary to compensate for losses due to the dead zones between pixels (the fill factor is 61.5%). A specific pre-amplifier ASIC will be designed to interface the SiPM matrix and the NECTAR front end board, including individual pixel gain adjustment to compensate for gain dispersion in the matrix which can be as high as 30%.

The design of this ASIC will be done in 2012 and a first prototype foundry is planned in early 2013. The cost of this development is estimated to 30 k€, including Multichip project foundry and test boards.

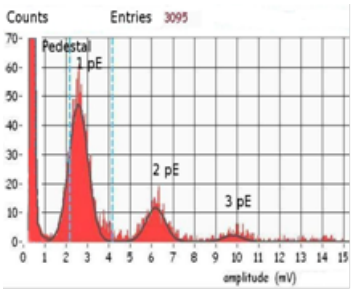

Figure 39: Hamamatsu 1mm^2 MPPC response

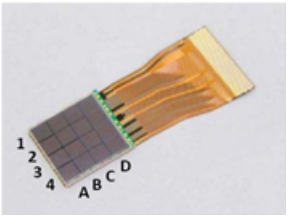

Figure 40: 4x4 Hamamatsu MPPC matrix

5.2 Mechanical design

This annex gives some mechanical features of the NECTArCam camera. Figure 41 gives the overall dimensions of the NECTArCam camera. Figure 42 gives the internal distribution (racks versus module sandwich) and figure 43 shows the layout of the module sandwich.

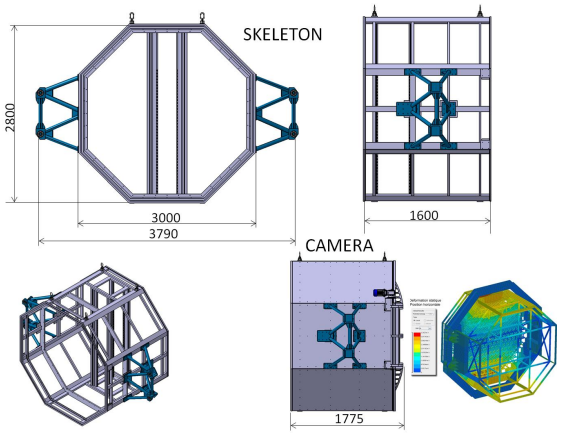

Figure 41: Dimensions of the mechanical skeleton of the NECTArCam camera

5.3 HV stability

This appendix shows the performances of the HV system used for the H.E.S.S PMTs. Fig 44 shows that the HV is very stable in time and Fig. 45 gives the variation of the intensity in the HV supply with time and temperature.

5.4 Organisation and WBS of the NECTArCam

This appendix gives the detailed WBS of the NECTArCam technical workpackages. The WBS of the mechanics and cooling, camera processing and monitoring, front end electronics and focal plane instrument workpackages are shown on figures 46,47,48 and 49.

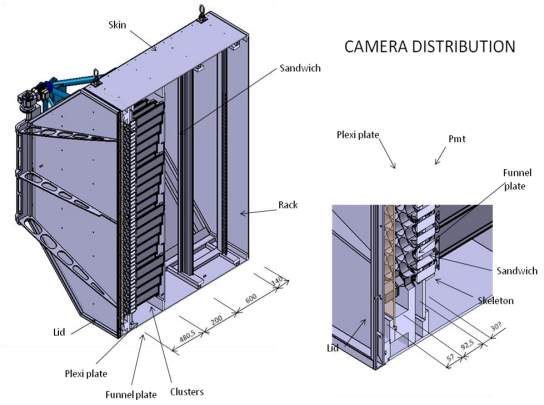

Figure 42: Internal spatial distribution of the NECTArCam camera

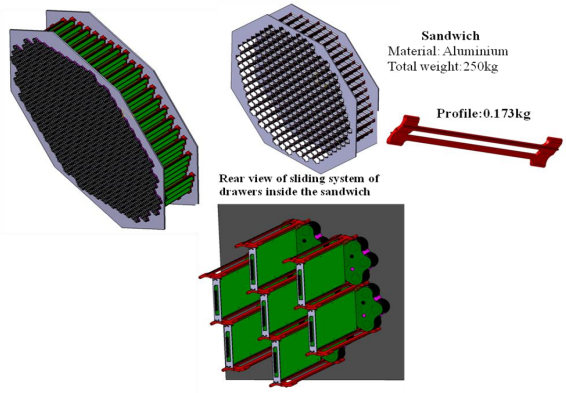

Figure 43: Mechanical properties of the module sandwich

5.5 Risk analysis

A preliminary study of the risks associated to the NECTArCam has been performed. Fig. 50 and 51 shows the main risks that have been identified.

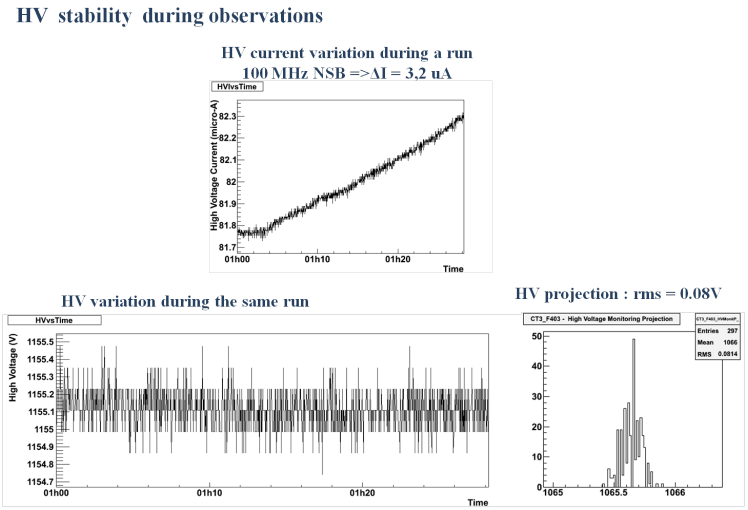

Figure 44: Evolution of HV with time in the H.E.S.S. camera

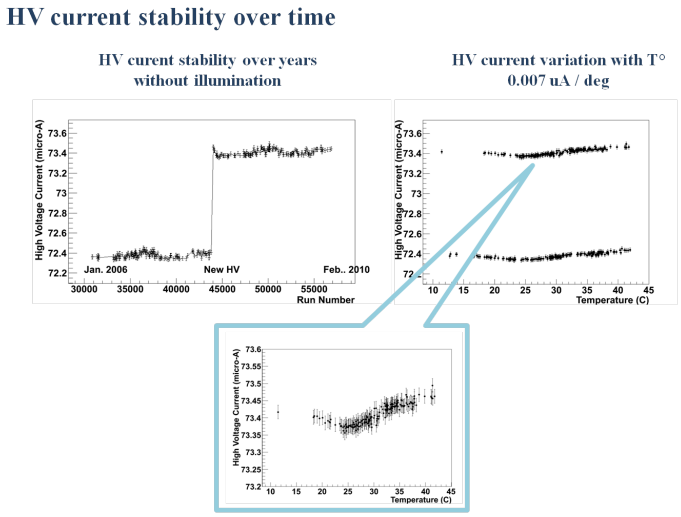

Figure 45: Evolution of current in PMT HV for the H.E.S.S. camera

References

[1] K.Bernloehr et al, "Level A: CTA system performance requirements", MANTPC20120316 (2012)

[2] K.Bernloehr et al,"Level B: CTA sub-systems performance requirements", MANTPC20120321 (2012)

[3] M.Barceló et al.,"Level C requirements for single dish CTA cameras", unpublished

[4] R.Mirzoyan,"CTA candidate PMT",Review of camera activities (2011)

[5] P.Vincent, "ELEC WP activities overview", Review of camera activities (2011)

[6] E. Delagnes et al., "A multigigahertz analog memory with fast read-out for the H.E.S.S.-II Front-End Electronics",Proc. IEEE Nuclear Science Symp. Conf., pp.332 -336 2006

[7] E. Delagnes et al., "NECTAr0, a new high speed digitiser ASIC for the Cherenkov Telescope Array",Proc. IEEE Nuclear Science Symp. Conf., pp.1457-1462 2011

[8] C.L. Naumann et al (NECTAr collaboration), "New electronics for the Cherenkov Telescope Array CTA", Nuclear Instruments and Methods in Physics Research Section A (2011), in press

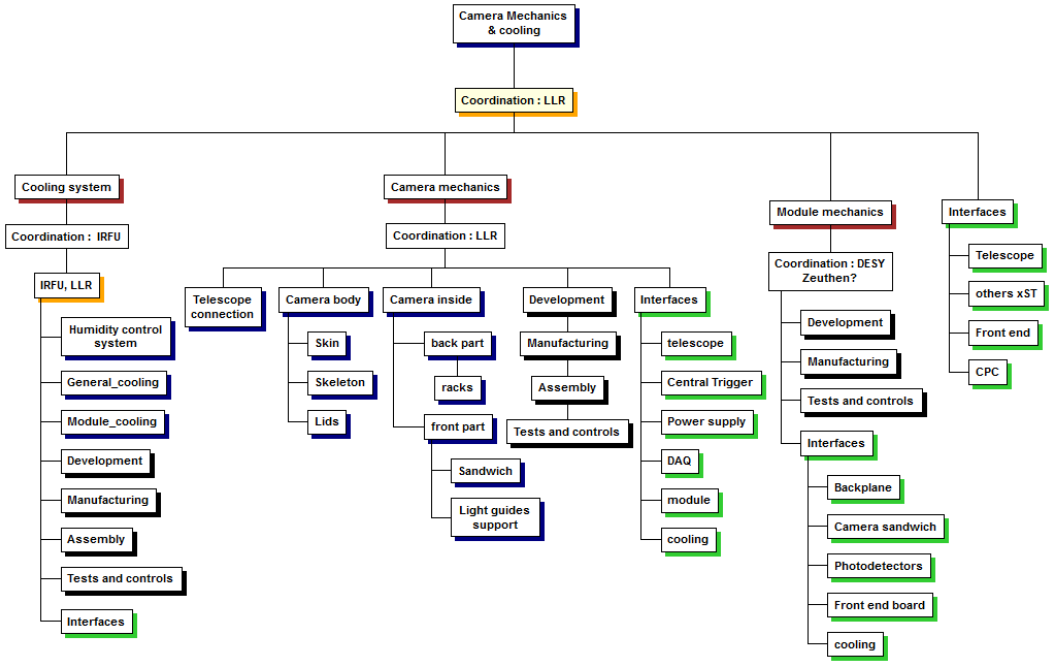

Figure 46: WBS of the mechanics and cooling workpackage

[9] D. Gascón et al., "Wideband (500 MHz) 16 Bit Dynamic Range Current Mode Input Stage for Photodetector read-out", 2011 IEEE Nuclear Science Symposium and Medical Imaging Conference, Valencia, 2011

[10] A. Sanuy et al., "Wideband pulse amplifiers for the NECTAr chip", Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, In Press, Corrected Proof, Available online 17 December 2011. http:dx.doi.org10.1016j.nima.2011.12.025

[11] Rissi, M. Otte, N. Schweizer, T. Shayduk, M., "A new trigger provides a lower energy threshold for the MAGIC Cherenkov telescope", NSS '08. IEEE (2008) 1472.

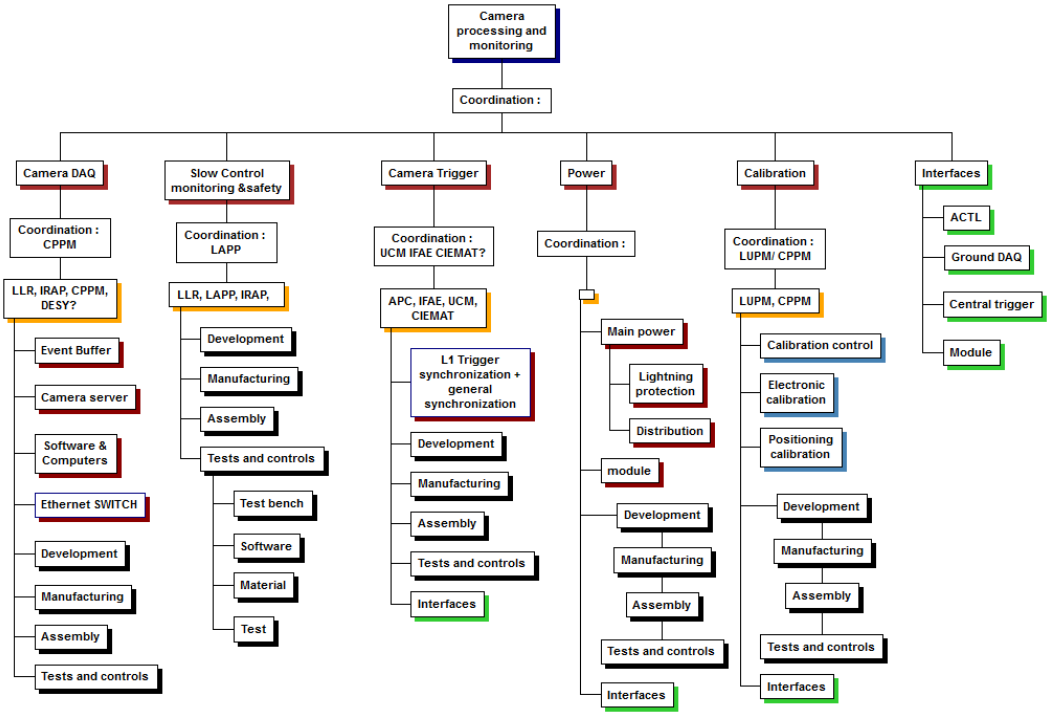

Figure 47: WBS of the camera processing and monitoring workpackage

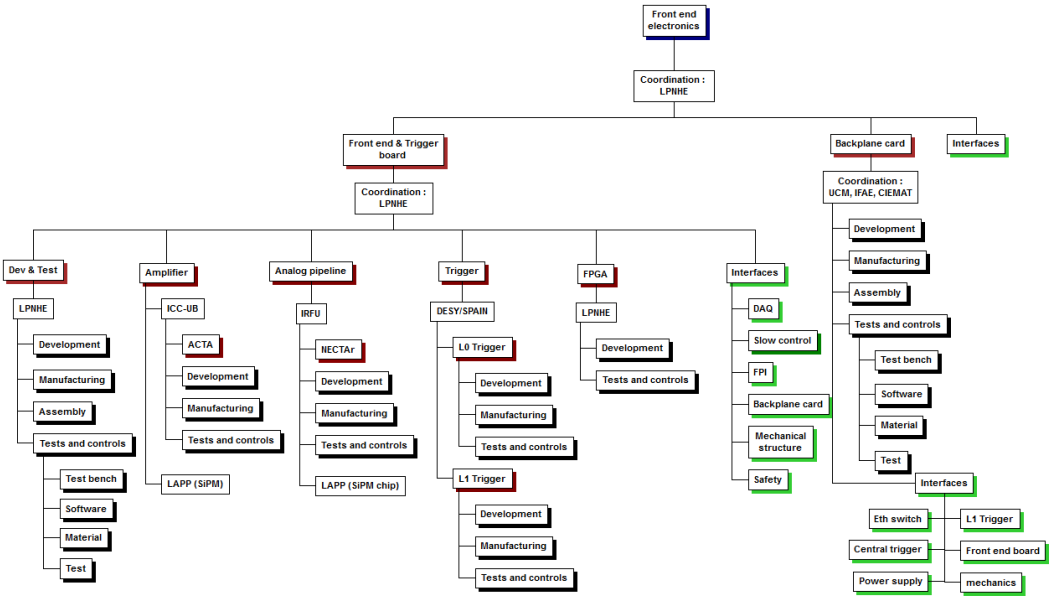

Figure 48: WBS of the front end electronics workpackage

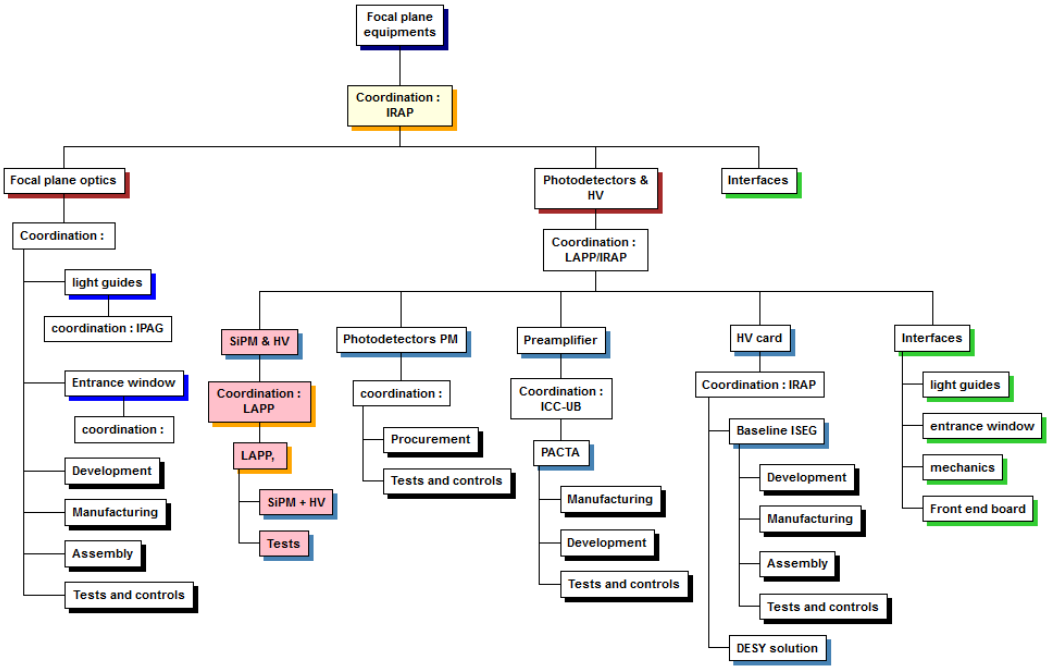

Figure 49: WBS of the focal plane instrument workpackage

Identification						Assessment			
Number	**Risk description**	**Cause and consequence**	**Comments / Possible actions**	**System or subsystem concerned**	**Risk impact type** (technical, cost, schedule, safety)	**Severity** 1 Low 4 Significant 7 Critical 10 Catastrophic	**Probability of occurrence** 1 Negligible 3 Low 6 Significant 8 High 10 Very high	**Risk Index** = Severity x Probability	**Risk magnitude**
Camera									
0070	Sustainability of the industrial (economic, sector of activity,...)	incomplete production, delay, change of industrial	the probability is high because of the economic context (crisis)	Camera	Cost, schedule	7	6	42	Medium risk
0038	Loss of expertise during the development of an element	because of the expert departure	Critical tasks need to have regular meetings, to formalize and share experiences. the risk disappear when the element can be producted (the development is finished)	Camera	schedule, cost, technical	5	6	30	Medium risk
0056	Significant delay in public procurement	delay		Camera	Schedule	6	5	30	medium risk
0006 to 0007	Poor communication inside the project	misunderstantding, lake of information ---> delay, sub systems incompatible	weekly meeting	Camera	schedule, technical	7	3	21	Medium risk
0003 to 0005	Poor definition of the interface and /or tasks : ommission of an interface and /or a task	interface or task not taken in account ---> the camera is not operated ---> unsatisfaction of collaboration, delay	Low probability of occurrence thanks to the work done on the detailled PBS and WBS	Camera	schedule, technical	6	3	18	Medium risk
0028 to 0030	Tardive definition of specifications	Requirements not taken in account in the design, performance not met Requirements taken in account very late requiring changes of the design ---> delay, overcost		Camera	Schedule, cost	5	3	15	Medium risk
0020 to 0022	Poor definition of the need / of the specifications	the camera doesn't meet the scientific requirements, low performances the camera is too efficient, upper	project reviews decrease the probability of occurrence	Camera	cost, technical	4	3	12	Low risk
0023 to 0027	Scientific needs changes	the camera is too efficient, upper performances ---> unnecessary extra cost the camera doesn't meet the scientific requirements, low performances the camera is not adapted to environmental constraints (temperature, humidity ...), risk of failure the design must be modified --> delay, overcost		Camera	schedule, cost, technical	4	3	12	Low risk
Camera DAQ									
0073	Problems with implementation and deployment of our solution on large scale	incompatibility with the chosen equipment, debug/development, unexpected cost	Choice of COTS makes reduces risk to a reasonable minimum	Camera DAQ	cost, technical	7	3	21	medium risk
0074	DAQ requirements exceeding possibilities of our solution	Modification of physics requirements, modification of DAQ s/w, delay and overcost	The existing solution margins can satisfy more needs	Camera DAQ	cost, technical	4	3	12	Low risk
Camera mechanics and cooling system									
0055	risks on the steel raw material	delai of supplying, increased costs		Camera mechanics and cooling system	schedule, cost	4	6	24	Medium risk
Focal plan optics									
0041	one of the two solutions for the light guide (lenses), is a technical innovative solution	the material found for this solution could be expensive. At the moment, there is no no contact with industrial (information expected in april 2012)	The impact on the cost can be very important but the probability of occurrence is low because there is an other technical solution	Focal plan optics	Cost	10	3	30	Medium risk
0042	tests on light guides (60 000 for CTA) have never been industrialized for the passed experiences (HESS)	difficulties to define and implement the tests by the subcontractor's --->impact on the cost and schedule	the tests should be properly defined with the industrial	Focal plan optics	cost, schedule	7	3	21	Medium risk
0043	one solution for the entrance window is a technical innovative solution : attach a little part in front of each light guide (cone)	difficulies to implement the system		Focal plan optics	Technical	4	3	12	Low risk
Front end electronics									
0044	(electronics) components obsolescence.	Availibity time of components is smaller and smaller. Some components used for prototyping can become unvailable for production. Need for redesign or increase of price to pay brokers to find stocks	Use of as standard as possible components	Front end electronics boards	Cost, schedule	4	6	24	Medium risk

Identification						Assessment			
Number	**Risk description**	**Cause and consequence**	**Comments / Possible actions**	**System or subsystem concerned**	**Risk impact type** (technical, cost, schedule, safety)	**Severity** 1 Low 4 Significant 7 Critical 10 Catastrophic	**Probability of occurrence** 1 Negligible 3 Low 6 Significant 8 High 10 Very high	**Risk Index** = Severity x Probability	**Risk magnitude**
0046	Obsolescence of the microelectronics technology used for custom chips.	Low lifetime of modern process and versatility of the microelectronics industry. If fabrication process disapear, a redesign of chips may be necessary	Use of Microelectronics technology from medium size foundries wich are not at the edge of the technology and which are purchasing automotive markets (longer lifetime required). Produce enough spare chips (30% more than required). Time between process stop annoucement and effective stop is usually 1 year.	Front end electronics boards	Cost, schedule	7	3	21	medium risk
0078	Problem during the FE board production (manufacturing error)	Modification or new manufacturing of boards is needed Legal problem if a change of the industry is necessary	A special care must be taken when chosing subcontractiers and writing technical and administrative specifications. Probability of occurrence quite low due to our experience in that fill in previous projects (LHC ...).	Front end electronics boards	Schedule, cost	7	3	21	medium risk
0045	Risks in custom chip productions (bad manufacturing).	Problem of chip manufacturing. Reprocess required or low yield of production	Use of mature Microelectronics technology well known and with good production yield. Pre-serie run of production to validate masks and evaluate the yield. Use of robust chip designs.	Front end electronics boards	Cost, schedule	5	3	15	Medium risk
0077	a performance degradation of the system once integrated	delay		Front end electronics boards	Schedule	4	3	12	Low risk
Photodetectors, preamplifier, HV									
0069	Monopoly or limited competition	Hamamatsu seems to be the only reliable PMT provides ---> overcost		photodetectors, preampl, HV	Cost	10	6	60	High risk
0065	Technical risks on interfaces	The mechanical interface between PMT and ISEG HV card has not yet been defined ---> Solution needs to be adapted or developed ---> overcost The PACTA PA is not yet integrated on ISEG		photodetectors, preampl, HV	cost, technical	7	6	42	Medium risk
0068	Technical solutions becoming obsolete	PMT may be replaced some day by SiPM	SiPM technology probably not mature for CTA first light	photodetectors, preampl, HV	Technical	10	3	30	Medium risk
0061 to 0064	No alternatives if questioning of technical choices, no technological options scenarios studies	Only ISEG HV studied , Only PACTA PA studied---> Alternative solution needs to be adapted or developed ---> delay, overcost	project reviews decrease the probability of occurrence	photodetectors, preampl, HV	Schedule, cost	7	3	21	Medium risk
0057 to 0058	Poor flow of information, withholding of information	No detailed technical drawings of ISEG HV system ---> Any modification or bug correction needs to go through industry ---> overcost, delay	Low probability of occurrence due to well specified interfaces and HESS heritage	photodetectors, preampl, HV	Cost, schedule	4	3	12	Low risk
Slow control and monitoring, safety									
0072	Subcontracting risks Poorly defined selection criteria for industrial. Incomplete contract, technical and administrative specifications		A special care must be taken when chosing subcontractiers and writing technical and administrative specifications. Probability of occurrence quite low due to our experience in that fill in previous projects (LHC ...).	Slow control and monitoring, safety	schedule	7	3	21	medium risk
Clock distribution, timestamping									
0082	Technical specification inaccurate, fluctuation after project started	scienfific needs inaccurate		Timestamping	Technical	4	6	24	medium risk
Trigger									
0039	a performance degradation of the Analog Trigger system once integrated in the readout electronics		It can be avoided by extensively testing the full camera readout system in the laboratory, taking special care in the hardware integration design phase in terms of space, heat dissipation and electromagnetic compatibility	Trigger	Technical	4	3	12	Low risk
0040	the impossibility of calibrating the system during field operations		It can be avoided by foreseeing the hardware elements, procedures and interfaces required for this operation	Trigger	Technical	4	3	12	Low risk