The NECTArCam camera project

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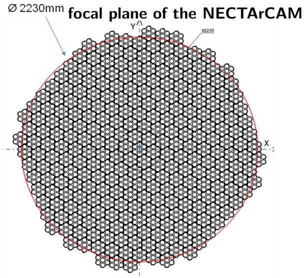
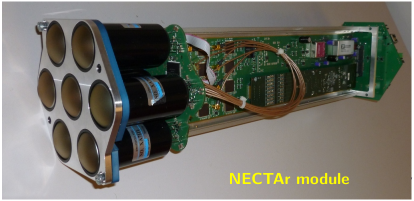
Outline

Key assumptions of NECTArCam design

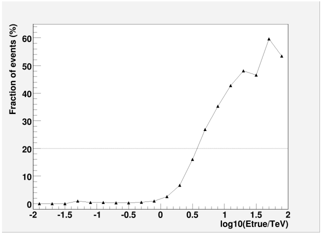
- MST camera
- Modular design
- photodetectors: 1.5 " PMTs
- FOV 8°
- pixel size 0.18° ⇒ 1897 pixels
- Improved version of H.E.S.S, MAGIC cameras
- Expected improvements:
  - Timing capabilities
  - Reliability
  - Cost
  - Weigth



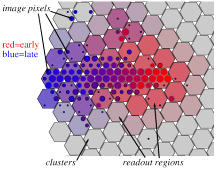


Basic measurements

- Basic measurements are total charge and arrival time Cherenkov signal
- Complete pulse shape analysis also possible
- Background light from photon noise: **100-300 MHz/pixel**
- Time width of Cherenkov signal: 2-3 ns $\Rightarrow$ 10-20 ns read-out window optimal.
- FOV of MST camera 8° $\Rightarrow$ notable fraction of events with time gradients $\Rightarrow$ flexible readout
- Measurement of time gradient $\Rightarrow$ Arrival time accuracy 2 ns/pixel



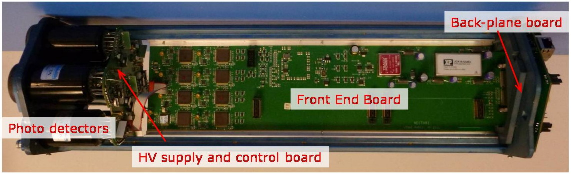
fraction of γ events with time gradient $> 10ns$/degree



Key assumptions for the NECTArCam readout

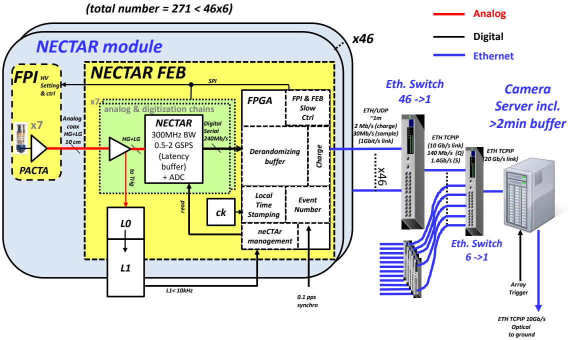
- minimal pulse distortion (charge measurement by pulse interpolation+systematics on timing measurement) with analogue bandwidth $>$ 300 MHz
- sampling rate $>$ 2 x analogue bandwidth (ideally 1-2 GHz)
- acquisition of charge/time of arrival or full signal
- flexible read-out window
- read-out window size 10-20 ns
- full or partial camera read-out
- event read-out triggered in camera
- events buffered waiting for array trigger

The heart of NECTArCam: the NECTAr module



- Camera module with 7 pixels ⇒ 271 modules in camera
- 3 boards: HV management and supply, FEB and back-plane
  → replacement of photodetectors possible
- 2 connectors: from FEB to HV management and supply, from FEB to back-plane
- All the power given by a **single 12 V DC** power supply

Camera architecture

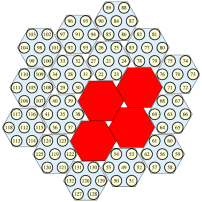


- output from PMT amplified (PACTA+ACTA)
- separated into a trigger path and a data path (HG+LG)
- After trigger, $\sim$ 2.7 kbits of data tranfered to on-module FPGA (16 sample read-out window)
- Charges, arrival times calculated in FPGA
- data transfer FPGA $\rightarrow$ camera server through 46 Ethernet switches
- data rate FPGA $\rightarrow$ switches $=$ 2 Mbit/s (charge+arrival time) $=$ 30 Mbit/s (all the time samples)
- events buffered on camera server

Trigger concept

Look for signal excess in a $\sim$ 4 ns time window in a compact region of focal plane.
Three trigger levels

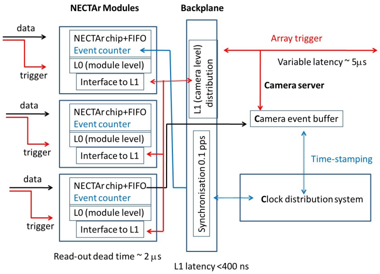
- module level (L0)
- camera level (L1)
- array level



2 possible L0, L1 implementations, Analog or Digital

- L0 information calculated in module
- L0 information is sent to neighboring modules.
- L1 algorithm calculated in module
- L1 information sent to all camera (or ROI)
- if trigger, event transfer from NECTAr chip to camera server
- if array trigger, sent to ground

Architecture of the trigger system of NECTArCam



- rate of physical cosmic ray events $\sim 3kHz$
- background events due to night sky (NSB) eliminated with L0/L1
- dead-time of NECTAr chip RO: 2-3 μs (depending on number of samples)
- camera deadtime expected @ 6 kHz trigger rate: 1-2 % (below 5% requirement)
- 2 min of data stored in camera server >> latency of array trigger ($\sim 5\mu$s).

Analog trigger concept

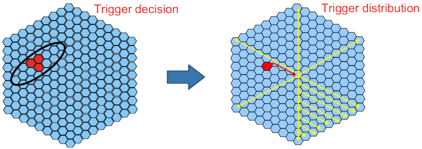
Concept Two possible approaches:

- **Majority trigger:** excess of the number of pixels with a signal above a threshold in the trigger region.
- **Sum trigger:** excess of the analog clipped sum of the signal in the pixels within the trigger region $\rightarrow$ Focus on Sum Trigger

Goals:

- Trigger rate: no limitation due to trigger implementation, should sustain 100 kHz
- Dead time: negligible ($<< 1$ %)
- Trigger latency: less than analog memories depth
- Jitter of trigger signal among modules: < 1 ns, as required from readout
- Optimized power consumption, weight and cost

Analog trigger concept (continued)



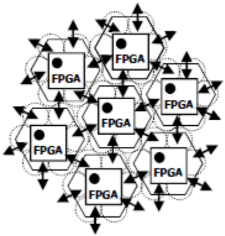
Each hexagon represents a NECTAr module

- First combines the signal within a module to provide a L0 signal
- Then combines the L0 among all trigger regions (closed-packed patches of 2, 3 or 4 modules)
- Camera triggered if the combination exceeds a certain threshold in any trigger region
- The trigger is distributed back among all modules isochronously
- The clock signals can also be distributed with the trigger distribution system (if needed)

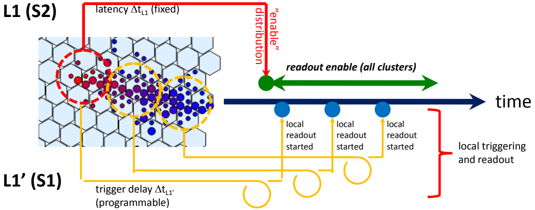
Digital trigger concept

- L0 board: output of PMT pulse discriminator
- L1 board on backplane: input signals from L0 boards in module+ neighboring modules (49 pixels)
- trigger algorithms running on an FPGA in the backplane
- flexibility in algorithms
- L1 decision sent to module FPGA to initiate RO
- L1 decision propagated to neighboring modules

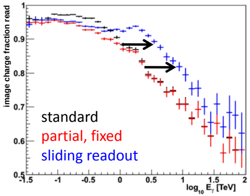
The DT L1 trigger implementation was not compatible with the backplane implementation of the NECTAr module $\rightarrow$ will be tested with next prototype.



Flexible readout: the Colibri scheme



- L1 trigger enable L'1 triggers (lower threshold) in camera for fixed time period
- L'1 triggers tag central and neighboring modules for RO
- L'1 RO only in short 10-20 ns time window
- Advantages: short time window, ROI read-out
- readout follows shower development → improved image coverage
- Possible implementation: 2 trigger levels, delays to accomodate L1 latency
- Fraction of high energy events charge recovered



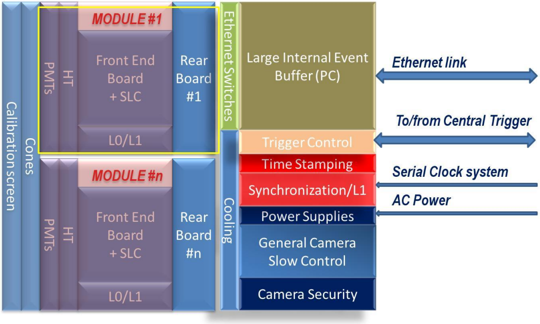
From the NECTAr module to a full camera

The operation of the NECTArCam requires additional tasks:

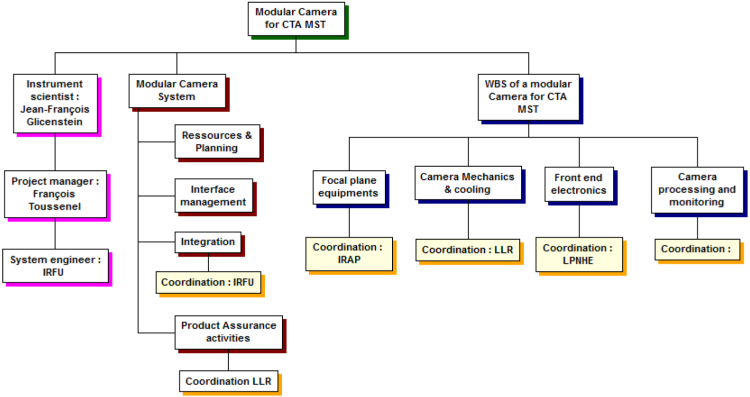
- optimized mechanics and temperature control
- powering
- safety
- monitoring/slow control
- clock distribution
- calibration

Implementation of these tasks based on experience

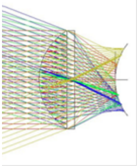
for H.E.S.S/MAGIC.



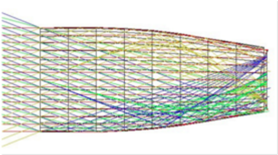
Organization of the NECTArCam project



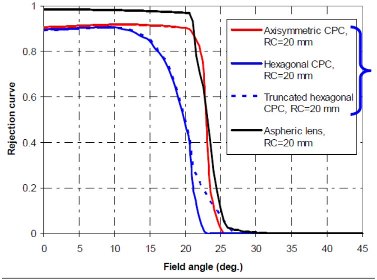
Light collectors



Aspheric lens simulation (Zeemax)



Winston cone simulation (Zeemax)

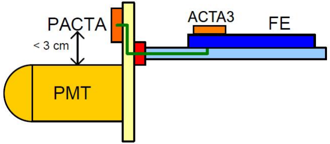


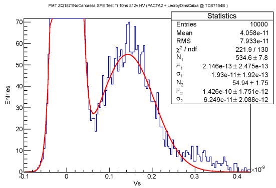
Light collectors could be

- standard Winston cones
- aspheric lenses → could also be used to seal the camera

PACTA preamplifier

- PMT signal amplified to allow operation at lower HV → decreases aging.
- second amplfication stage on FE board (ACTA)





Parameter	Result	Comments
BW	500 MHz	
Noise (ENC). Dif.	5 ke	10 ns int. time
Noise (ENI). Dif.	400 nA rms	
Dynamic Range	16 bits	
Relative linearity error	$\lesssim$ 2 %	(Charge meas.-fit)/fit
Power consumption 3.3 V operation	120-150 mW	2 diff outputs. (HG/LG)
Power consumption 3.3 V operation	80-100 mW	2 S.E. outputs. (HG/LG)

spe spectrum (R11920-100-01 PMT+PACTA) gain ($G = 4\ 10^4$)

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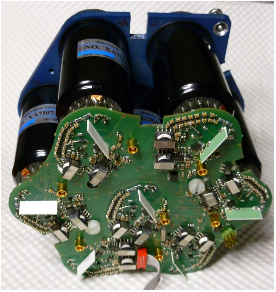
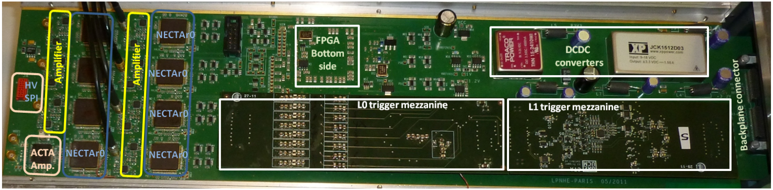
HV control board

- prototype board: industrial design with ISEG
- very good performances in H.E.S.S-I and H.E.S.S-II
- supplies for 7 channels on single board
- integrates control and monitoring of the HV supply for each of the 7 PMTs through a dedicated micro-controller (SPI serial link)
- on-going redesign to lower power consumption



Front End Board

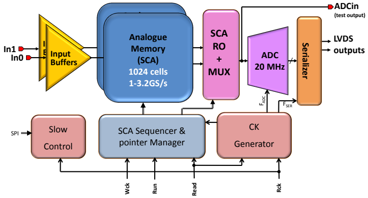


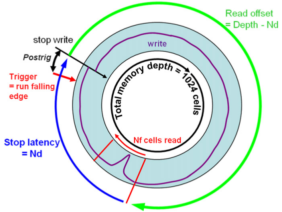
Prototype of the module FEB

Components of the FEB

- ACTA amplifier (also commercial amplifiers on prototype)
- NECTAr0 chips (Switched Capacitor Array+ADC)
- Altera FPGA for control of HV, NECTAr, etc and transmission of data on the Ethernet
- DC/DC converters
- L0 and L1 trigger components (now mezzanines)

NECTAr chip

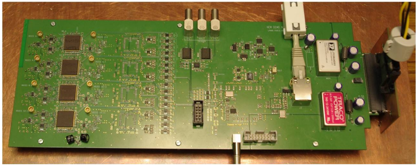




- NECTAr0 chip first prototype of an analogue buffer and digitiser chip **specifically designed for the CTA experiment**
- based on the architecture of the SAM chip (H.E.S.S.-II telescope)
- uses AMS CMOS 0.35 μm technology
- SCA part: 2 channels used as a circular buffer (1024 cells)
- sampling frequency 0.4 to 3.2 GSPS
- Readout time: 2 μs (16 samples)/ 3.2 μs (32 samples)

NECTAr chip: performances

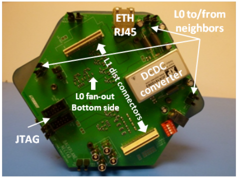
	Feature or Performances	Initial Requirement	Unit
Nb of Channels	2		Differential Channels
Memory Depth	1024		Cells
Input impedance	4		pF
Power Consumption	210	$\leq$ 300	mW
Analog Bandwidth	410	$\geq$ 300	MHz
Sampling Frequency	0.4 to 3.2	0.5 to 2	GSPS
Deadtime/event (16 samples)	2	5	μs
ADC LSB	0.5	0.5	mV
Total Noise	$\leq$ 0.8	$\leq$ 0.8	mV RMS
Maximum signal	2	2	V
Dynamic Range	11.3	$\geq$ 11	Bit RMS
Crosstalk	0.4		%
Relative NonLinearity	$\leq$ 3	$\leq$ 3	%
Sampling Jitter	$\leq$ 40	$\leq$50	ps RMS

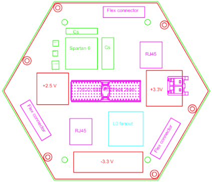


NECTAr chip test board (similar to NECTAr module test board except amplification part)

Backplane Board

Analog Trigger Backplane



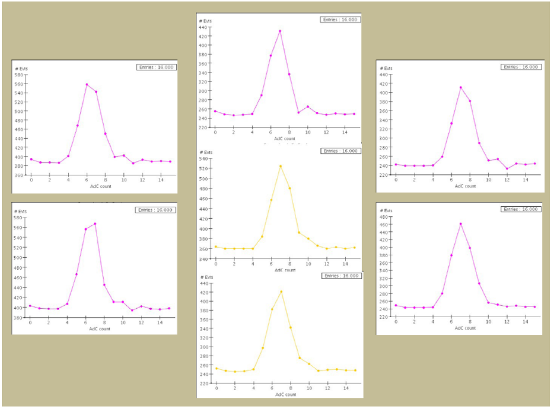


Functionalities:

- Ethernet connection
- Module time synchronization (1 pps)
- Power distribution
- L0 distribution
- L1 distribution
- Backplane of central module used for L1 decision (AT)

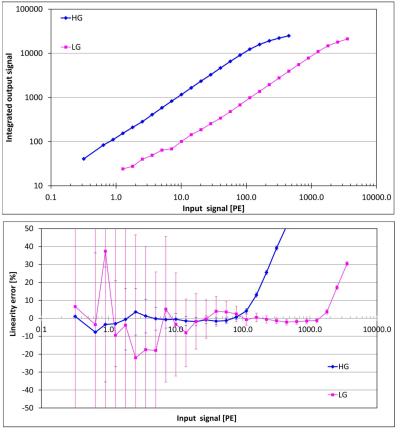
Discussions for a common design with DragonCam team. New design compatible with digital trigger.

Tests of the NECTAr module: 7 channel response



Low gain, 7 channels, sampling rate 1 GHz, signal amplitude $\sim$ 64 **PE**

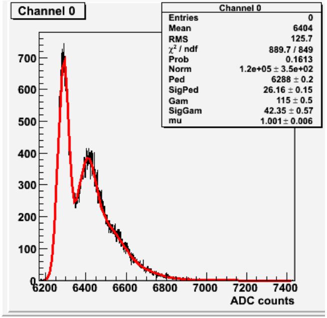
Tests of the NECTAr module: linearity



High gain (HG) and low gain (LG) output as function of the input signal.

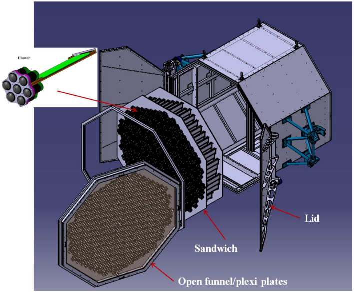
- prelimary results obtained with ACTA3
- charge integrated over 16 samples
- linear up to 100 PE (HG), 1000 PE (LG)
- required 3000 PE can be obtained by lowering the ACTA LG by ~ 2.

Tests of the NECTAr module: single PE

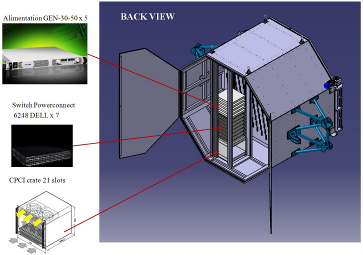


SPE spectrum obtained with the NECTAr module prototype. One channel of the NECTAr module prototype was equipped with PACTA and ACTA preamplifiers. The photomultiplier gain was set to the nominal value of 5 10^4

Mechanical design: global view



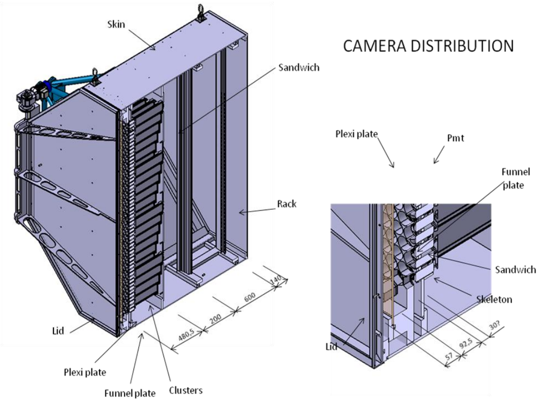
Front view



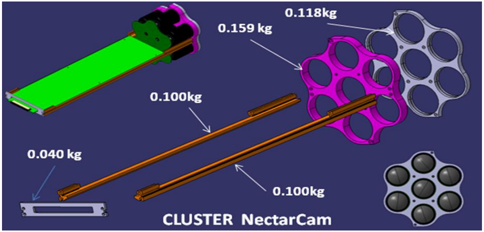
Rear view

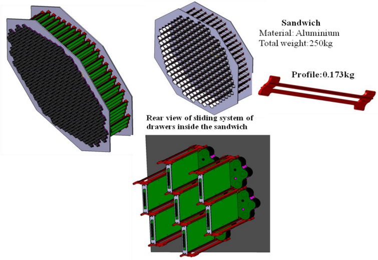
- made of aluminium tubes, with sides covered by a skin
- total weigth (all included) = 1.9 tons (less than required 2.5 tons)
- front: funnel plates, entrance window, sandwich with NECTAr modules
- back: single (cPCI) crate with slc, safety, camera server

Camera distribution



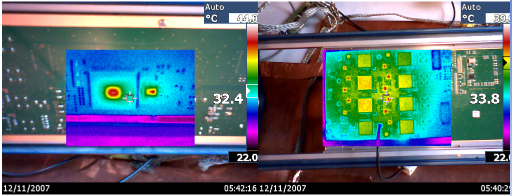
Module mechanics

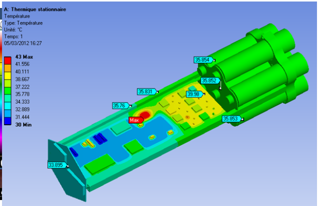


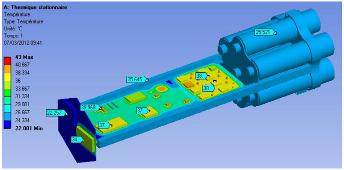


- first prototype available
- redesign to accomodate the PMT spacing of 50mm
- total weigth = 1.64 kg

Cooling





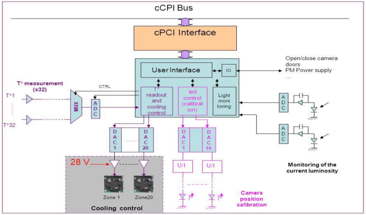


- FEM 3D model for drawer module with thermal characteristics of electronics elements
- $T_{\text{external}} = 22\ ^{\circ}$

Preliminary results:

- with no cooling, $T < 36^{\circ}$ on structure, T map agrees with measurement
- convection with low air flow, $T < 25^{\circ}$ on structure, $T < 40^{\circ}$ on components.

Monitoring, slow control



Safety and slc solution used for the H.E.S.S. 2 Camera

Slc/safety system located in (cPCI) crate in the rear of camera
Monitoring/safety functionalities:

- Camera temperature, pressure and humidity
- Temperature regulation
- Ambient light, if too strong, HV will be quickly shut down to protect the PMTs.
- Camera parameters (doors, HV, Power supplies, CPU reset . ..)

Control:

- LED obstructing system placed on the doors
- Mylar film (SPE measurement).
- Reference external PMT (SPE measurement).

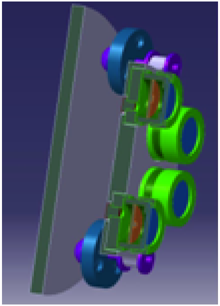
Calibration

Parameters to measure/monitor:

- Pedestals: ADC position in the absence of signal.
- Flat-fielding: Corrects for inhomogeneities in the photon detection efficiency of the camera pixels
- Gain Calculation: Relates the number of digital counts at the digitizer to the number of PE generated at the photocathode.
- SPE height spectrum

Calibration performed with bright LEDs ($>\sim$ 30 PE per pixel). Baseline characteristics:

- UV Range : 300-500nm
- low consumption (few mW)
- nominal brightness $>$ 3000mcd
- power angle $>$ 40% at 6 degrees



LED module, with a single UV source

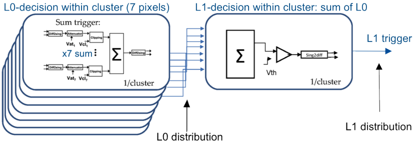
Conceptual design still ongoing.
First prototype should be available by end 2012

Analogue trigger implementation

Same implementation possible for LST, MST and SST

Front-End elements:

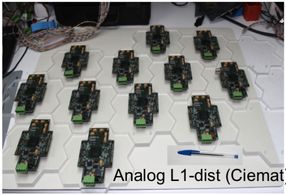
- L0-decision: Analog sum of signals in 1 cluster
- L1-decision:
  - Analog sum of L0 signals from neighboring clusters from all trigger regions (2, 3, 4 clusters)
  - L1 trigger (camera trigger) generated if any L1-decision sum in the camera above a given threshold
  - Allows Region of Interest autonomous readout



Analogue trigger implementation (continued)

Backplane elements:

- L0-distribution: Fan-out to neighbors for L1-decision
- L1-distribution:
  - Module-based distribution network interconnecting neighbors with a low-cost FPGAs in each module
  - L1 signal distribution to all camera within < 1ns
  - Allow Region of Interest autonomous readout (Colibri)
  - Allow super-module grouping for reduced cost and power


Analog L1-dist (Ciemat)

Tests of analogue trigger prototypes

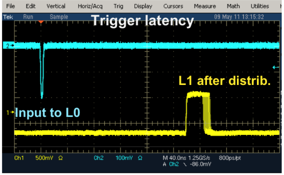
Working prototypes of all elements, in mezzanine boards to ease testing. Eventually integrated in FE and BP boards.
Stand-alone tests (Colibri version):

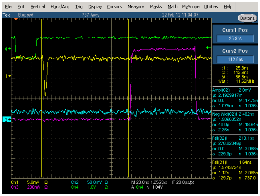
- Tests interconnecting all trigger elements
- Latency: 200 ns
- Noise: 0.3 phe
- Dynamic range: 0.4 200 PE
- Clock jitter: 5 ps increase @ 10 MHz

Integration test with NECTAr module:

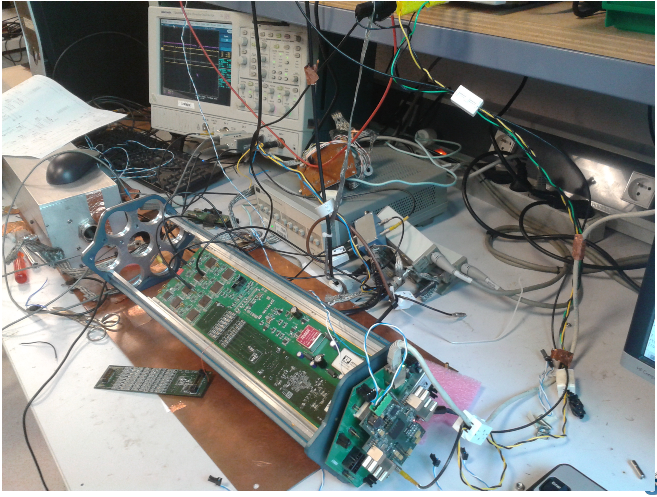
- setup: all trigger elements equipping one NECTAr module
- Full tests including LEDs + PMTs + Readout + Trigger
- Analog Trigger compatibility verified

Future tests with 3, 7, 19 modules



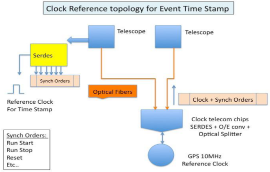


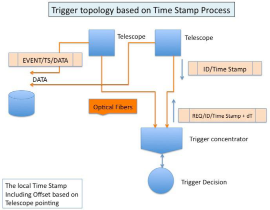
AT Integration tests with the NECTAr module



Integration tests of the L0,L1 AT with the NECTAr module

Clock distribution, module synchronisation





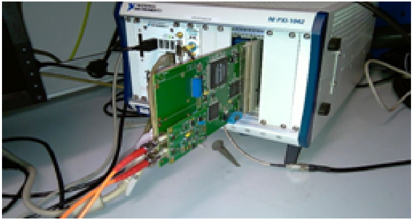
Clock distribution:

- Central GPS, distribution of 10 MHz and 1 pps
- Transmission with dedicated fibre-optic links
- Uses MUTIN boards at each end of the links
- 1 pps signal distributed to NECTAr modules
- Events are time stamped-in camera server

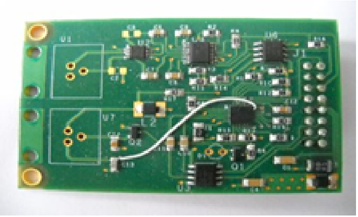
Array trigger

- Event time stamps sent to central trigger
- Look for time coincidence between telescopes
- Send back the read-out request

Clock distribution prototypes

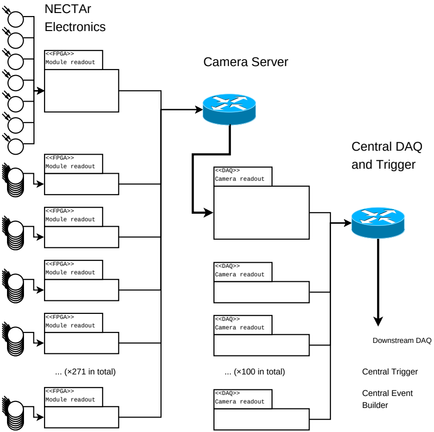


PXI crate with a MUTIN card on an extender board



Layout of one of the optical daughter boards

Data acquisition



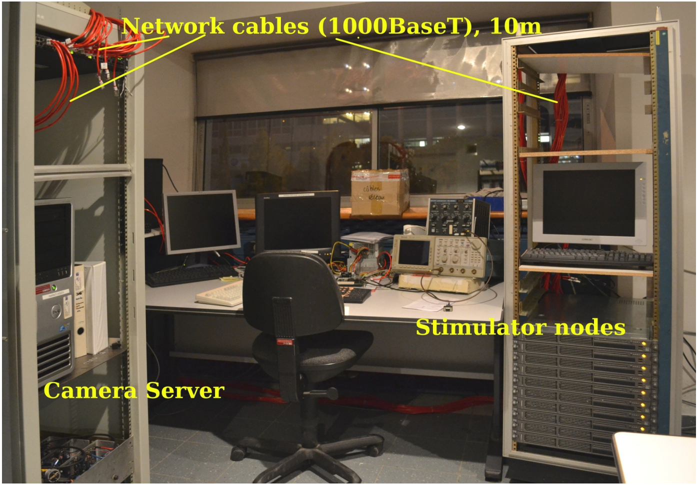
Architecture

- concentration of 46 NECTAr modules in multi-1-Gb/s switches
- 20 Gb/s connection switches → camera server
- 10 Gb/s connection camera server → central DAQ
- use COTS hardware/software to reduce costs

Tests

- use 1 DELL server + 1 switch
- Camera server receives and recontructs data
  -consistency check of input
  -buffer, possibility to react on trigger
  -possibility perform online reconstruction for more sophisticated higher level trigger decision
- Test with standard libraries/drivers up to 19.6 Gbps on 2x10 Gbps links
  -no need for low-level ethernet programming

Data acquisition test setup



Conclusion of developments: "readiness"

Item	TRL	Legacy
Focal plane equipment		
Light guides	4 to 5	Similar concept used in MAGIC and H.E.S.S. I
Entrance window	4 to 5	Concept validated by MAGIC
Photo-detectors	3 to 4	CTA candidate
Pre-amplifier (PACTA)	4	Integration work with HV under evaluation
HV power supply (ISEG)	4	HE.S.S. I and II HV boards
Front-end electronics & trigger		
Front end architecture		H.E.S.S. cameras
Analogue pipeline (ASIC)	4 to 5	Similar chip used for H.E.S.S. II
Front-end board	4 to 5	Tests done with full chain from PMT to GUI
NECTAr Backplane card	4	Discussion ongoing to design common CTA BP.
Analogue trigger (AT)		Similar concept used in MAGIG and H.E.S.S. I
AT L0 trigger	4	6 prototypes functional
AT L1 trigger	4	5 prototypes fully functional
AT L1 distribution	4	12 prototypes fully functional (incl. Firmware)
AT CLK distribution	4	12 prototypes fully functional (incl. Firmware)
AT backplane	4	Concept of super backplane under evaluation
AT delay lines	3	Concept under evaluation
Digital trigger (DT)	3 to 4	prototypes available
Camera processing & monitoring		
Camera DAQ	3	
Camera slow-control & monitoring	4	
Camera trigger	2 to 3	
Power	2 to 3	
Calibration systems	3	
Safety	5	Similar design implemented in H.E.S.S. II
Camera mechanics & cooling		
Embedded camera concept		H.E.S.S. cameras
Camera telescope connection	4	
Camera body	4	Similar concept used in H.E.S.S.
Camera inside	4	Similar concept used in H.E.S.S.
Module mechanics	4	Similar concept used in H.E.S.S.
Module cooling	2	
General cooling	2	
Humidity control system	2	

Table: Technology Readiness Levels of NECTArCam components

Power

Item		Unity power	Qty / camera	Total / camera
Automatism		50.00	1	50
Module	Estimate (with 85% DC/DC eff.)	16.3	271	4417.3
Front-end board	Using ACTAlow power amp.	9.65		
Analog trigger	Estimate AT scheme	5.25		
HV + PMTs	Reduced power on the new prototype	1.40		
cPCI crate	estimate CPU, + SLC + Safety	300.00	1	300
DAQ (all)	max	1,200.00	1	1200
Others		75.00	1	75
		W/channel		W/ camera
	Total	3.19	$\Leftarrow$	6042.3

Dissipation/pixel fulfills requirement (< 5 W)

Weight

Item		Unity weigth	Qty / camera	Total / camera
Camera mechanics				
	Skeleton	420	1	420
	Skin	60	1	60
	Sandwich	250	1	250
	Funnel plate	140	1	140
	Automatism	100	1	100
	Entrance Window	80	1	80
	Lids	70	1	70
	Interface Camera/Telescope	100	1	100
	Others	50	1	50
Module : prototype		1.64	271	444.44
cPCI crate		30	1	30
CPU		1.3	3	3.9
Safety cards		10	1	10
DAQ switch		70	1	70
Power supply		10	5	50
Auxiliary systems		20	1	20
cables		30	1	30
Others		30	1	30
		kg/pixel	Qty / camera : 1897	kg/camera
	Total	1.03	⇐	1958.34

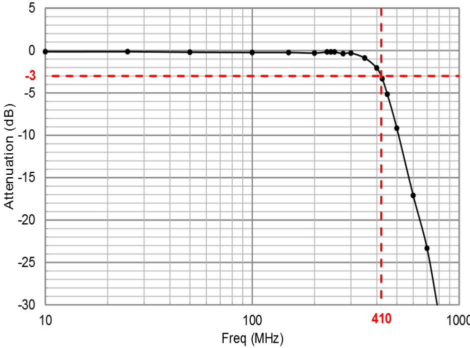
Total weigth fulfills requirement (< 2.5 tons)

Cost

Item		Unity cost	Qty / camera	Total / camera
Photodetectors & optics	**462,949.50 €**	244.04 €		
Entrance window	FPI estimate	20,000.00 €	1	20,000.00 €
Light guides	FPI estimate	14 €	1897	26558.00 €
PM Tube	FPI estimate	170.00 €	1897	322490.00 €
Preamplifier + HV	estimate + offer	45.00 €	1897	85,365.00 €
Mechanics	**331,975.00 €**	175.00 €		
Module mechanics	estimate	385.00 €	271	104,335.00 €
Camera mechanics	estimate	120.00 €	1897	227,640.00 €
Front end electronics	**210,025.00 €**	110.71 €		
read-out board	estimate	550.00 €	271	149,050.00 €
Trigger	based on AT estimate	100.00 €	271	27,100.00 €
Backplane	estimate	125.00 €	271	33,875.00 €
Camera processing & monitoring	**91,500.00 €**	48.23 €		
cPCI crate	estimate	10,000.00 €	1	10,000.00 €
CPU	estimate	3,500.00 €	3	10,500.00 €
Safety cards	estimate	20,000.00 €	1	20,000.00 €
DAQ (switch + server + cables +...)	estimate	20,000.00 €	1	20,000.00 €
Power supply	offer	2,200.00 €	5	11,000.00 €
Auxiliary systems	estimate	10,000.00 €	1	10,000.00 €
cables	estimate	10,000.00 €	1	10,000.00 €
			Total 1 camera	1087913 €
			cost / pixel ⇒	573.49 €

Analogue Bandwidth and timing measurements

- Analogue BW of NECTAr chip measured with test board = 410 MHz.
- BW of ACTA/PACTA=500 MHz
- Analogue BW should be > 400 MHz, larger than 300 MHz requirement
- Other contributions to timing errors: clock synchronization, transit time spread of PMTs, etc under investigation



Dynamic range, charge resolution

Measurement conditions:

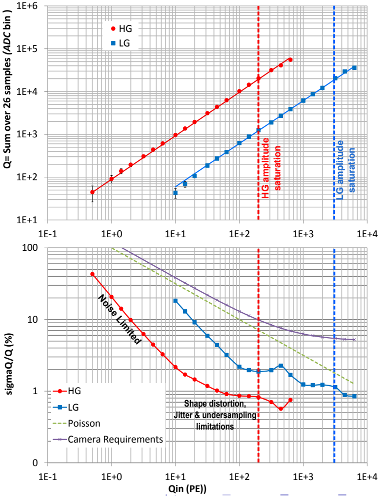
- NECTAr chip test board
- 2 Gains: x1 and x16 (commercial amplifiers)
- "Electrical photoelectrons"
- sampling 2GS/s
- Charge calculated on 26 samples.

Linearity

- HG amplitude saturates @ 200 PE
- LG amplitude saturates @ 3000 PE
- charge measurements OK to $\geq$ 6000 PE

Charge resolution

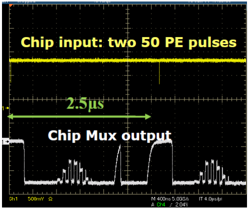
- 20 % resolution on SPE
- Floor resolution of 0.8% @ large charge on HG
- consistent with sampling jitter $<$ 40ps rms
- better than requirement at all charges



Maximum trigger rate, dead time

Tests with periodic pulses

- 2 consecutive triggered pulses (50 PE charge) separated by $\Delta t = 2.5\ \mu s$
- FPGA operating in "charge mode" with 16 samples
- Pulses acquired without any loss of data
- charge resolution equivalent to single pulse $\Rightarrow$ RO deadtime of the NECTAr chip $< 2.5\ \mu s$

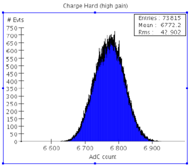


Variation with burst period

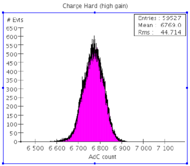
- burst period progressively decreased down to 20 μs (limited by test acquisition software)
- no data loss
- no charge resolution degradation

FPGA read by UDP link can sustain a rate of trigger and data of $\geq$ 100 kHz
If dead-time of NECTArCam only due to chip RO, deadtime $<$ 1.5 % @ 6 kHz trigger rate $\Rightarrow$ fulfill requirement.

Charge (16 samples 1GS/s) distributions



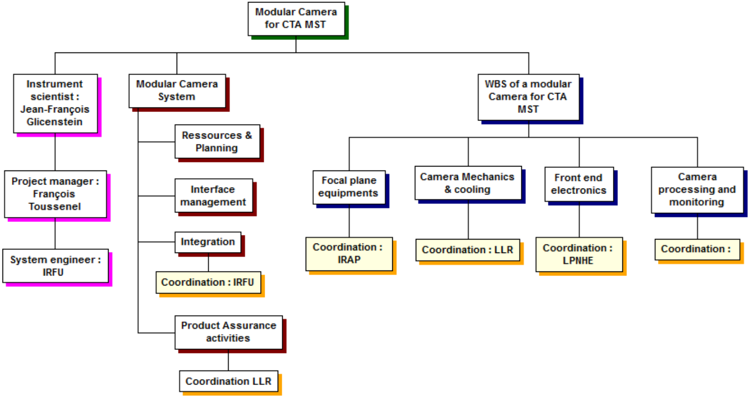
Single Pulse



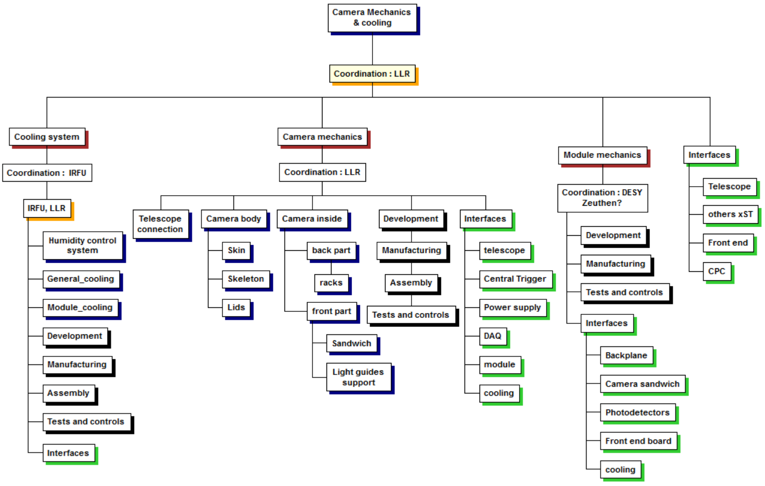
Double Pulse

Measurements of the response of the NECTAr prototype module with Poisson distributed pulses planned.

Organization of the NECTArCam project



Organization of the mechanics task



Preparation for industrial production

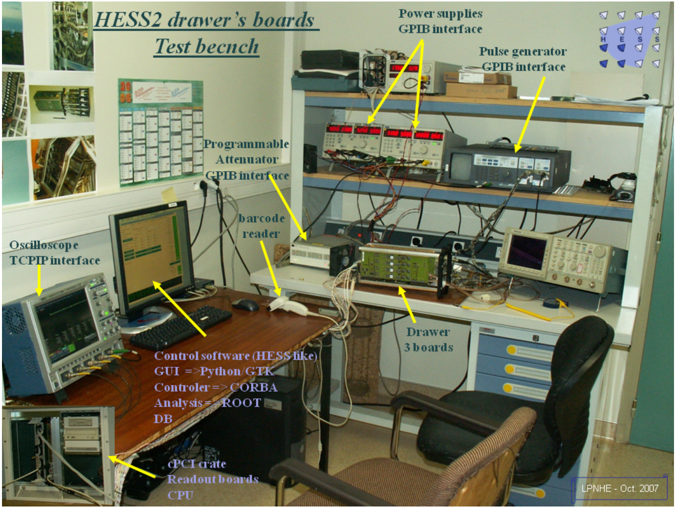
The NECTArCam has

- a reduced number of elements
- as simple as possible interfaces between sub-systems
- modular design ⇒ possibility to test the sub-systems independently

Lessons from H.E.S.S-2:

- Validation of sub-systems ⇒ development of a dedicated test bench and associated software
- Same test-bench/software to be used in the industry
- Reliability improved with HALT/HASS tests.

Test bench setup (H.E.S.S-2)



Prototyping

Purpose of demonstrator:

- validate the trigger scheme, the DAQ scheme, the mechanical structure and interfaces with other systems (such as the power supplies, central/array trigger and cooling system).
- establish and validate the testing and integration procedures→knowledge transfer to industry and other labs

Demonstrator:

- composed of 19-37 NECTAr modules
- all other relevant parts: mechanics, cooling, trigger, DAQ etc
- modular system ⇒ allows the validation of full camera

Risk management

- production of a NECTArCam risk management document (MST-CAM/20120309)
- risk list adapted from the IN2P3 risk list
- risk assessment based on severity (1-4-7-10) and probability of occurence (1-3-6-8-10)
- risk index = severityx(probability of occurence)

Occurrence Probability of		Risk magnitude convention based on the Risk Index			
	Very High 10	Medium risk	High risk	High risk	High risk
	High 8	Medium risk	Medium risk	High risk	High risk
	Significant 6	Low risk	Medium risk	Medium risk	High risk
	Low 3	Low risk	Low risk	Medium risk	Medium risk
	Negligible 1	Low risk	Low risk	Low risk	Medium risk
		Low 1	Significant 4	Critical 7	Catastrophic 10
		Severity			

No severe technical risk was identified for the moment (risk list is dynamic)

Several medium risk have been identified.

Risks list (excerpt)

Identification						Assessment			
Number	Risk description	Cause and consequence	Comments / Possible actions	System or subsystem concerned	Risk impact type (technical, cost, schedule, safety)	Severity 1 Low 4 Significant 7 Critical 10 Catastrophic	Probability of occurrence 1 Negligible 3 Low 6 Significant 8 High 10 Very high	Risk Index = Severity x Probability	Risk magnitude
Camera									
0070	Sustainability of the industrial (economic, sector of activity,...)	incomplete production, delay, change of industrial	the probability is high because of the economic context (crisis)	Camera	Cost, schedule	7	6	42	Medium risk
0038	Loss of expertise during the development of an element	because of the expert departure	Critical tasks need to have regular meetings, to formalize and share experiences. the risk disappear when the element can be producted (the development is finished)	Camera	schedule, cost, technical	5	6	30	Medium risk
0056	Significant delay in public procurement	delay		Camera	Schedule	6	5	30	medium risk
0006 to 0007	Poor communication inside the project	misunderstantding, lake of information ---> delay, sub systems incompatible	weekly meeting	Camera	schedule, technical	7	3	21	Medium risk
0003 to 0005	Poor definition of the interface and /or tasks : ommission of an interface and /or a task	interface or task not taken in account ---> the camera is not operated ---> unsatisfaction of collaboration, delay	Low probability of occurrence thanks to the work done on the detailled PBS and WBS	Camera	schedule, technical	6	3	18	Medium risk
0028 to 0030	Tardive definition of specifications	Requirements not taken in account in the design, performance not met Requirements taken in account very late requiring changes of the design ---> delay, overcost		Camera	Schedule, cost	5	3	15	Medium risk
0020 to 0022	Poor definition of the need / of the specifications	the camera doesn't meet the scientific requirements, low performances the camera is too efficient, upper	project reviews decrease the probability of occurrence	Camera	cost, technical	4	3	12	Low risk
0023 to 0027	Scientific needs changes	the camera is too efficient, upper performances ---> unnecessary extra cost the camera doesn't meet the scientific requirements, low performances the camera is not adapted to environmental constraints (temperature, humidity ...), risk of failure the design must be modified --> delay, overcost		Camera	schedule, cost, technical	4	3	12	Low risk
Camera DAQ									
0073	Problems with implementation and deployment of our solution on large scale	incompatibility with the chosen equipment, debug/development, unexpected cost	Choice of COTS makes reduces risk to a reasonable minimum	Camera DAQ	cost, technical	7	3	21	medium risk
0074	DAQ requirements exceeding possibilities of our solution	Modification of physics requirements, modification of DAQ s/w, delay and overcost	The existing solution margins can satisfy more needs	Camera DAQ	cost, technical	4	3	12	Low risk

Milestones for the NECTArCam project

Several milestones have already been achieved:

- Milestone1: 01/2011 7 pixels HV board available
- Milestone2: 03/2011 NECTAr0 test board available
  - validation of NECTAr0 chip with in-ADC, Eth link for readout, java GUI & Power strategy
  - first Single photoelectron spectrum with PACTA + NECTAr0 at a gain of 5.10^4
- Milestone3: 10/2011 : NECTAr module prototype available
- Milestone4 : 01/2012 : Preliminary tests with ACTA+PACTA, analog trigger integration tests
  - Validation of the full read-out chain with the final preamplifiers (CTA PMT + ACTA + PACTA + NECTAr0)
  - Successful integration of the AT mezzanines

The next milestones for building the camera demonstrator are:

- Milestone5: 12/2012 Several modules available, software development, mechanical structure
- Milestone6: 03/ 2013 Assembly of a 19 module demonstrator with associated DAQ, Trigger system, Slow control, Calibration and mechanics.
- Milestone7: 09/2013 Demonstrator test and validation
- Milestone8: 03/2014 Concept fully worked out, ready to start camera production.

Conclusion

NECTArCam is a modular camera designed for the MST
Adaptable to other types of telescopes
A first module prototype has been built and tested. It fullfils the CTA requirements.
The NECTArCam group has worked out a WBS to coordinate the development/organization/integration tasks.
Development work is ongoing in focal plane instrumentation, mechanics, electronics and camera processing, and quality assurance.
A fully equipped demonstrator with 19-37 modules will be built.