Commodity readout electronics for an underwater neutrino telescope

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Abstract

Typically the front end electronics required for a neutrino telescope, incorporates electronics to perform waveform capture of photomultiplier tube signals, possibly applying a local triggering algorithm and transmission of the data to the shore. We show how a commodity based system which employs Component Off The Shelf (COTS) devices, with Flash Analog to Digital Converters (FADCs) and Field Programmable Gate Arrays (FPGAs), can be used for synchronous signal digitization of multiple photomultiplier tubes. The transmission link to the shore has been realized using the standard communication protocol of Gbit Ethernet through fiber. We describe the readout system and our designs to interface with existing electronics for control and operation of a neutrino telescope.

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1. Introduction

A front end electronics platform to capture the waveforms of signals from multiple photomultiplier tubes for an underwater Neutrino

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telescope requires three parameters: fast ADCs, processing power (FPGAs) and a data transfer bidirectional interface between the underwater site and the shore site. Hardware units to accomplish each of the three functions exist in the marketplace; however, single platforms integrating all functions with the desired specifications have only recently become available as a COTS system.

In this paper, a commercially available system fulfilling our requirements is briefly described along with our design of additional boards needed to augment the operability for an underwater neutrino telescope.

2. System Requirements

The specifications are partially fixed by the application requirements to read out the Optical Modules (OMs)[1] and partially by market availability.

The system requirements are:

a) waveform capture for acquiring the signal from multiple OMs;
b) sampling rate greater than 200MSPs (Mega Samples Per Second) due to signal frequencies [1];
c) analog input bandwidth greater than 200MHz due to signal frequencies [1];
d) analog input dynamic range from -60mV to -1.2V which is equivalent to about 1 - 20 Single Photoelectrons respectively;
e) amplitude resolution equal to or better than 8 bits;
f) external general purpose I/O for signaling;
g) standard high bandwidth interfaces for data transfers from the underwater site to the shore site;
h) the capability to process the captured waveforms and implement a trigger;
i) standard PC interface (PCI/PCIX) and form factor (fit on a standard pc motherboard);
j) power consumption of less than 25W per OM;
k) a cost per OM of less than 3000€.

The readout electronics is actually an off the shelf system commercially available produced by the Nallatech [2] company.

3. System Description

The system architecture is separated into two regions the on-shore and the off-shore (deep sea) site, connected through the electro/optical cable which provides power to the system through its electrical conductor and data transfer through its optical fibers.

The on-shore system consists of the clock generation and transmission system, the data reception and storage and the command transmission to the off-shore system.

The off-shore system consists of the clock reception, synthesis and fan out system, the readout electronics, the monitor and control electronics, the calibration electronics and the communication devices.

3.1. The Clock Distribution System

The clock distribution is a custom made system using a GPS unit incorporating a high precision Rubidium clock. It has the capability of generating a 10MHz reference frequency and adheres to the UTC standard. Clock signal and transmitted optically to the off-shore system. At the point of reception the optical signal is converted back to electrical. This 10MHz reference frequency is then used to synthesize the 250MHz clock that the readout electronics require. This 250MHz is fanned out to 4 channels with a maximum skew of 35ps.

3.2. The Readout Electronics

The readout system is comprised of two distinct parts; the mother card, see fig. 1 and the daughter card, see fig.2. The mother card has a 64-bit 33MHz PCI interface a Xilinx Virtex II Pro FPGA and three slots for daughter cards, interconnected with several high bandwidth, low latency buses.

A daughter card has a Xilinx Virtex 4 FPGA and a quad 12-bit flash ADC sampling at 250MSPS. When fully equipped, the system can perform continuous sampling at the above rate for 12 OMs and has the potential to search for signal patterns on a sample by

sample basis (every 4ns). Between the daughter cards - and between the daughter cards and the main mother card FPGA - are 32-bit and 64-bit high bandwidth buses and a common 122-bit bus interfacing all FPGAs together, giving the ability to the system to transfer high volumes of parallel data. The four FPGAs with the interconnecting low latency buses provide adequate processing power to implement local triggering algorithms which can be applied to the digitized signals of all OMs. We have implemented local algorithms with programmable parameters such as the input signal thresholds, the width of time windows in which to search for OM coincidence signals and the multiplicity of OMs required for a temporal and/or spatial coincidence search. In addition, we have implemented trigger schemes based on external signals interfaced to the readout card.

Two routes are available to transfer data from the readout electronics to the station on-shore through Ethernet (1Gbit) connections. - either via the host PCI bus and an external Ethernet connection or through the multiple Ethernet connections available on the mother card. Both routes are available for controlling the readout card remotely.

The mother card also provides interfaces with general purpose I/O lines that have been used for interfacing custom electronic modules [3] for the slow controls of the detector and for signaling between various spatially separated, readout boards of different sets of OMs.

Fig. 1. Readout Electronics Mother Card

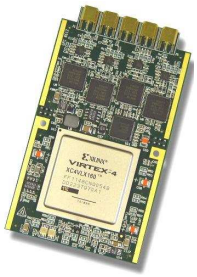

Fig. 2. Readout Electronics Daughter Card

3.3. Detector Monitor & Control Electronics

A custom made board, the housekeeping system, that is directly connected to the readout board to receive commands and transmits data, provides power to the OMs and controls the high voltage applied to them. This is done by digitally controlled power relays and digital to analog converters. It monitors the high voltage of the OMs and all the environmental sensors such as compasses, tilt meters, accelerometers, thermometers, hygrometers, pressure sensors and the main voltage supply of the detector. It interfaces with two calibration LED beacons and controls the rate of pulsing, the amplitude, and synchronization of the pulse sequence between two beacons. All these functions are implemented in firmware on an Altera Flex10K FPGA.

3.4. Calibration of Detector Readout Electronics System

Although the performance of the Flash ADCs is guaranteed within the specifications given by performance tests of the manufacturer, it is necessary to know *in situ* that it remains unchanged. Another aspect that must be checked is the clock skew amongst daughter cards.

To facilitate these evaluations we have designed an electronic circuit that multiplexes external OM signals with external calibration signals. High bandwidth amplifiers allow this multiplexing to take place. Hence, one will have the ability *in situ* to make a dedicated calibration run and monitor the performance of the readout electronics.

4. System Tests and Characterization

A very important aspect of the whole system, the readout card and monitor and control boards, is the power consumption. Powered from a 300V supply line all necessary voltages are generated using DC to DC converters.

Results from the first measurements of power consumption, for the system both in idle and in digitizing and triggering mode, are shown in table 1.

Table 1. Results from power consumption tests

Configuration	Readout Electronics Consumption (W)	Readout Host (W)	Monitor & Control Electronics (W)	Total System Consumption (W)
Idle	10	60	8	78
12 Channels	120		90	210

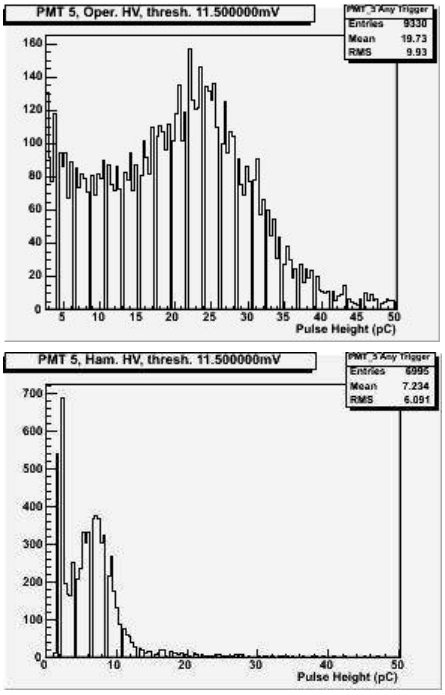

Fig. 3. Plots of pulse height distribution at two different high voltages for single photoelectrons in an optical module equipped with a 15-inch photomultiplier.

This system has a power consumption per Optical Module of about 17W. However these figures have been produced from measurements without optimizing the power consumption of the system, such as deactivating devices that are not used continuously.

A program of extensive system tests is in progress, to characterize the system performance, using multiple OMs in the NESTOR Institute dark room test bed [4]. Figure 3 shows pulse height distributions of an OM at two different high voltage settings for single photoelectron signals.

5. Conclusions

We have a positive experience with the Flash ADC / FPGA readout electronics tested in our test bed succeeding simultaneous 12 channel digitization at 250MSPs capability, local processing power for algorithm implementations and very easy interface of custom electronics using the general purpose I/O lines.

Additional tests are planned for long term stability using convection cooling and development of high throughput interconnects to shore.

This exercise proves that a commercially available piece of hardware can be used for the purpose of an underwater neutrino telescope

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