Low Power Multi-Dynamics Front End Architecture for the Optical Module of a Neutrino Underwater Telescope

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Abstract

A proposal for a new front-end architecture intended to capture signals in the optical module of an underwater neutrino telescope is described. It concentrates on the problem of power consumption, signal reconstruction, charge and time precision.

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1. Introduction

The work described in this paper is aimed at the development of the low-power front-end for the OMs of the NEMO submarine neutrino detector [3,4,5,7].

This solution is based on the use of an Application Specific Integrated Circuit (ASIC) for the fast sampling of the PMT signal, which is performed according to its shape classification made by another unit. Two other units, one ADC and a Field Programmable Gate Array (FPGA), provide digital encoding of the voltage sampled signals, the packing of the data and its transfer towards the shore station.

An electronics board containing the PMT interface and the mentioned units constitutes the OM front-end. By means of the FPGA, this board receives the slow control signals and transmits the measurements of environmental parameters such as temperature and humidity, together with the data.

2. The OM front-end

The design of the front-end is based on parameters and specifications that in some cases are not yet definitive, for the performance of the whole detector. We have used the most recent data coming from simulations of high energy neutrino events produced in a submarine detector in order to define the specifications of the front-end electronics that optimise the detector performance [2].

As a result of this study, an appropriate architecture has been defined for the system that performs the sampling.

The block diagram of the front-end under design is shown in figure 1. In the following sections all the blocks will be described in detail.

3. The PMT interface

The PMT interface, described in detail in [2], has been designed and tested with the NEMO PMT in a dark box using a laser light.
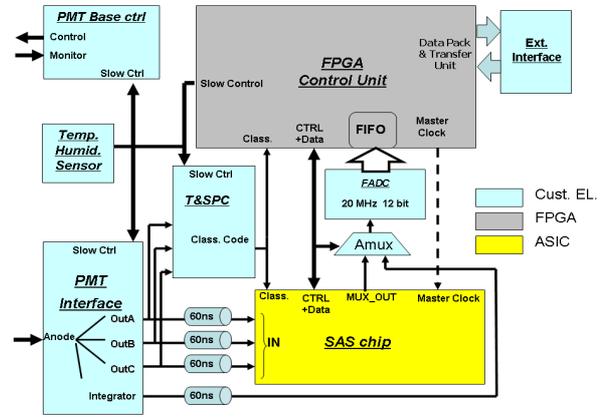

Figure 1: The block diagram of the OM front-end architecture.

The single pe signal amplitude, measured on the unitary gain channel of the PMT-interface, is about 1 V. We choose a voltage dynamic range of 2 V corresponding to 8 pe. So the gain of the PMT must be lowered by a factor of about 4 which means $1,2 \cdot 10^7$, with the effect of reducing the PMT aging and the dark current [8] and increasing the PMT linear dynamic range.

The rise time of the signals is about 12 ns due to the increased time constant of the input anodic circuit. An additional filter avoids aliasing effects in the 200 MHz sampling performed by the analogue memories.
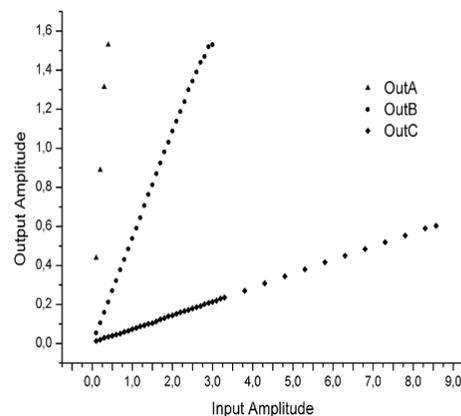

Figure 2: Linearity and gain of the PMT interface outputs.

The gain values of the three output channels are settable by changing the resistor ladder at the input of the PMT-interface. The current consumption of the PMT interface board is 8 mA at 3.3 V. The PMT interface response to voltage waveforms with different amplitudes emulating the PMT signal has been used to characterize the gains of the three linear channels, Out A, Out B and Out C (see figure 2).

4. The Trigger and Single Photo-electron Classifier

The Trigger and Single Photo-electron Classifier, called the T&SPC, is the unit devoted to generate the trigger for acquisition and the classification of the PMT signals.

The T&SPC consists of four fast comparators with hysteresis, a slow control interface and two 6 bit DACs. The two thresholds, Th0 and Th1, generated by the DACs, can be set by slow control, through a serial code.

The signal Out A coming from the PMT-interface is compared to the threshold Th0 and the result of the comparison is labelled SOT for Signal Over Threshold: the rising edge of this signal is used as the start of the signal sampling and time stamping, while its pulse width is used for the signal classification.

A second threshold (Th1) is used to determine the over-range condition for all the outputs of the PMT-interface by three more comparators. This threshold is equal to the voltage limit of the three linear dynamics. The output of the three comparators constitutes the signal amplitude classification (classification code), used to choose the sampling record length (see next session).

The classification code and the SOT signal are directly sent to the SAS chip while the PMT-interface signals are delayed and filtered.

5. The Smart Auto-triggering Sampler chip

This new integrated device, called Smart Auto-triggering Sampler (SAS), will consist of functional blocks very similar to those already designed and successfully tested in the chip LIRA05[5]. This choice allowed to introduce the performance of each block into the simulations of the whole front-end making their results more significant and realistic.

The block diagram of the SAS chip is shown in figure 3.

The chip consists of four main blocks: the analogue memories, the control unit, the analogue multiplexer and the counter.

The three input signals shown in figure 3 are the delayed replicas coming from the PMT-interface outputs of figure 1: these signals are internally buffered and made continuously available to the 5 analogue memories.

All the analogue memories have a voltage sampling-voltage transfer architecture and the schematic of the sampling cell is shown in figure 3. The memories are divided in two specialised groups. Four modules consist of 3 channels of 16 cells each, called SCA_Short in the figure: they are dedicated to the sampling of the short time duration signals (up to 80 ns). One module, called SCA_Long, consists again of 3 channels but with 128 cells each, for their digitisation.

cells each: this is used only for signals exceeding the 80 ns timing limit.
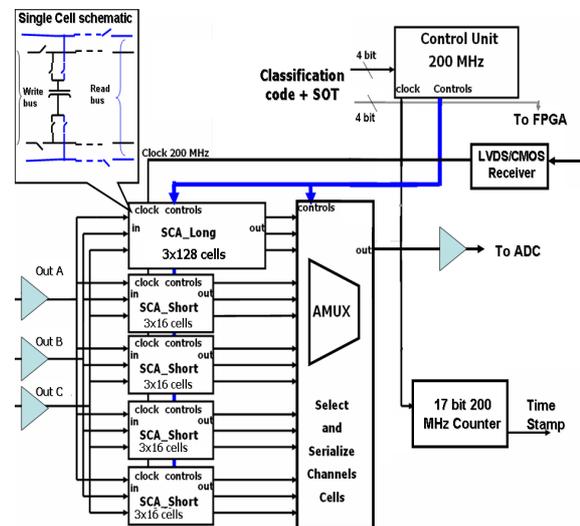

Figure 3: the block diagram of the SAS chip.

The sampling of all three signals starts after a rising edge, produced by the PMT-interface on the input of the SAS, and ends after the full depth of the unit has been reached. Each analogue memory

samples the voltages at its three inputs and stores them in an array of switched capacitors, to be made available through the analogue output multiplexer for the digitisation performed by the external ADC. One of the analogue memories is actively sampling the signals after being started, while the others are retaining the previously acquired signals waiting for a readout request coming from the FPGA-Control Unit.

The analogue multiplexer, shown in figure 3, selects the correct analogue memory block and channel for the serial transfer towards the ADC under the control of the FPGA-Control Unit.

At a given time only one of the four SCA_Short is waiting for the start sampling signal issued by the T&SPC: if other SOT events arrive while one SCA_Short is still transferring its data, the next SCA_Short will start sampling in circular chain. The number of SCA_Short, their depth and the ratio between write and read frequencies have been optimised for the expected highest event rate of 300 kHz, giving a negligible dead time.

The write and read frequencies of the SCA_Long are the same as the SCA_Short: in the occurrence of an event longer than 80 ns, all the samples stored on its three channels are transferred towards the ADC. In the case of low amplitude signals, when the signal voltage is within the first input dynamics, Out A, only the samples stored in the corresponding channel are converted. If the PMT signal exceeds all the three linear dynamics, being its charge higher than 512 pe, after one of the SCA_Short ends sampling, the ADC will be connected to the integrator output of the PMT-interface until the moment the SOT signal returns to zero. The Control Unit shown in figure 3 is an asynchronous digital circuit that produces the control signals for all the analogue memories as a function of the classification code and the SOT signal. It also has the role of acting as an interface with the FPGA.

The 200 MHz write clock is produced inside the FPGA by a DLL as an LVDS signal in order to reduce the noise and the power consumption.

The 200 MHz 17 bit counter also shown in figure 3 is used for time stamping the events at each rising edge of the SOT: its value is stored together with the analogue voltage samples and serially transferred to the FPGA each time an event is read.

SPICE simulations of the architecture indicate an estimated total power consumption lower than 60 mW. The technology used is AMS CMOS 0,35 μm.

6. Conclusions

A proposal for a system to capture signals in the Optical Module of an underwater neutrino telescope has been described, with focus on power consumption and dynamics considerations. All considerations regarding the signals and their acquisition are made starting from the most general hypothesis possible, so that they will be valid for any underwater Cherenkov neutrino telescope.

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