Fast Controller Roadmap

ITER_D_4C4N8S

Reference for diagnostics I&C functional specification

Fast Controller Definitions

- Fast Controllers are IN-KIND
  - CODAC HPC is NOT a Fast Controller
  - CODAC HPC has no I/O and is IN-FUND
- Fast Controllers have normally I/O
- Fast Controllers run RHEL and CODAC Core System (CCS)
- Fast Controllers have CCS interface on PON
- Fast Controllers CCS interface is configured by SDD
- Fast Controllers may interface to HPN
- Fast Controllers may produce scientific data streamed up using the PON archiving channel
- Fast Controllers may in addition run RTOS

Where are Fast Controllers Deployed?

- Diagnostics
- Coil Power Supplies
- Fuelling
- Heating (EC H&CD, IC H&CD, NB H&CD)
- …
- Mechanical stress (vacuum vessel, first wall,…)
- …

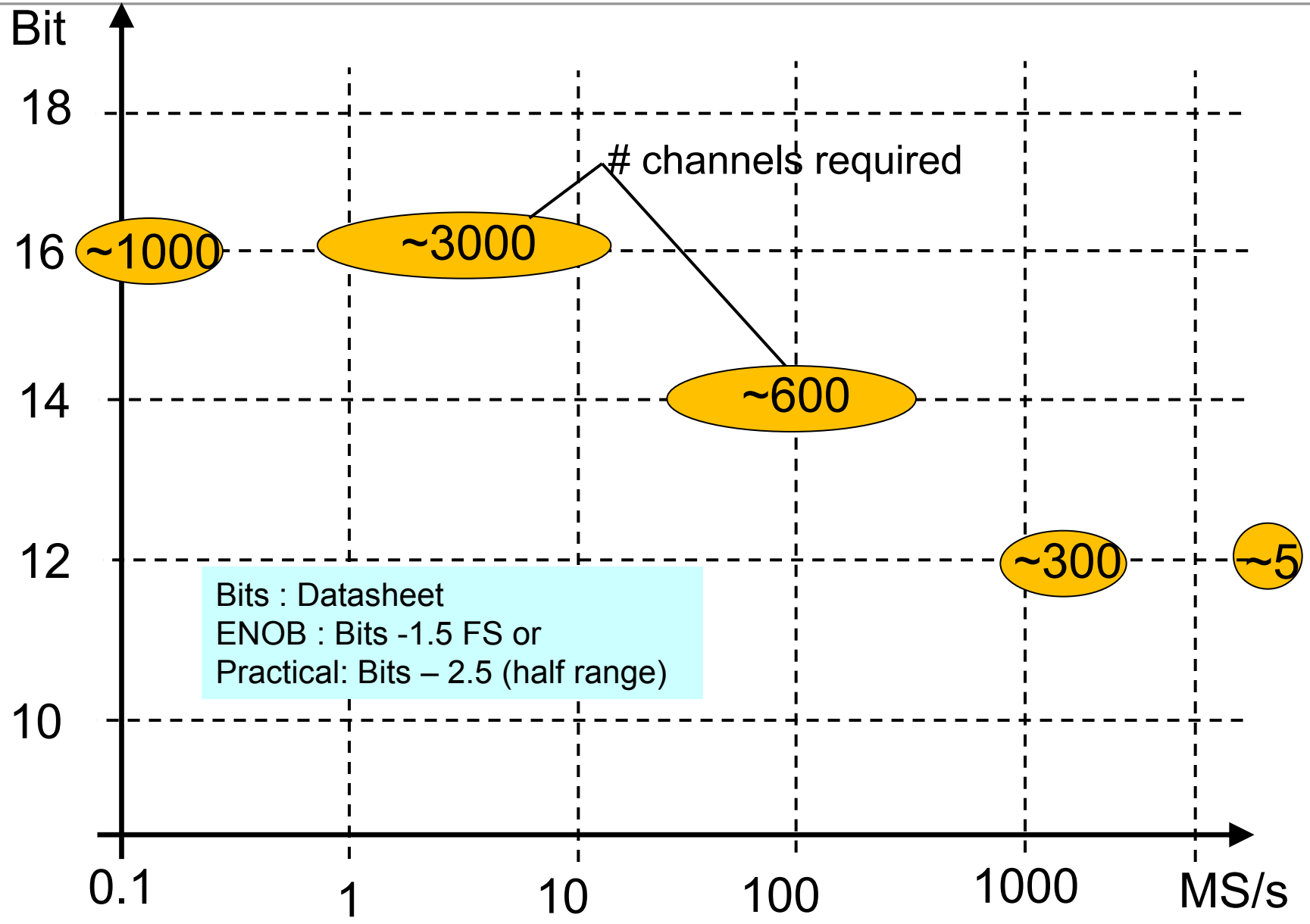
ITER will have many hundreds of Fast Controllers

PBS	~0.1 MS/s	1 -10 MS/s	~100 MS/s	~1 GS/s	Dig. I/O	Camera
11 (Magnets)	~100 ?	-	-	-	-	-
15 (VV)	~300 ?					
16 (Blankets) + 17 (Divertor)	~300 ?					
18 (Fuelling & Wall Cond.)	~10	-	-	-	~10	-
31 (Vacuum)	~10	-	-	-	~10	-
41 (Coil Power Supply&Distr.)	~150	-	-	-	~50	-
51 (ICH + CD)	~200	~100	-	-	~250	-
52 (ECH + CD)	~50	-	-	-	~250	-
53 (NB H&CD)	few 10	-	-	-	few	-
55 (Diagnostics)		~3000	~300	~200	~500	~24 (1kfps) ~200 (50fps)

Example: Fast Controllers for Diagnostics

Measurement Group	Signal Conditioning	Data IO	Signal Processing in Plant	Signal Processing in PCS
Magnetics	Chopper Amplifier (low offset)	1400 ADC (1 MS/s) 240 ADC (10 MS/s)	FPGA / GPU / CPU	GPU/CPU
Dosimetry and Fusion Products	Custom	50 ADC (100 MS/s)	FPGA / CPU	GPU/CPU
VIS/IR Cameras	Built-in Camera Functions	24 cameras (1 kHz frame rate)	FPGA / CPU	NA
Optical (ex. LIDAR)	Custom	150 ADC (20 GS/s)	FPGA/GPU	NA
Imaging Spectroscopy	NA	~ 200 cameras / Detector arrays	FPGA / CPU	GPU/CPU
Other spectroscopy and neutral particle analyzer	COTS Spectrometers	Custom	FPGA / CPU	GPU/CPU
Bolometers	Bias + Amplifier	~500 ADC (1 MS/s)		GPU/CPU
Microwave	RF/Microwave Back End	~100 ADC(1 GS/s) ~100 ADC (10 MS/s)	FPGA / CPU (Teraflop computing)	GPU/CPU
(Langmuir) Probes	Preamplifier	~300 ADC (1 MS/s)	CPU	GPU/CPU
Integration System (Port Plugs)	Amplifier/Filter	~100 ADC (1 MS/s)	CPU	NA
Engineering Systems	Amplifier/Filter	~100 ADC (1 MS/s)	CPU	NA

First Estimate of ADC needs for Diagnostics



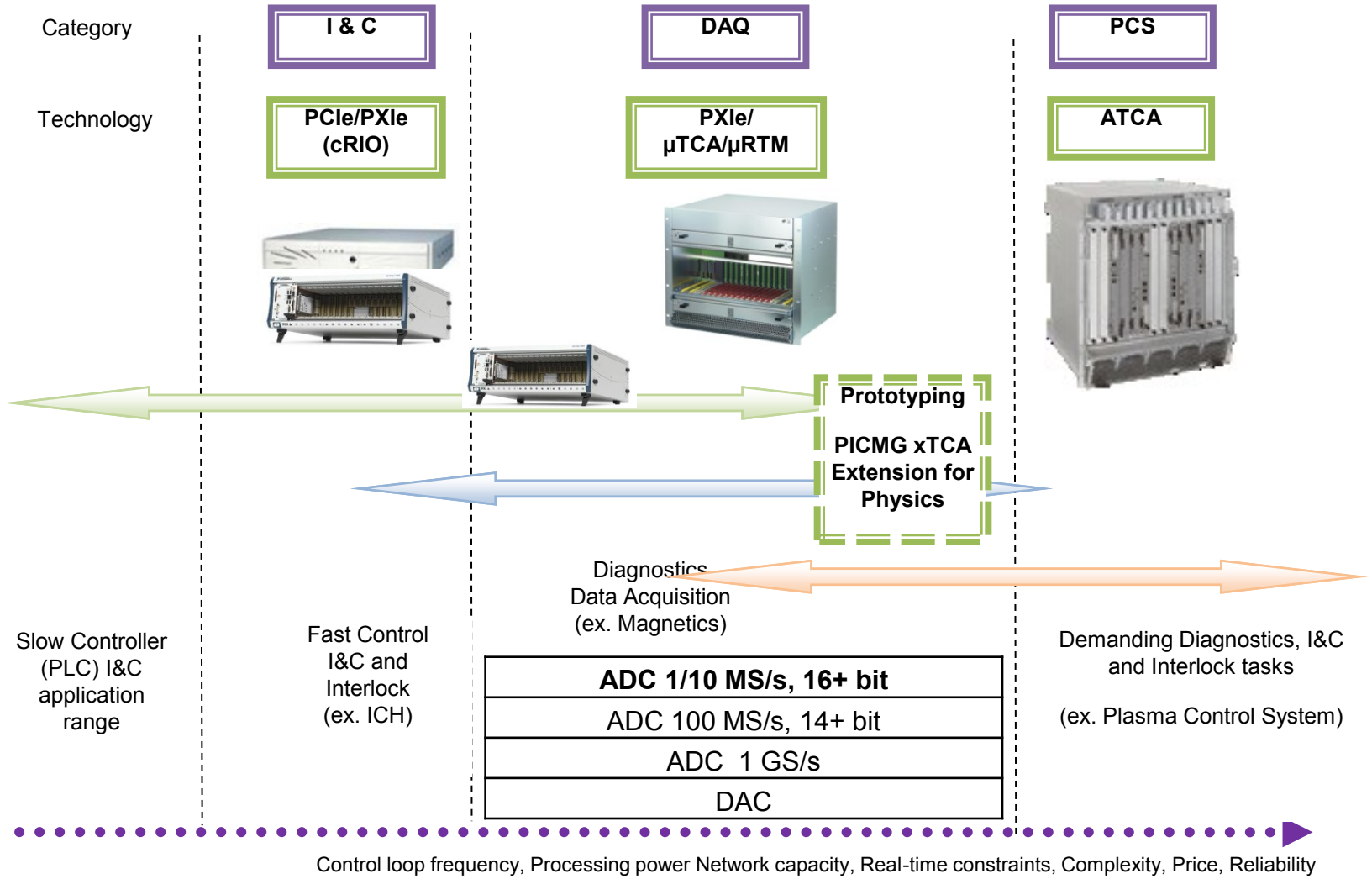
Objectives of Prototyping

1. Demonstrate design of integrated system with complete signal chain from data acquisition to archiving (limited features)
2. Products for fast controller catalog + CODAC Core System
3. Example system close to diagnostics needs which serves as basis for plant I&C development by domestic agencies.
4. Use prototype to execute FAT and SAT procedures and document issues with procedure.
5. Improve FAT and SAT procedures
6. Commissioning, operate and maintain prototype system
7. Add missing features to prototype system

Fast Controller Selection Criteria (in progress)

Fast Controller Formfactor →	PCIe/PXIe	µTCA/µRTM	ATCA
General features / functionality :			
Timing (timing receiver (clock and trigger) / distribution / hardware time stamping)			
Applicable to instrumentation			
Signal conditioning support			
High Availability (up to 99.99 %)			
Magnetic field environment (5 mT and up to 150 mT)			
Radiation (up to 10e5 n / cm**2 / sec)			
EMI shielding / EMC compatibility			
Shelf management			
Health management support (complete system)			
Scalability (IO channels and processing power)			
Modularity (IO, signal processing, comm. links etc.)			
Hardware:			
Analog IO : fast / medium / slow ADCs			
Camera Interface: Camera Link / GbE			
Signal Processing: FPGA / GPU / CPU			
Network : PON / SDN / TCN			
Software:			
EPICS driver (library)			
Linux system driver			
Application programming tools			
FPGA (Virtex 5 and 6)			
GPU (TESLA)			
IOC (CPU)			
Other:			
Cost			
Commercial availability (short / long-term)			

Roadmap


Category
I & C
DAQ
PCS
Technology
PCIe/PXIe (cRIO)
PXIe/ µTCA/µRTM
ATCA
Prototyping
PICMG xTCA Extension for Physics
Diagnostics Data Acquisition (ex. Magnetics)
Slow Controller (PLC) I&C application range
Fast Control I&C and Interlock (ex. ICH)
ADC 1/10 MS/s, 16+ bit
ADC 100 MS/s, 14+ bit
ADC 1 GS/s
DAC
Demanding Diagnostics, I&C and Interlock tasks
(ex. Plasma Control System)
Control loop frequency, Processing power Network capacity, Real-time constraints, Complexity, Price, Reliability

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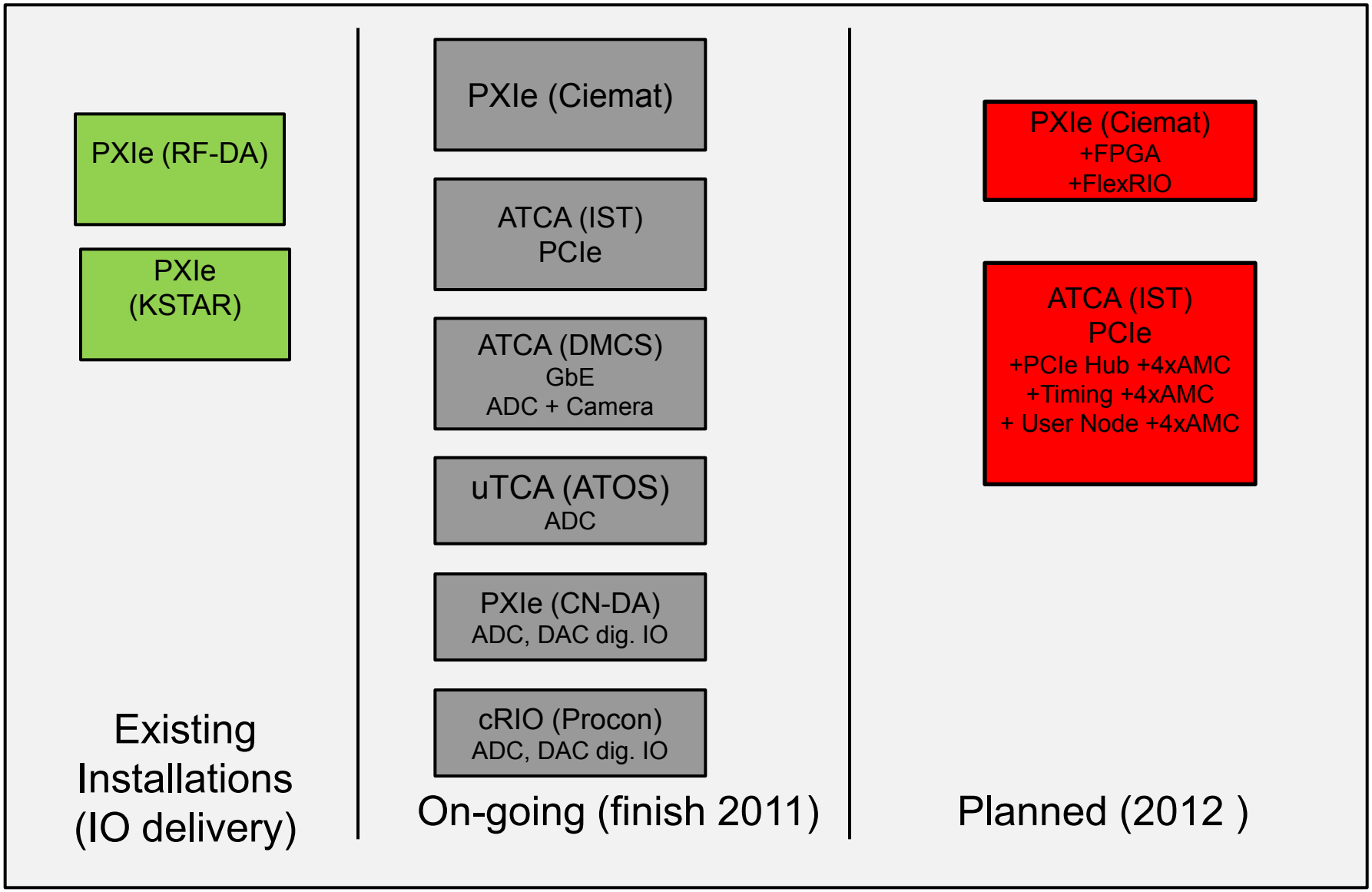
R&D Programs (Prototyping)



Products Expected from Prototyping

- **Complete example systems close to plant system needs**
  - To be included in CODAC core system
- **Hardware in fast controller catalog**
  - Chassis/shelf (including health monitoring)
  - Boards (ADC, Camera Interface, Timing receiver, Carrier boards)
  - Network Interfaces
- **Software**
  - Linux drivers for boards in fast controller catalog
  - EPICS device support for boards in fast controller catalog
  - Prototype examples included in CODAC core system (Application software, configuration data (SDD), HMI (Boys screens)
  - Source code in SVN
- **Documention in IDM**
  - Cubicle installation and wiring, thermal and fire load studies
  - User and developer manuals
  - Other design documents
  - FAT and SAT reports

General features evaluated in fast controller R&D

General Features	PX 01	PX 02	PX 03	AT 01	AT 02	AT 03	AT 04	uT 01	uT 02
Timing (TCN)	Y	Y	Y	N	N	N	Y	N	Y
Real-time networks (SDN)	N	N	N	N	N	N	N	N	N
Chassis health monitoring	N	N	N	Y	Y	Y	Y	Y	Y
System health monitoring	Y	Y	Y	Y	Y	Y	Y	Y	Y
Radiation tolerance	N	N	Y	N	N	N	Y	N	Y
Magnetic field tolerance	N	N	Y	N	N	N	Y	N	Y
EMC compatibility / EMI shielding	Y	Y	Y	Y	Y	Y	Y	Y	Y
Scalability	Y	Y	Y	Y	Y	Y	Y	Y	Y
Modularity	Y	Y	Y	Y	Y	Y	Y	Y	Y
Availability	N	N	N	N	N	Y	Y	N	Y
Hot-Swap	N	N	N	Y	Y	Y	Y	N	Y
Signal Condition in chassis	N	Y	Y	Y	Y	Y	Y	Y	Y
Rear Cabling for signals	N	N	N	N	N	Y	Y	N	Y
Installation in Standard SAREL Cubicle	Y	Y	Y	Y	Y	Y	Y	Y	Y
Cubicle grounding	Y	Y	Y	N	Y	Y	Y	Y	Y

Hardware components evaluated in fast controller R&D

Hardware Features	PX 01	PX 02	PX 03	AT 01	AT 02	AT 03	AT0 4	uT 01	uT 02
Timing Interface (IEEE-1588)	Y	Y	Y	N	N	Y	Y	N	Y
Timing distribution on backplane	N	N	N	N	N	Y	Y	N	Y
Remote PCIe I/O	Y	Y	Y	N	Y	N	Y	N	N
Network switch (1588 compatible)	Y	Y	Y	Y	Y	Y	Y	Y	Y
ADC 1/10 MS/s, 16+ bit	Y	N	N	N	N	N	N	N	N
ADC 100 MS/s, 14+ bit	N	Y	N	Y	Y	Y	Y	Y	N
ADC 1 GS/s	N	N	N	N	N	N	Y	N	Y
DAC	Y	Y	Y	Y	Y	Y	Y	Y	Y
Digital I/O	Y	Y	Y	Y	Y	Y	Y	Y	Y
Camera Interface	N	N	Y	N	N	Y	N	N	Y
RTM (PCIe and/or GbE)	n/a	n/a	n/a	Y	Y	Y	Y	n/a	n/a
uRTM (signal conditioning)	n/a	n/a	n/a	n/a	n/a	n/a	n/a	N	Y
PCIe on carrier	n/a	n/a	n/a	N	Y	Y	Y	Y	Y
PCIe on backplane	Y	Y	Y	Y	Y	Y	Y	Y	Y
PCIe on external	Y	Y	Y	Y	Y	Y	Y	Y	Y
GbE on carrier	N	N	N	Y	Y	Y	Y	Y	Y
1/10 GbE on backplane	N	N	N	10	10	10	10	10	10
1/10GbE on external	1	1	1	10	10	10	10	10	10
Chassis/Shelf	C	C	C	S	S	S	S	C	C
Cubicle wiring	Y	Y	Y	Y	Y	Y	Y	Y	Y
Patch Panels and termination blocks	Y	Y	Y	Y	Y	Y	Y	Y	Y
Cubicle forced air cooling	Y	Y	Y	Y	Y	Y	Y	Y	Y
Cubicle health monitoring	Y	Y	Y	Y	Y	Y	Y	Y	Y

Software components studied in fast controller R&D

Software Features	PX 01	PX 02	PX 03	AT 01	AT 02	AT 03	AT 04	uT 01	uT 02
Mini-CODAC	N	N	N	N	N	N	N	N	N
CODAC core system V2	Y	Y	Y	Y	Y	Y	Y	Y	Y
Red Hat Linux 5.5	Y	Y	Y	Y	Y	Y	Y	Y	Y
MRG Real time extension	N	N	N	N	N	Y	Y	N	Y
MARTe (real time framwork)	N	N	N	N	Y	N	Y	N	N
Hardware time stamp readout	Y	Y	Y	N	N	Y	Y	N	Y
EPICS time stamp	Y	Y	Y	Y	Y	Y	Y	Y	Y
Data quality flag	N	N	N	N	N	Y	Y	N	Y
Linux drivers	Y	Y	Y	Y	Y	Y	Y	Y	Y
EPICS device supports	Y	Y	Y	Y	Y	Y	Y	Y	Y
FPGA applications	N	Y	Y	Y	Y	Y	Y	Y	Y
GPU applications	N	N	N	Y	N	Y	Y	N	Y
CPU applications	Y	Y	Y	Y	Y	Y	Y	Y	Y
Hot-swap	N	N	N	Y	Y	Y	Y	N	Y
Self-description (SDD)	Y	Y	Y	Y	Y	Y	Y	Y	Y
FPGA programming tools	N	LV	LV	Xi	Xi	Xi	Xi	ML	ML
CODAC system integration	Y	Y	Y	Y	Y	Y	Y	Y	Y
Scientific Data Archiving	N	Y	Y	Y	Y	Y	Y	Y	Y
Data acquisition	N	Y	Y	Y	Y	Y	Y	Y	Y
Signal Processing	N	Y	Y	Y	Y	Y	Y	Y	Y