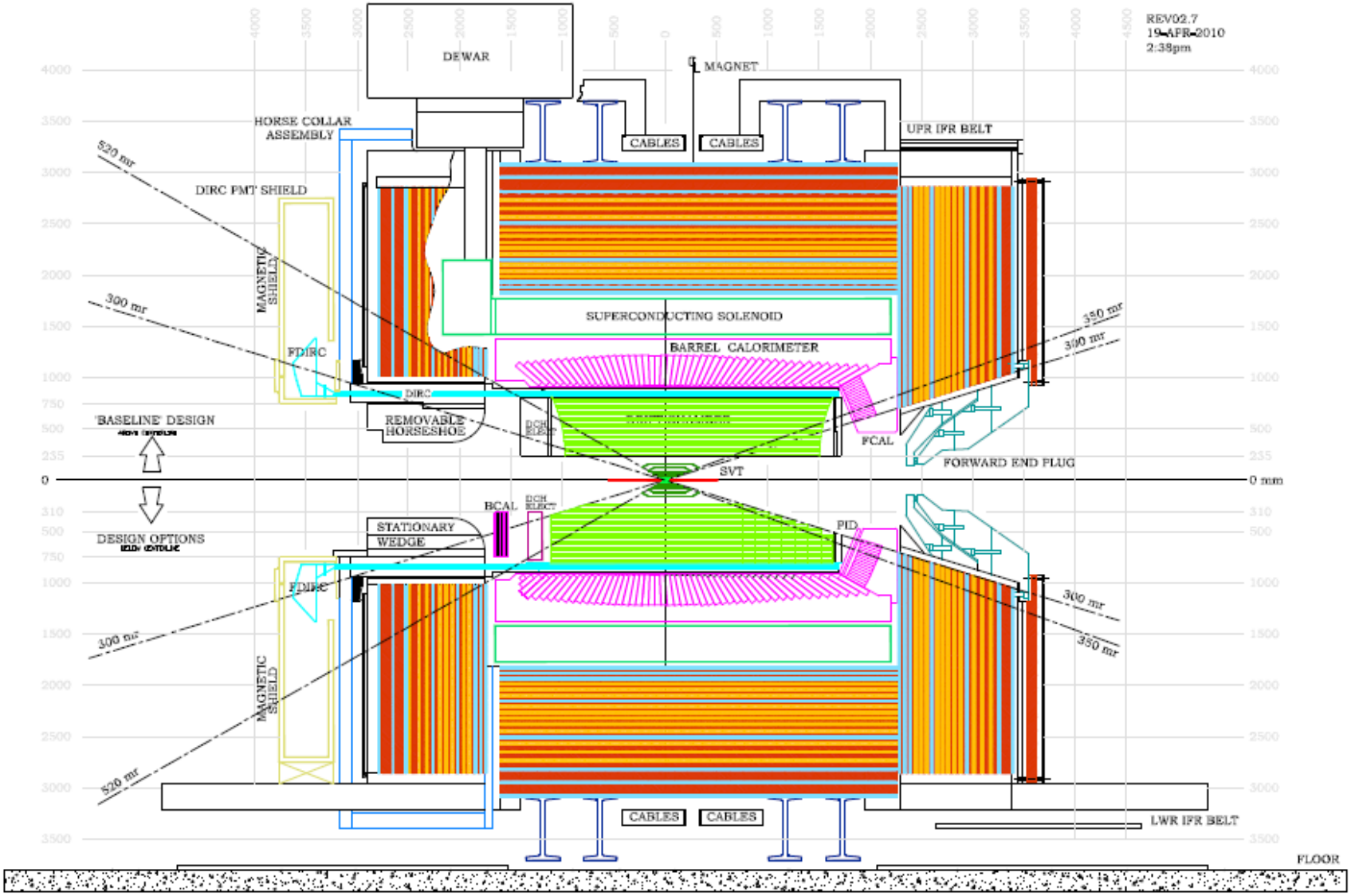
XTCA for SuperB project

- FTCS
- ECS

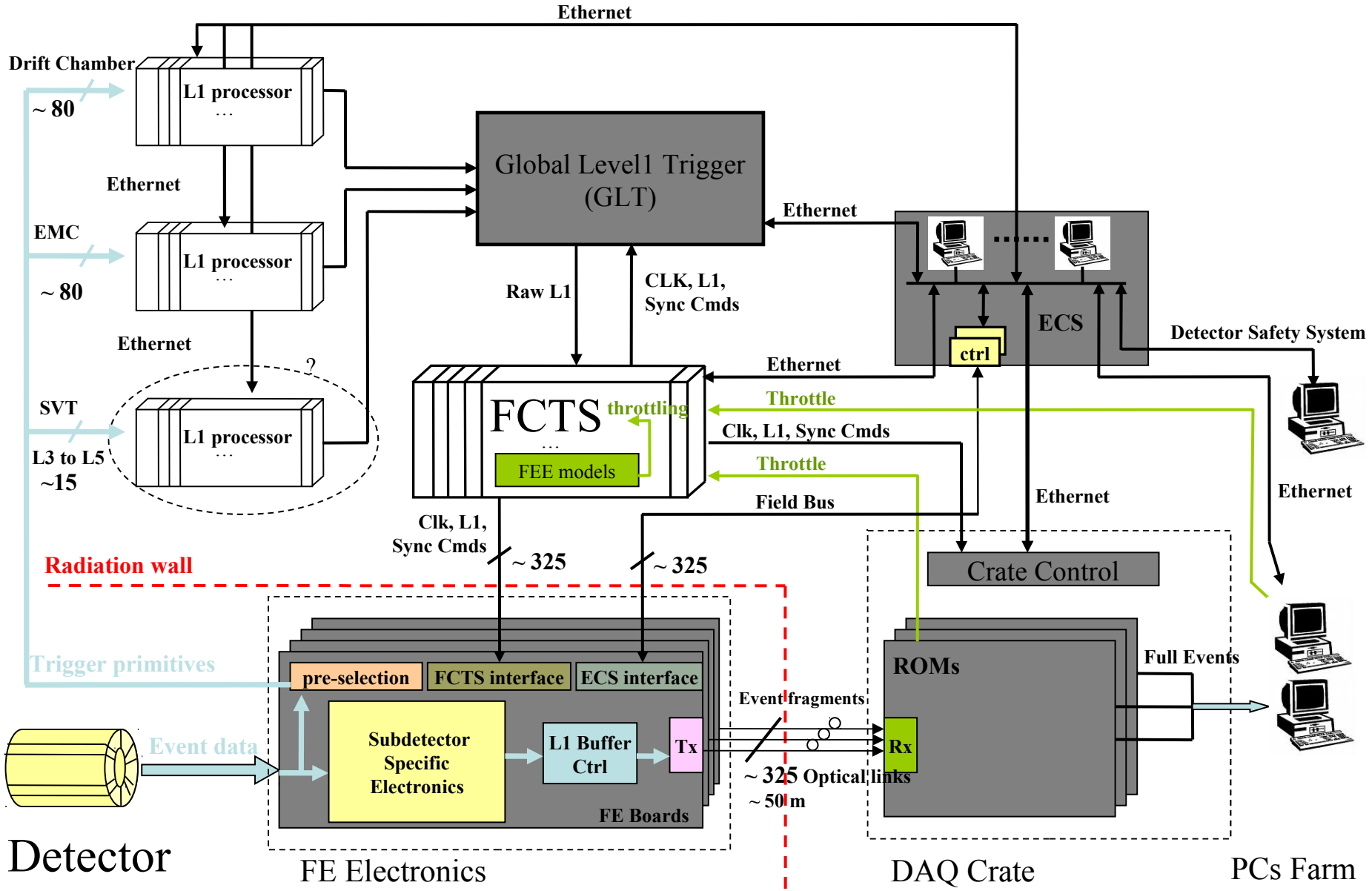
SuperB detector



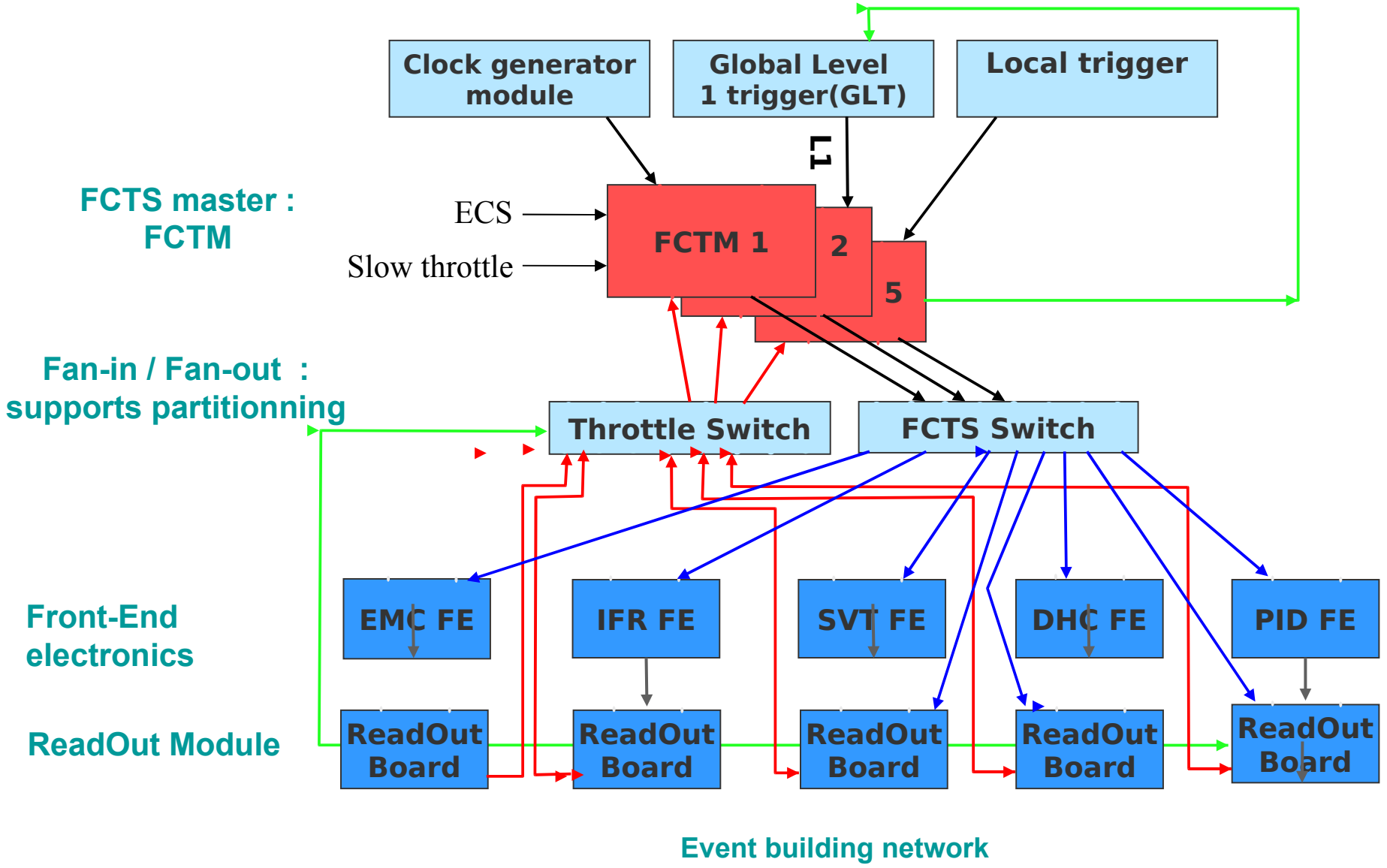
FCTS requirements

- Synchronizing the experiment with the machine.
- Delivering and buffering the clock to the experiment.
- Dealing with the raw L1 trigger decision.
- Throttling the latter.
- Permits the partitioning the system into independent subsystems or groups of subsystems.
- Generating programmable local trigger for calibration and commissioning.
- Generating different commands (calibration pulse, reset, BxID and event ID).
- Managing the stack of IP addresses for PC farm.
- Keeping trace of all event-linked data to put in the event readout

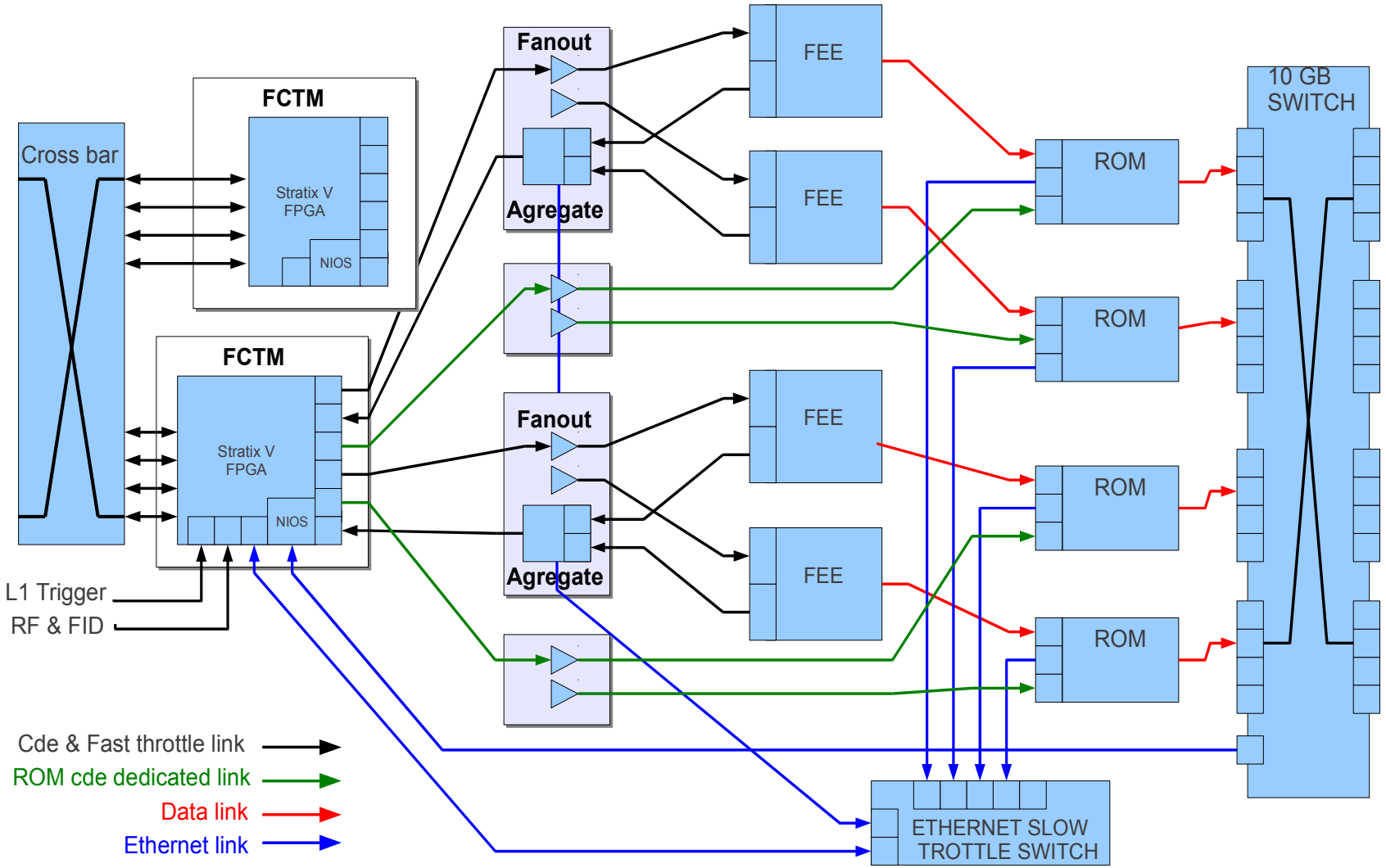
Overall system achitecture



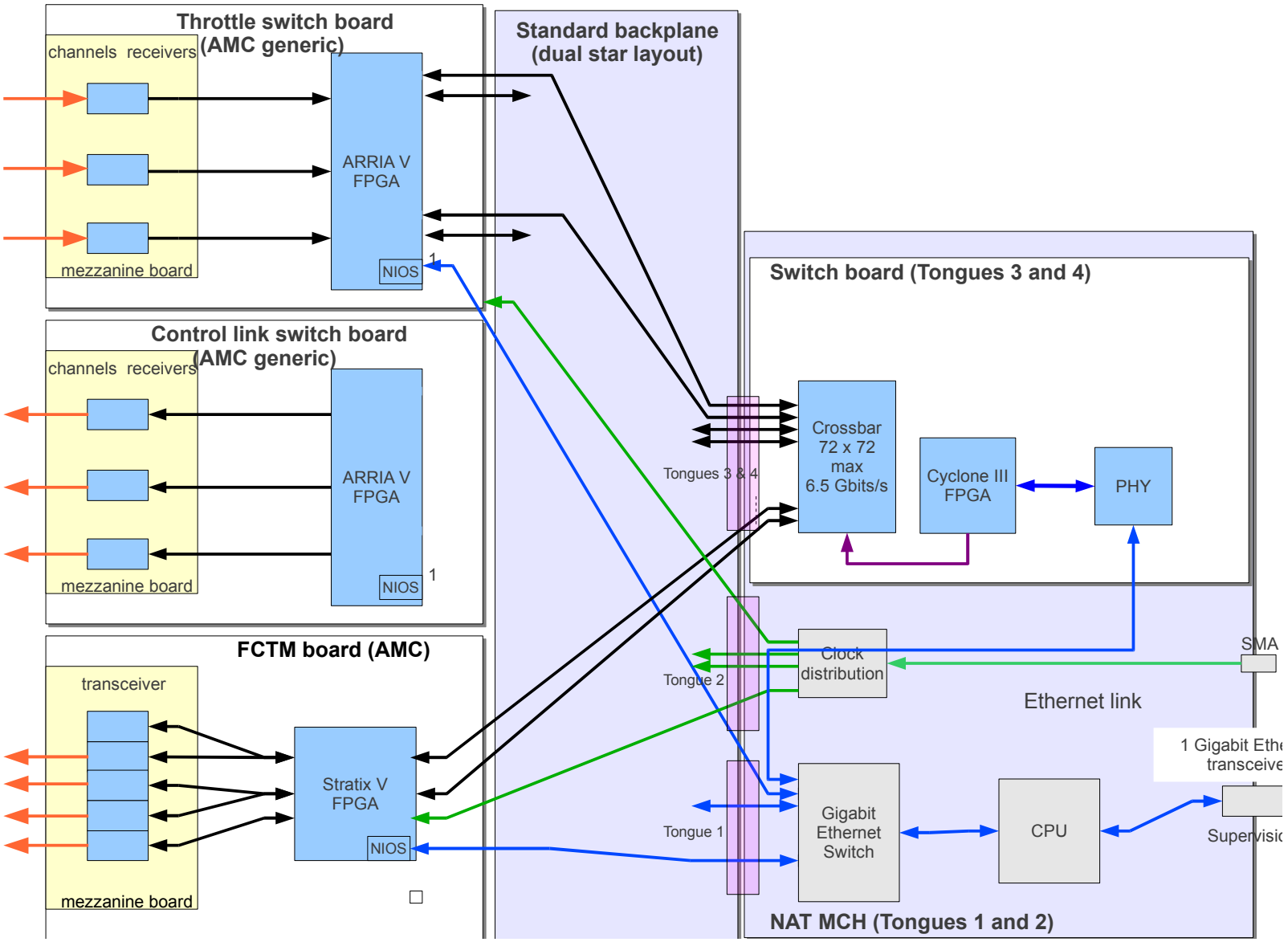
FCTS Architecture



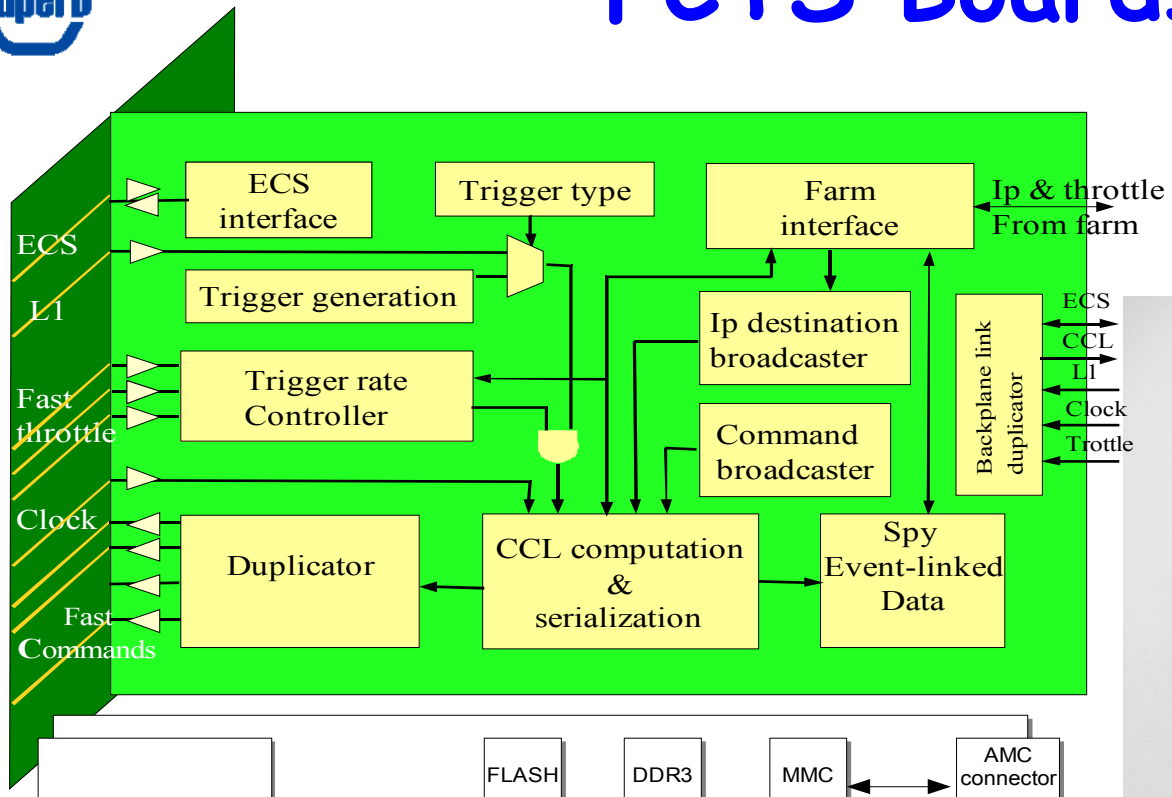
FCTS architecture push concept

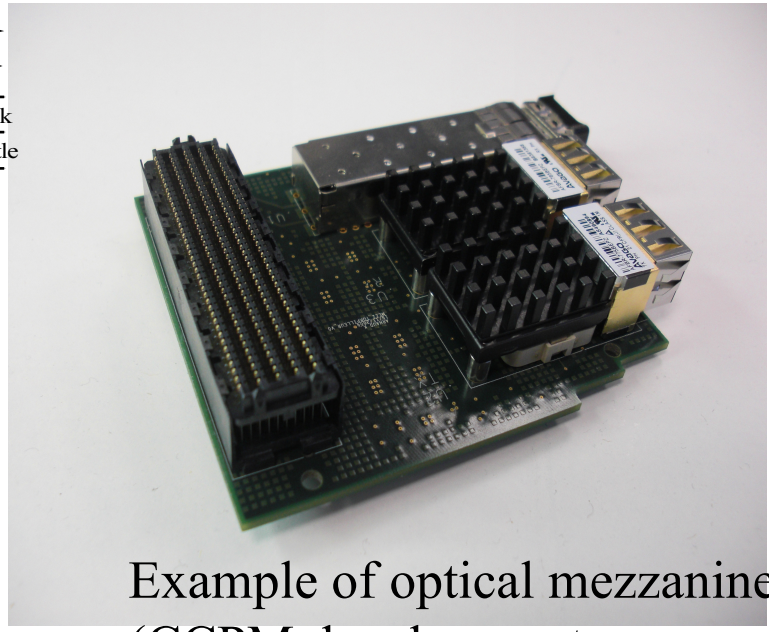


FCTS xTCA architecture

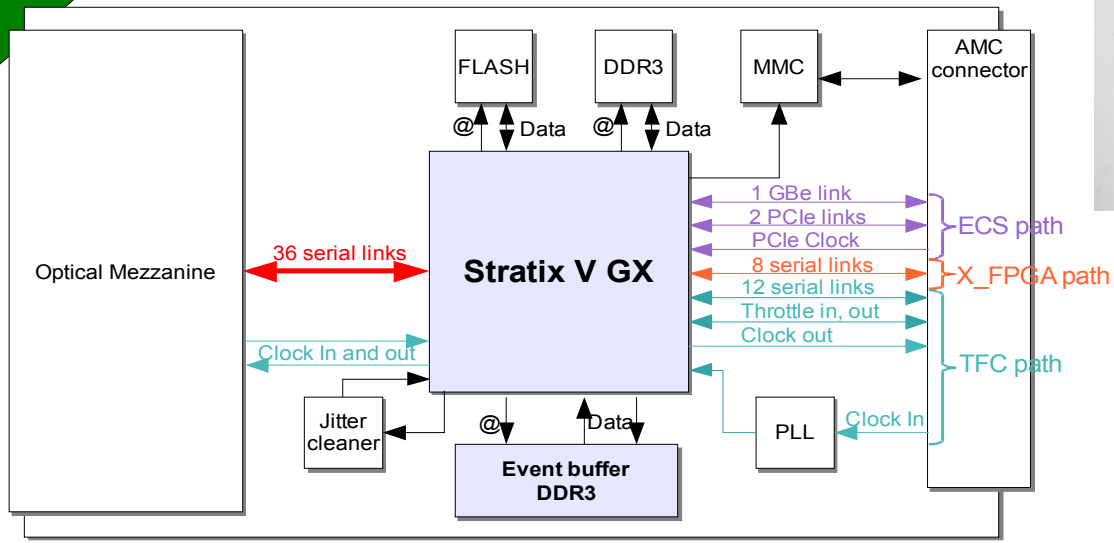


FCTS Boards



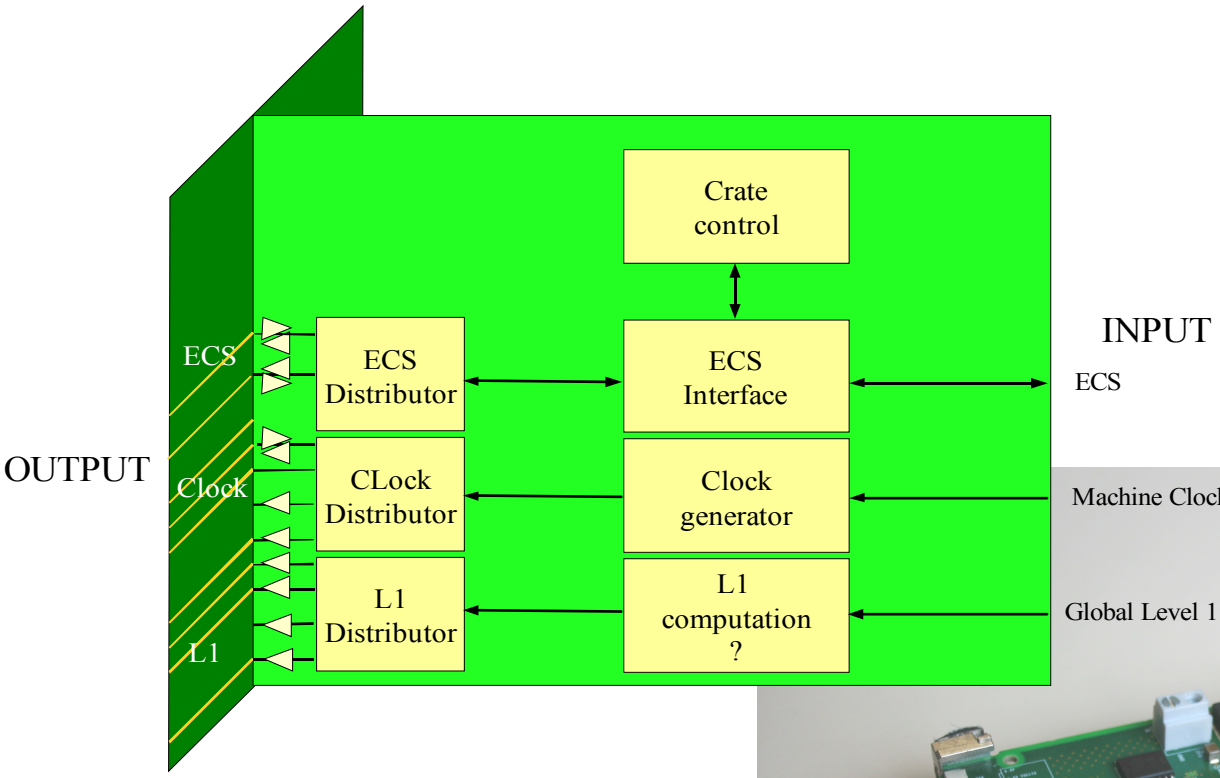


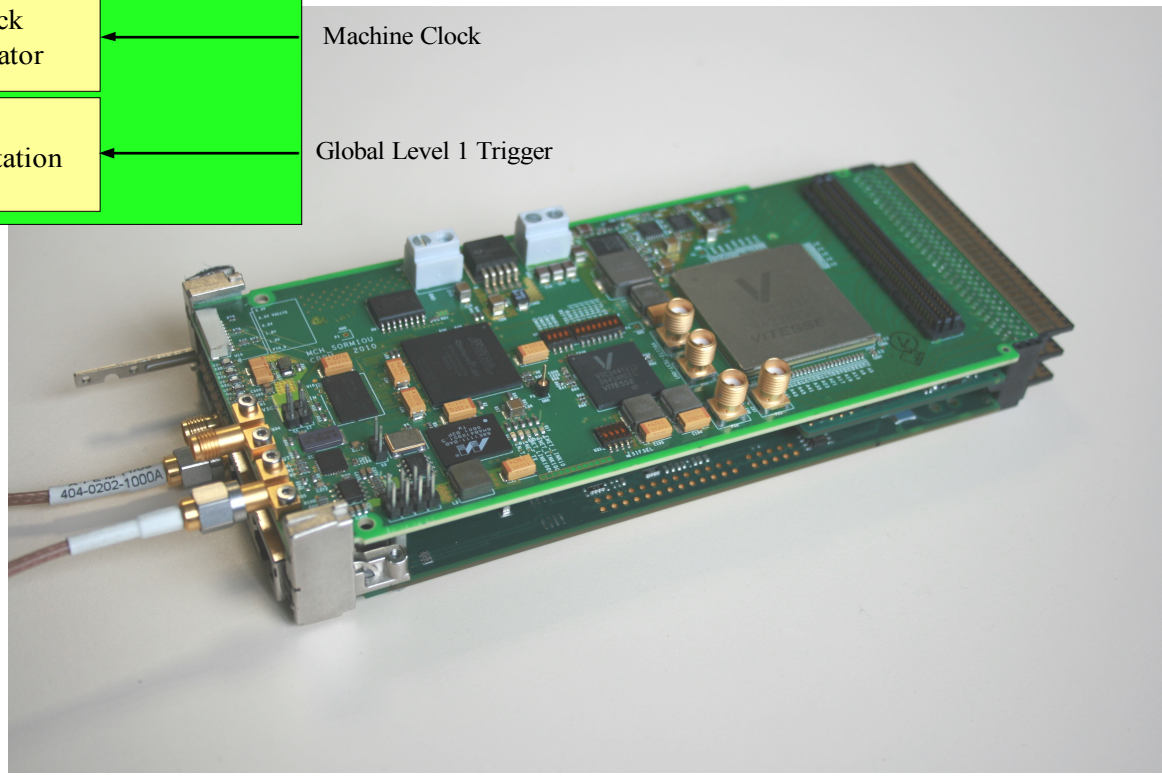
Example of optical mezzanine (CCPM development



AMC mezzanine board (CCPM development)

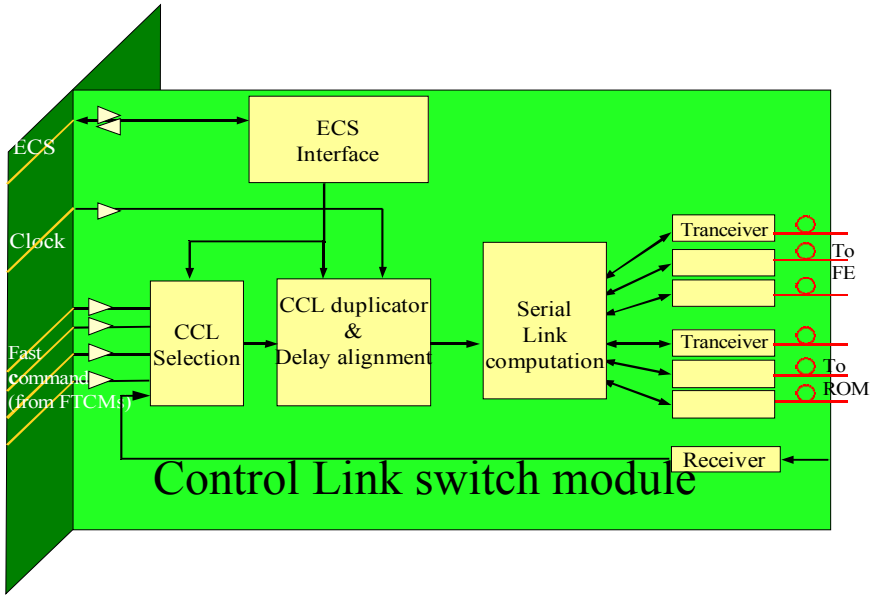
Control & distribution module

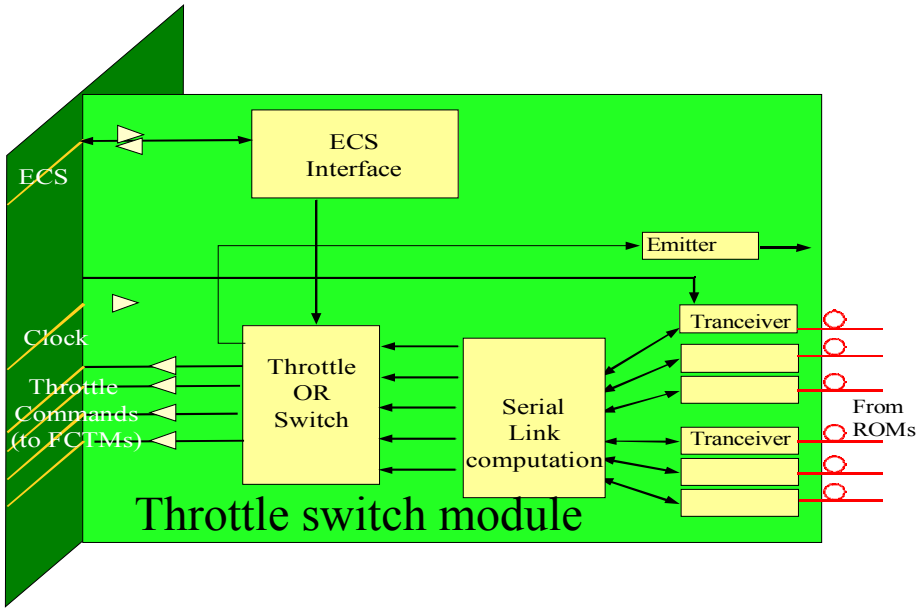


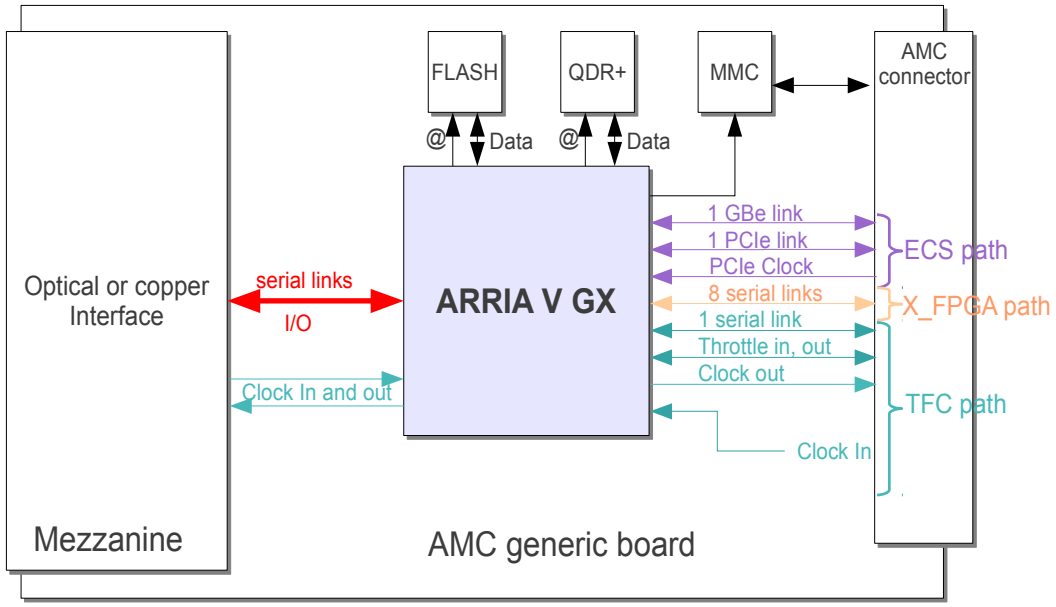


Tong 1: On the shelf industrial board.
Tong 2 : CCPM board

Distribution & trottle





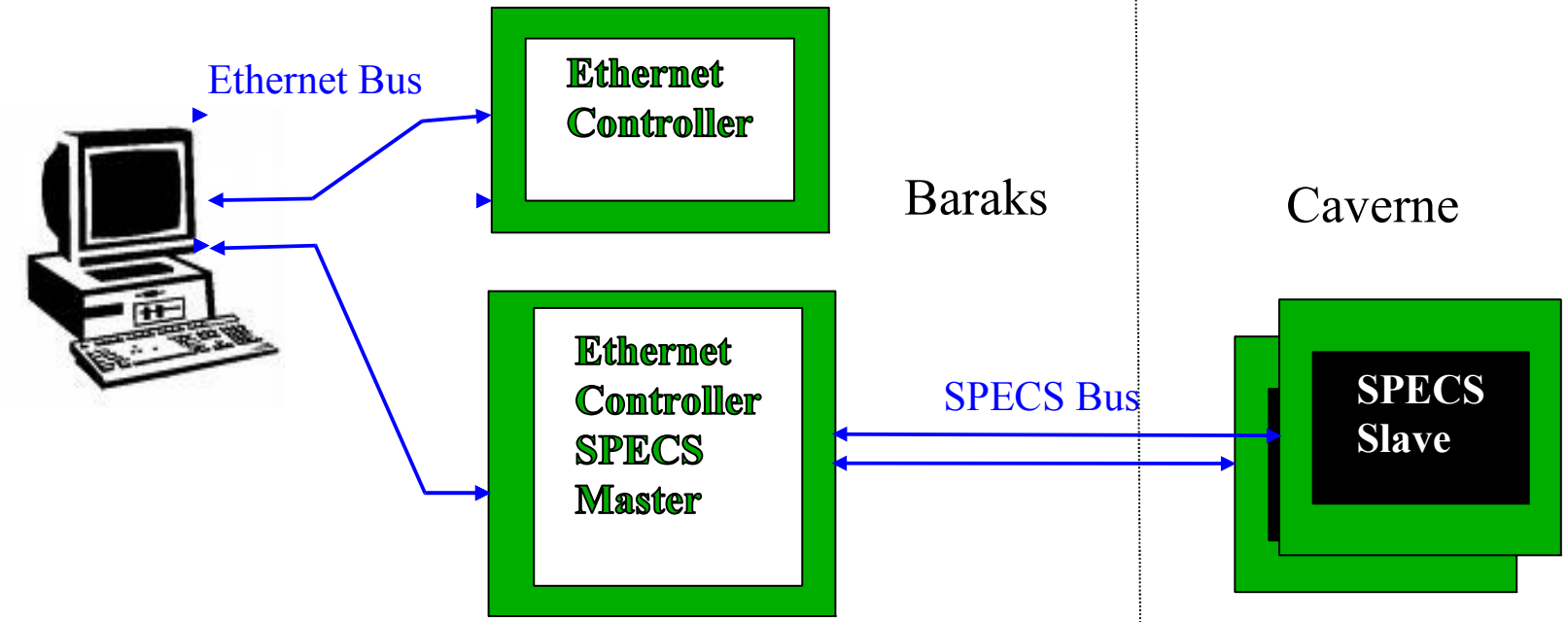


Open questions for FCTS

- FPGA transceiver latency.
- DS92Lv018 FPGA emulation.
- Fast throttle link (links type, number, location,...).
- Slow throttle latency (Ethernet UDP).
- 2 Clocks (CCPM MCH mezzanine manage one)
- FCTS crate form factor ATCA or ATCA for physics (due to the link number)
  - CCPM AMC and MSC mezzanine.

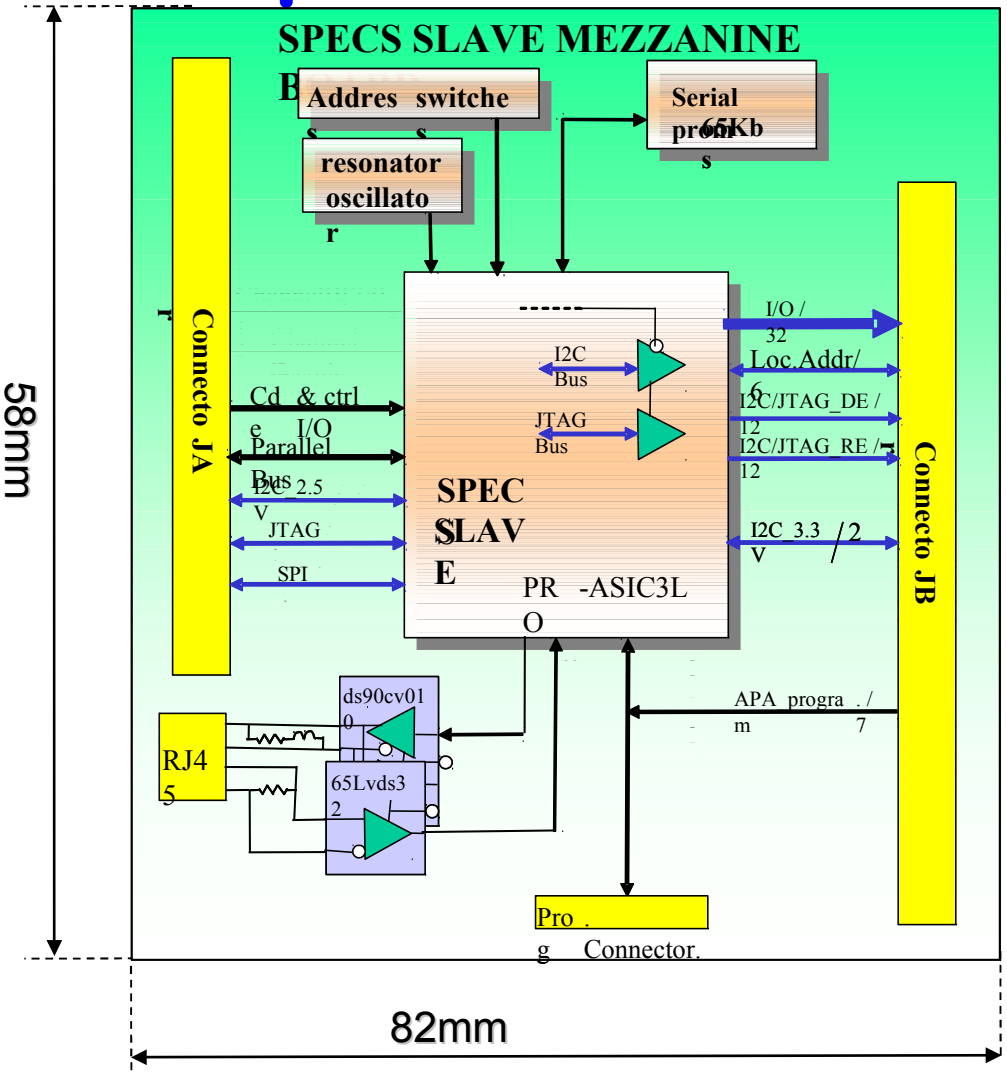
ECS requirement

- Configuration system for individual boards located on the detector or crate located in the cavern.
  - Located in radiation sensitive environment, up to 20KRad.
  - Long distance link, up to 130m.
  - Multi configuration (multi-drop bus, point to point).
  - Multi standard interfaces (JTAG, I2C, parallel bus, ctrl I/O).



A Serial Protocol for Experiment Control System SPECS

SuperB SPECS slave implementation



FPGA ProASIC3L from ACTEL.
Triple voting register.

Transfer rate: ~ 14Mbits/s

Address: Local address switch.
Broadcast address capability.

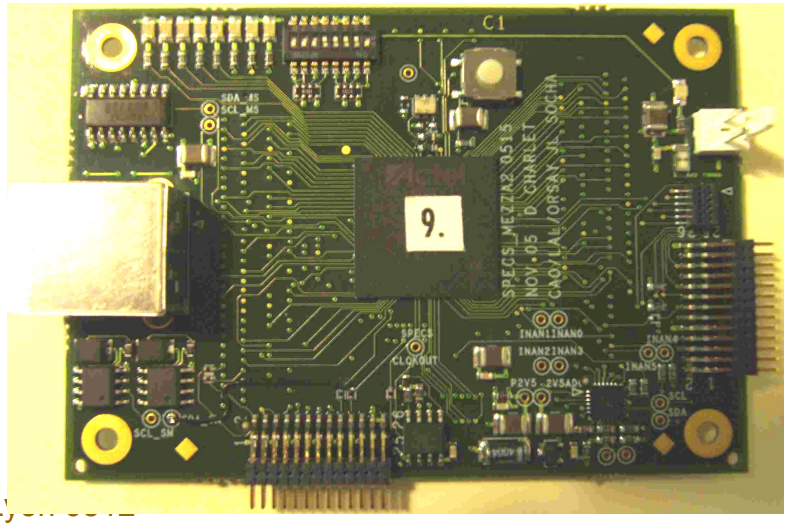
On board clock: Crystal resonator

Programmable clock for SPECS read back:

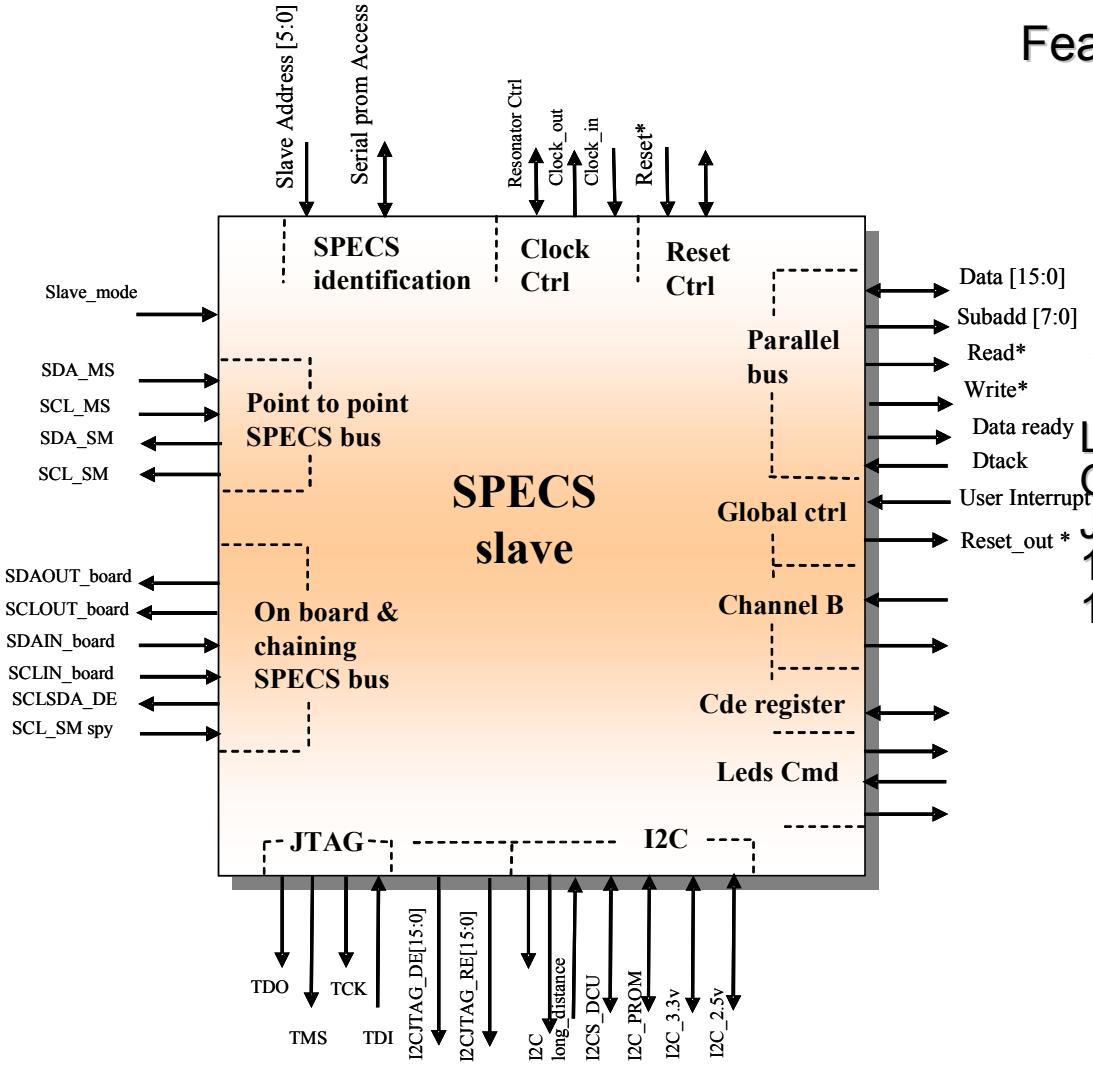
Long distance capability: 120m cat6 cable

User Serial EEPROM: 65Kbits capacity

JTAG bus, I2C bus, SPI Bus



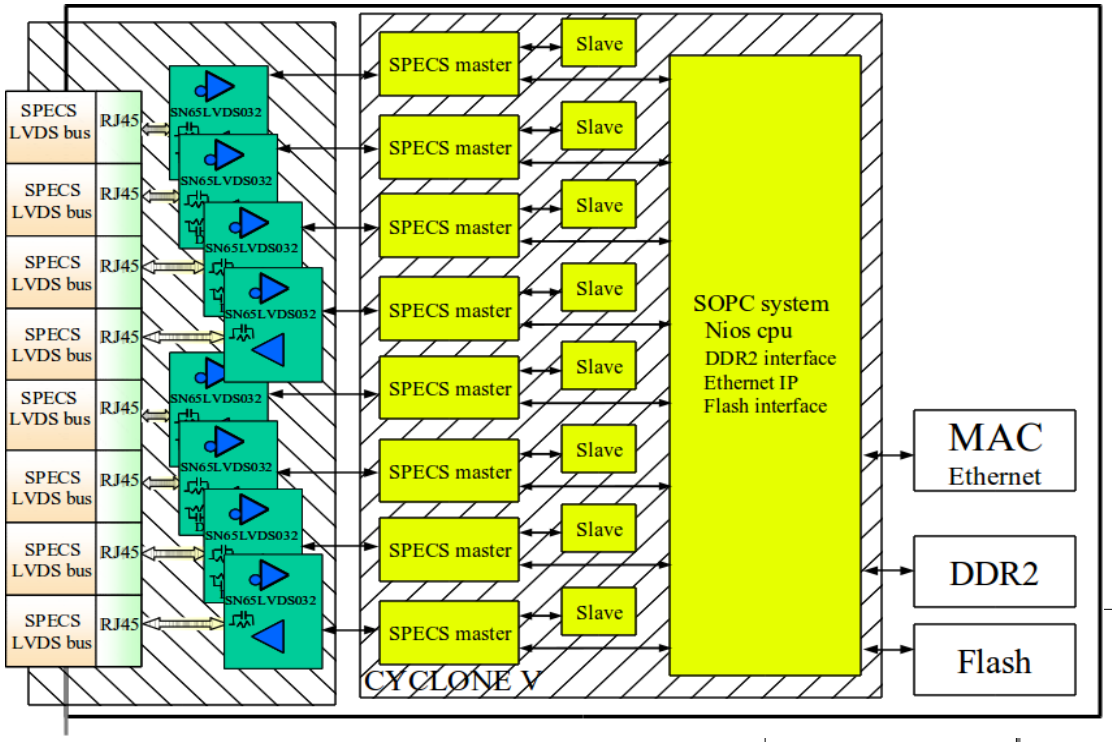
SPECS slave functions

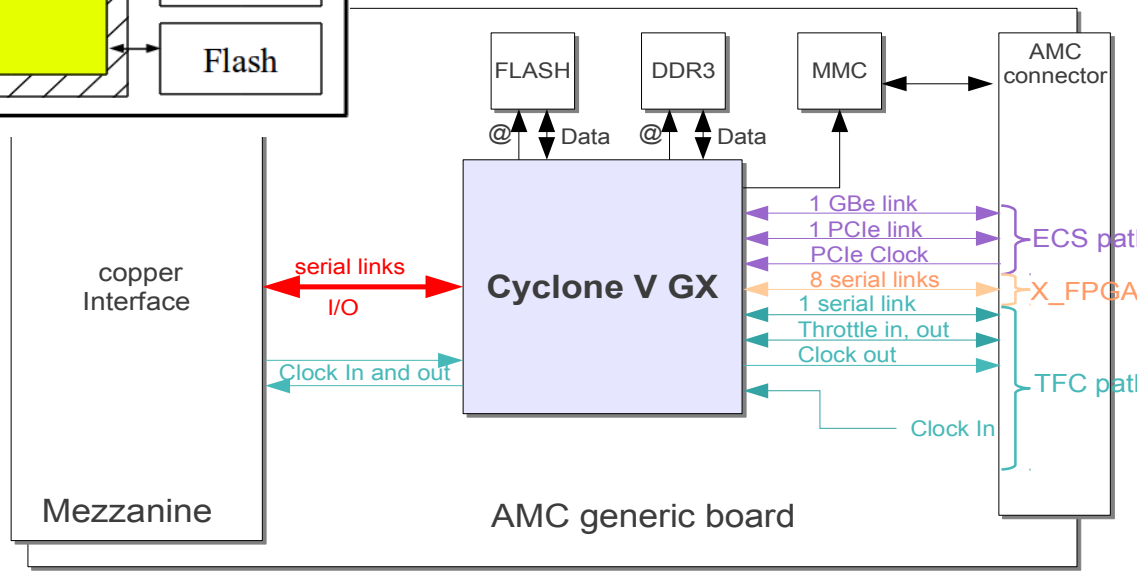


Features of slave:

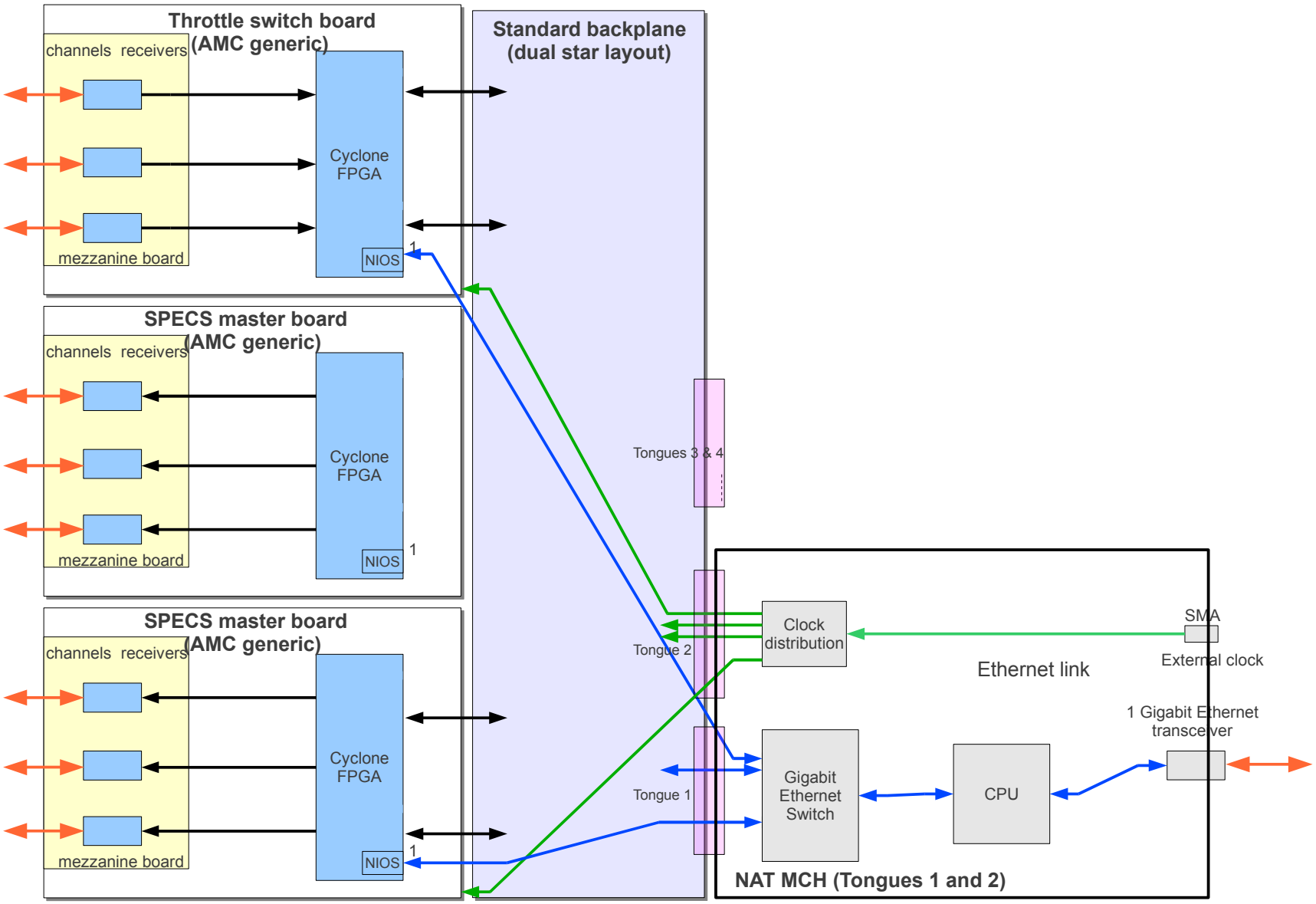
- SPECS bus:
  Point to point slave interface
  Multi drop
- Parallel interface:
  Parallel bus (16data, 8address)
  32 configurable I/O lines
- Serial interface:
  Long distance I2C bus
  On board I2C bus
  JTAG bus
  12 receiver enable
  12 driver enable
- Interrupt:
  User interrupt
  Transmission error
- Serial EEPROM interface:
  Identification register
  Users register

Ethernet SPECS master





ECS xTCA architecture



Open questions for ECS

- Data transport: Ethernet/PCIExpress