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# Challenges for Emerging New Electronics Standards for Physics

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For the xTCA for Physics Lab-Industry Collaboration

# PICMG-ese

Term	Definition
PICMG	PCI Industrial Computer Manufacturers Group, 250 corporations
ATCA	Advanced Telecommunications Computing Architecture large board
Carrier	ATCA or $\mu$ TCA board that supports smaller standard board
Shelf	Crate, ATCA (large) or $\mu$ TCA (small)
RTM/ $\mu$ RTM	Rear/Micro Rear Transition Module
AMC	Advanced Mezzanine Card mounting on ATCA Carrier, $\mu$ TCA shelf
Micro/ $\mu$ TCA	Crate designed to support AMCs directly
MCH	Micro-Controller Hub Switch module for $\mu$ TCA shelf
PU, CU	Power Unit (Module), Cooling Unit (fan or fan tray)
IPMI	Intelligent Platform Management Interface
Shelf Mgr	Shelf board hosting IPMI controller (BMC, MMC controllers)
Wide, High	High (vertical module height), Wide (front panel width)
xTCA	ACTA and /or MicroTCA standard platforms

# Outline

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- I. Introduction - New Standards Defined
- II. Goals & Status of New Physics Standards
- III. PICMG\* Lab-Industry Development Model
- IV. Conclusions
- V. Acknowledgments

- PCI Industrial Computer Manufacturers Group for open source standards, [www.picmg.com](http://www.picmg.com)

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# I. Introduction

## New Standards Defined

# Physics Extensions to PICMG Standards

## ***AdvancedTCA***<sup>®</sup>

PICMG<sup>®</sup> 3.8  
Draft RC1.0 for Revision 1.0

**AdvancedTCA Rear Transition Module  
Zone 3A**

26 July 2011



**Open Modular  
Computing Specifications**

## ***MicroTCA***<sup>™</sup>

PICMG<sup>®</sup> Specification MTCA.4  
R 1.0 Draft 0.9xi

**MicroTCA Enhancements for Rear I/O  
and  
Precision Timing**

18 July 2011



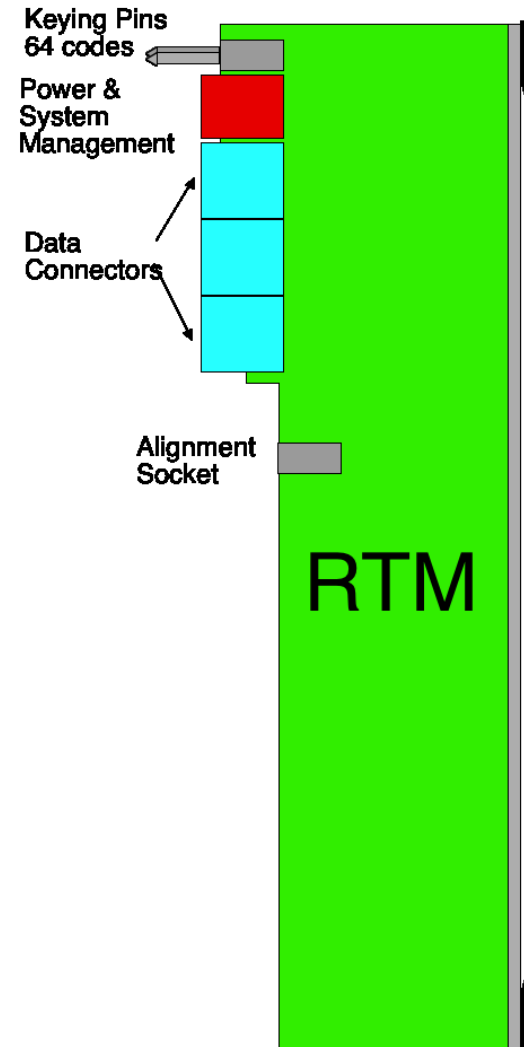
**Open Modular  
Computing Specifications**

***μTCA***<sup>®</sup>

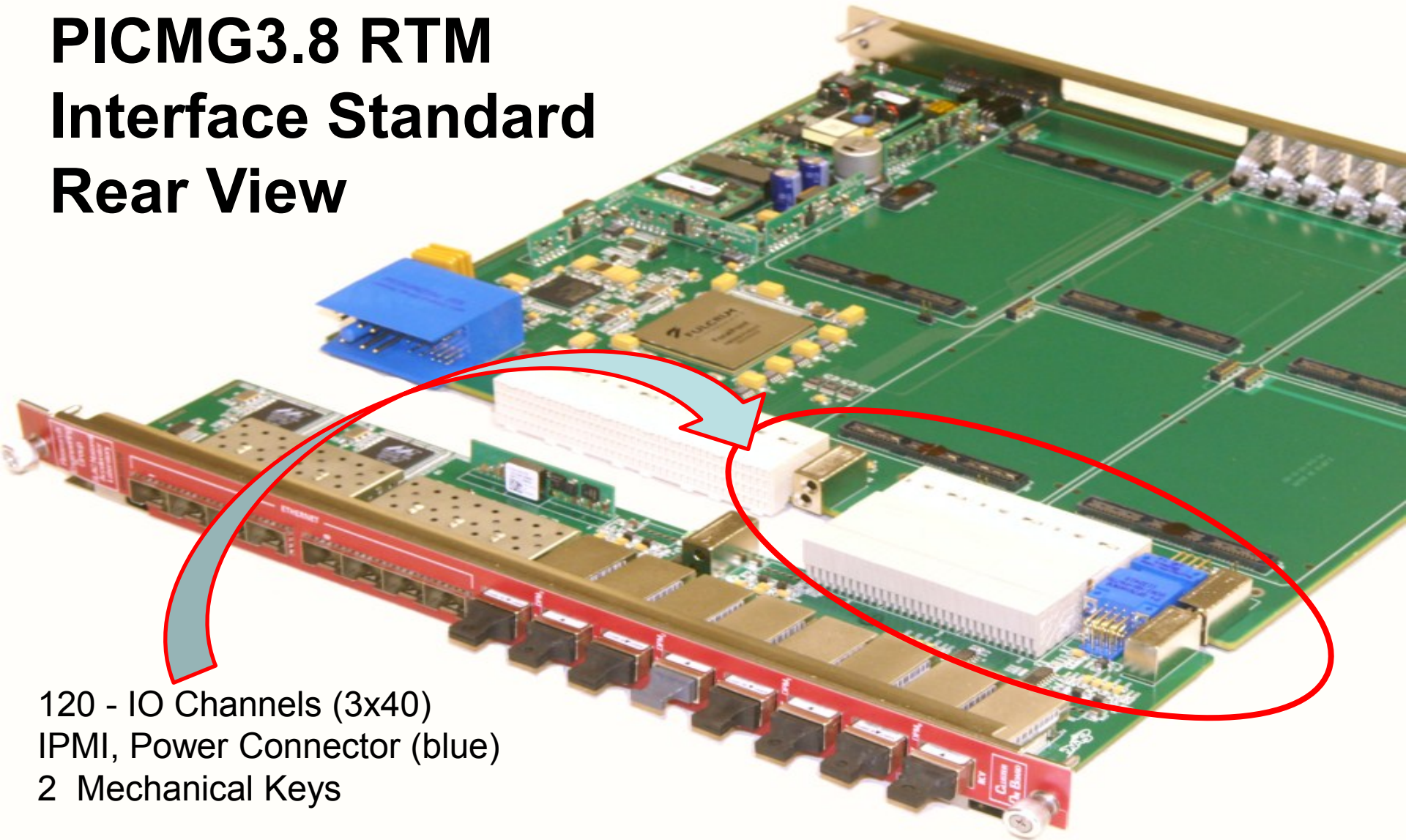
# PICMG3.8- Rear Transition Interface

## New Features for Physics:

- Alignment/Keying
- Power & System Management
- User I/O – ADF Connectors



# PICMG3.8 RTM Interface Standard Rear View



120 - IO Channels (3x40)  
IPMI, Power Connector (blue)  
2 Mechanical Keys

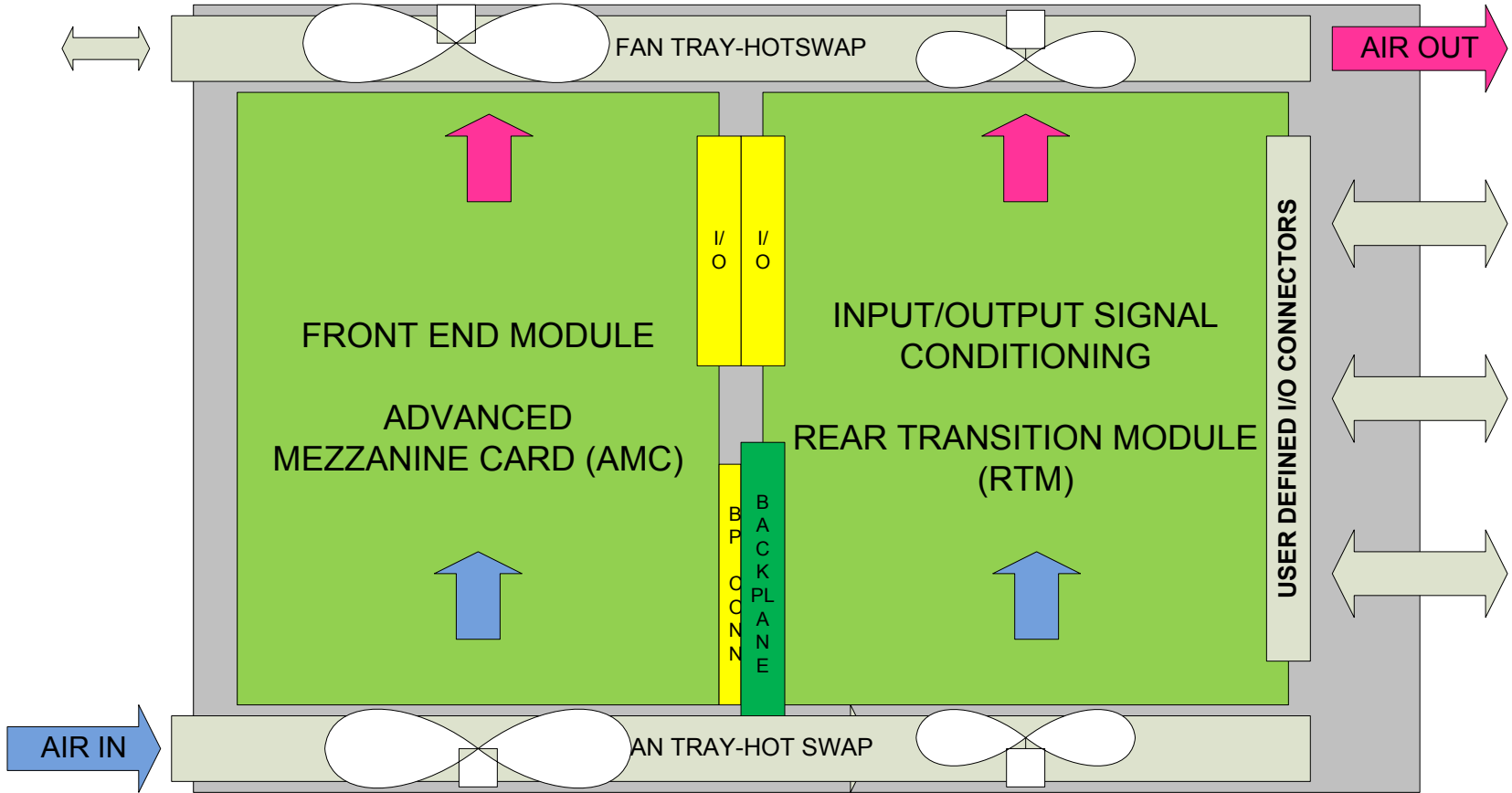
# MTCA.4 New Double-Wide Shelf, RTM

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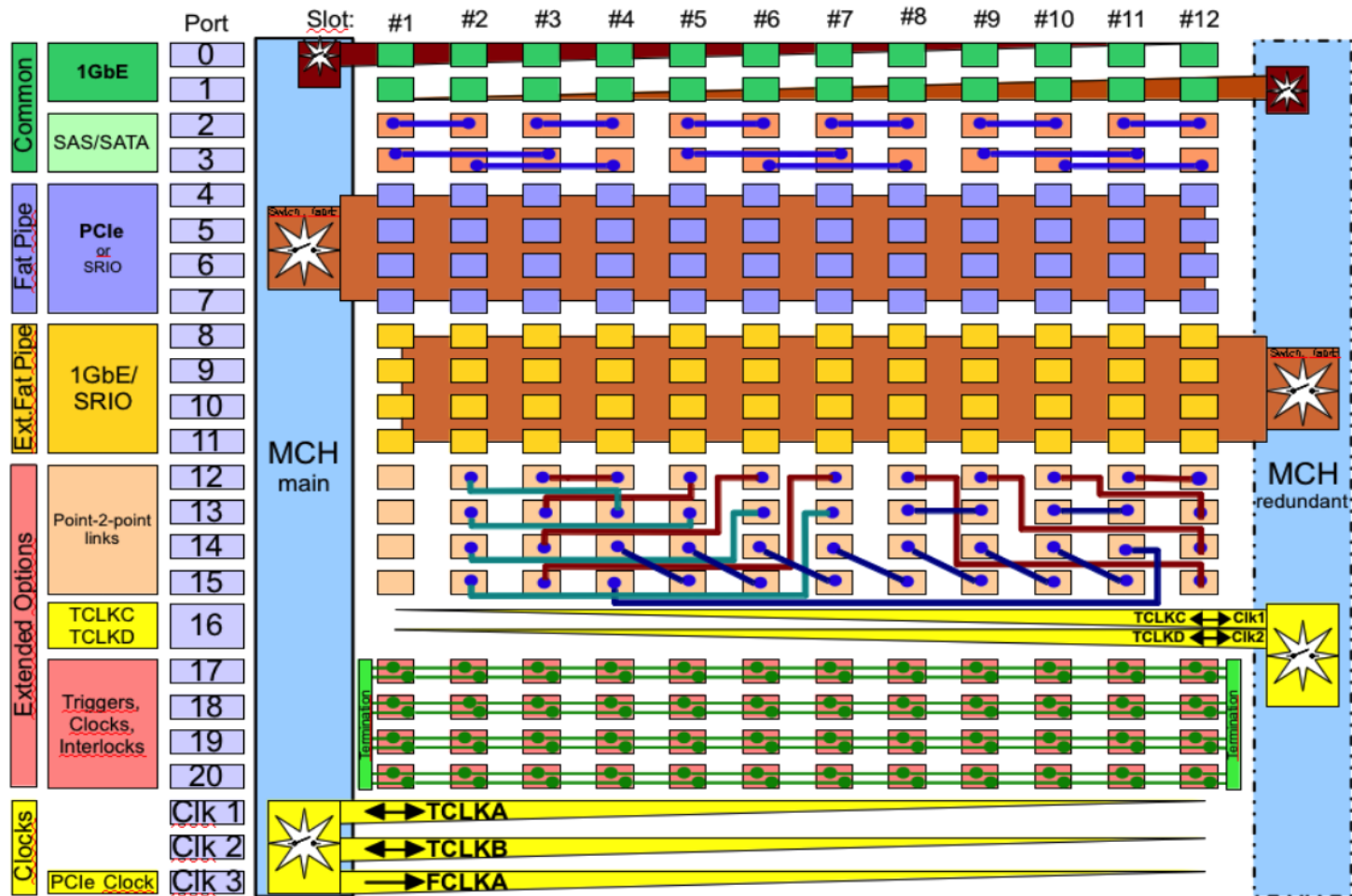
- PICMG double wide AMC had no RTM defined
  - Hot swappable AMCs deemed essential for next gen physics, hence added hot-swappable RTM
- Major backplane addition: Timing
  - New parallel backplane lines on one layer for triggering or interlocks; daisy chain lines for interlock chains, defined undesignated star lines for precision clocks



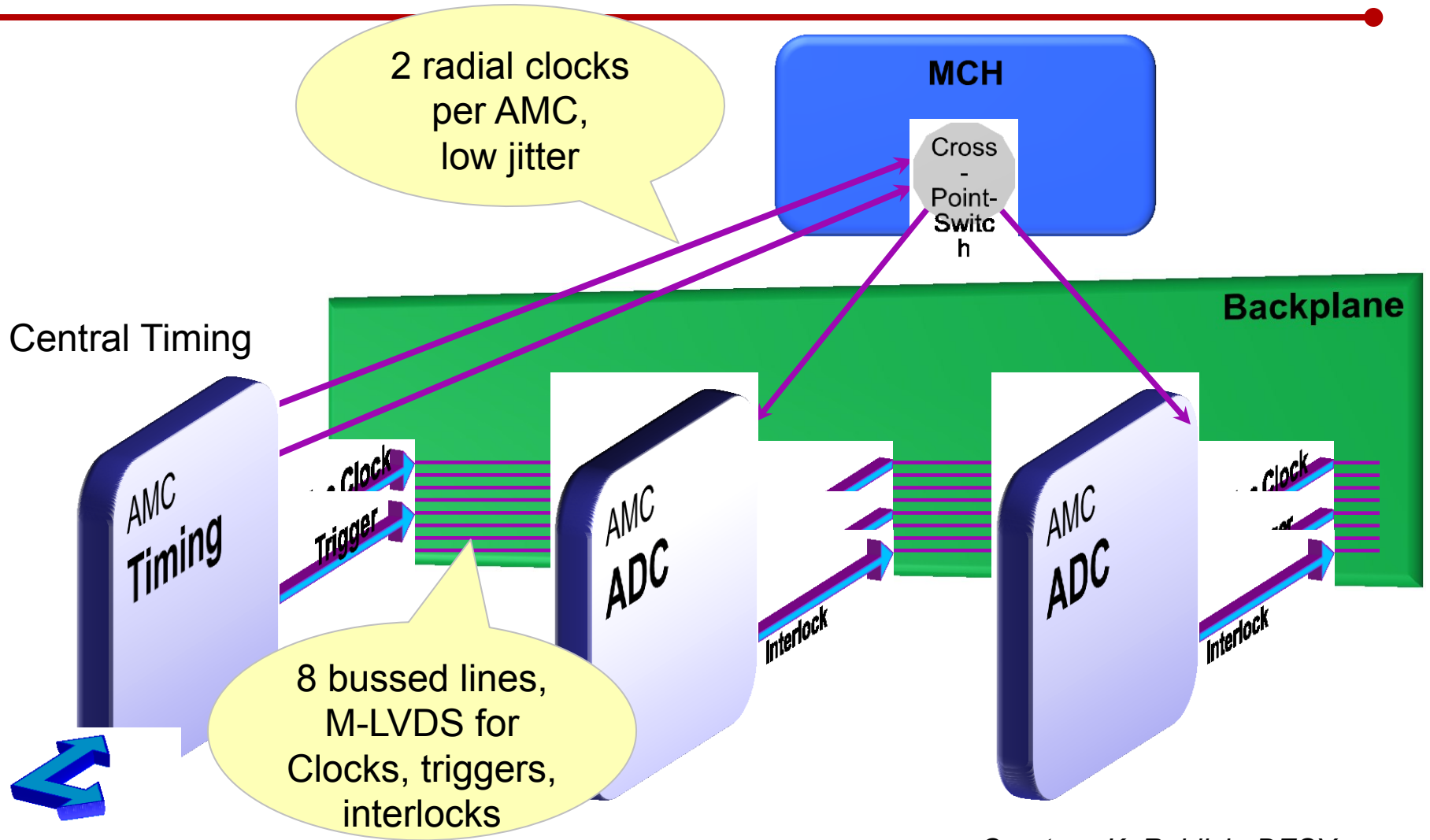
# MTCA.4 AMC-RTM-Shelf Concept



# MTCA.4 12-AMC Backplane



# MTCA.4 Backplane Timing Distribution



Courtesy K. Rehlich, DESY

# MTCA.4 Prototype Shelves & Modules

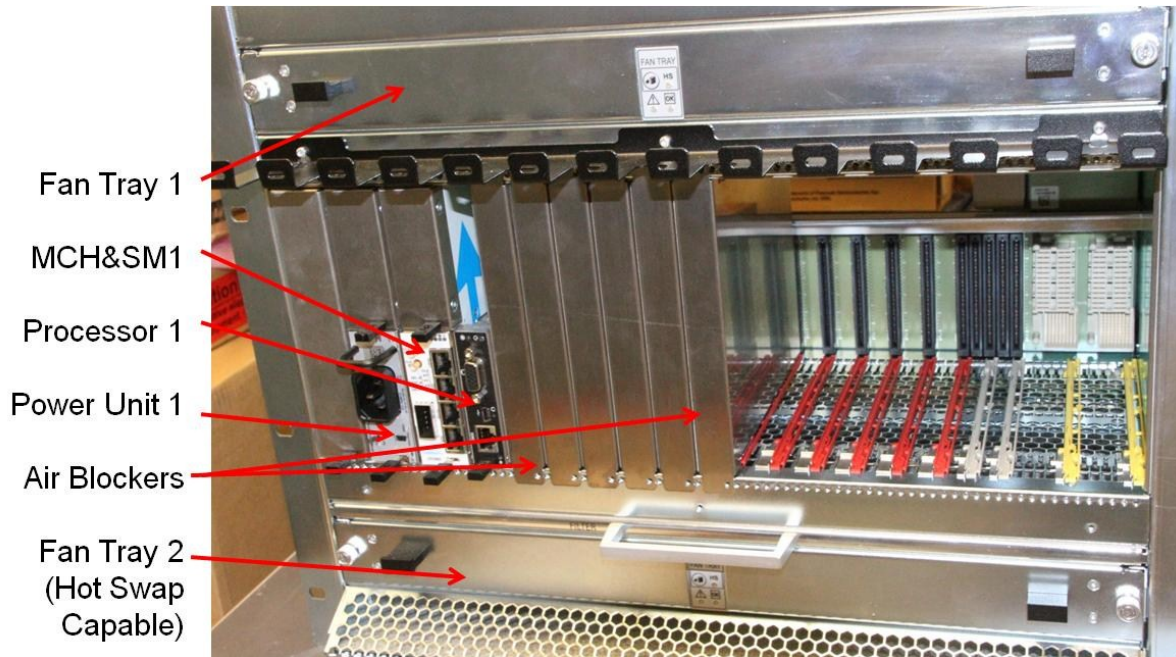


6 Slot Crate  
AMC & RTM  
(Schroff)



12 Slot Crate  
Front-Rear Fan Trays  
(Schroff)

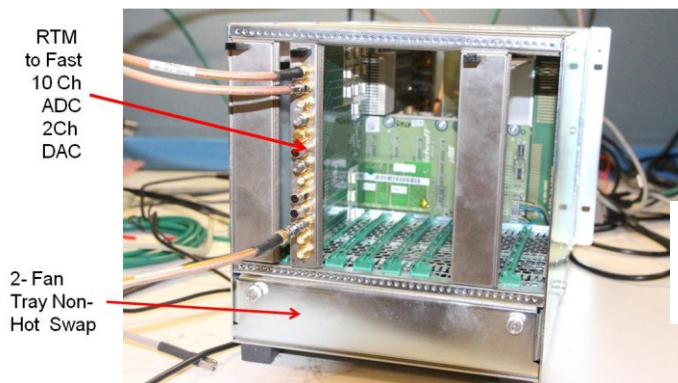
# MTCA.4 Compliant Shelves Operational



12 Payload AMC-RTMs  
 Dual Star Redundant  
 Front View

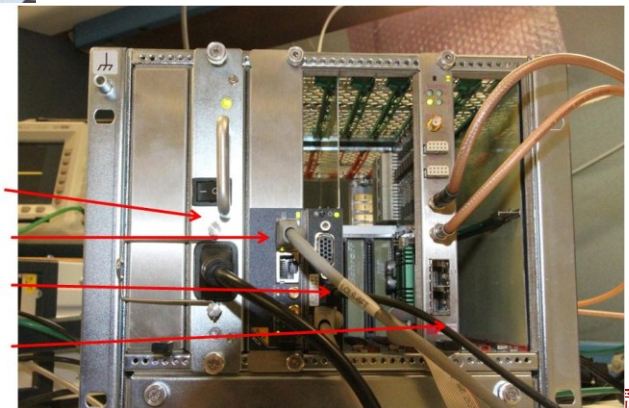


6 Slot Development Unit  
 1-Star Non-Redundant  
 Front View



6-Slot  
 Rear View

1-Star Non-Redundant Backplane  
 300W Power Unit  
 MCH-SM  
 Processor  
 10 Ch Fast ADC-DAC



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## II. Goals & Status of New Physics Standards

# Goals & Status of New Standards

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- 1) Serve expressed needs of a physics user community market segment
- 2) Achieve COTS\* support – commercialization
- 3) COTS in time for emerging opportunities in new accelerators, upgrade of obsolete large accelerator control systems
- 4) Demonstrate broad applicability in accelerators, physics detectors (DAQ), non-physics areas (military, telecom, industrial control, medical imaging...)

# 1.) Addressing Expressed Needs (e.g.)

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- **ILC:**
  - ILC I&C adopted ATCA for technical, cost model
- **DESY XFEL:**
  - LC spinoff project approved, under construction
  - Adopted xTCA as primary I&C solution in 2008 (ATCA, MTCA)
  - Major contributions to standards; many I&C solutions underway
- **ITER:**
  - Studying xTCA for fast feedback, etc. w/ IPFN (prototypes at JET)
- **SLAC:**
  - MOUs with DESY, ESSB & IPFN
  - ATCA: Developed MPP Generic DAQ module; operating in several experiments incl. LCLS1
  - MicroTCA: RF feedback, Interlocks, BPM prototypes funded, underway



## 2.) Achieving COTS Support (MTCA.4)

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- Two Types
  - A. Infrastructure:
    - A. Shelves (crates), Power Modules, Processors, Hub switchers (MCH), 2-wide module hardware (AMC, RTM), Timing AMC, RTM)
  - B. Generic AMCs
    - A. Modules that serve multiple applications through variety of RTMs (ADC-DAC, FPGA, PMC & IP Adapters etc.)

## 2.A) COTS Infrastructure Progress

Infrastructure	Description	COTS Availability
Development Shelf non-redundant	6-payload shelf with PU, integral cooling fans	2 vendors
Station Node Shelf dual star redundant	12-payload slot shelf , hot-swappable fan tray(s)	3 vendors
Modular Power Supplies	12V Power Units (PUs) 300/600/900W	2-4 vendors
Hub Controller (MCH) – full featured for timing needed	MCH Controller w/ integral IPMI shelf manager, hot-swap, access to radial timing option	2 vendors Switches for radial timing lines need development
IO Controller Processor (IOC)	Generic AMC processor running Linux, EPICS	2+ vendors
Timing Module	1 or 2-wide AMC (SLAC needs EVR compatible, needs adaptation)	1 <sup>st</sup> units available (U. Stockholm), <b>need COTS sources (2)</b>

# 2B.) COTS Generic AMC Progress

Generic AMC	COTS Availability	Lab RTM Adapters
10/2 Ch ADC/DAC 16 bit 125 MSPS	1 vendor available 2 <sup>nd</sup> vendor due end FY11	<ul style="list-style-type: none"> <li>• RF-IF down-mixers</li> <li>• BPM adapter</li> <li>• Photodiodes</li> </ul>
4 Ch ADC AMC 14-16 Bit 125 -500 MSPS	1-2 vendors in development	<ul style="list-style-type: none"> <li>• BPM single bunch</li> <li>• BPM multi-bunch</li> <li>• Beam intensity Toroid</li> <li>• Beam Length</li> </ul>
FPGA Virtex/Spartan, FMC optional	1 vendor available	<ul style="list-style-type: none"> <li>• Interlocks ADCs 12 bits, 8 ch @60 MSps, 16ch@2KSps</li> <li>• Wire scanner interface</li> </ul>
AMC Industry Pack Adapter (2-3 IPs)	2 vendors in development	<ul style="list-style-type: none"> <li>• Stepping motor control</li> <li>• Vacuum control-monitoring</li> <li>• Temp control-monitoring</li> </ul>
AMC PMC Adapters	2 vendors	<ul style="list-style-type: none"> <li>• Timing Rx adapter</li> <li>• Frame grabber adapter</li> </ul>

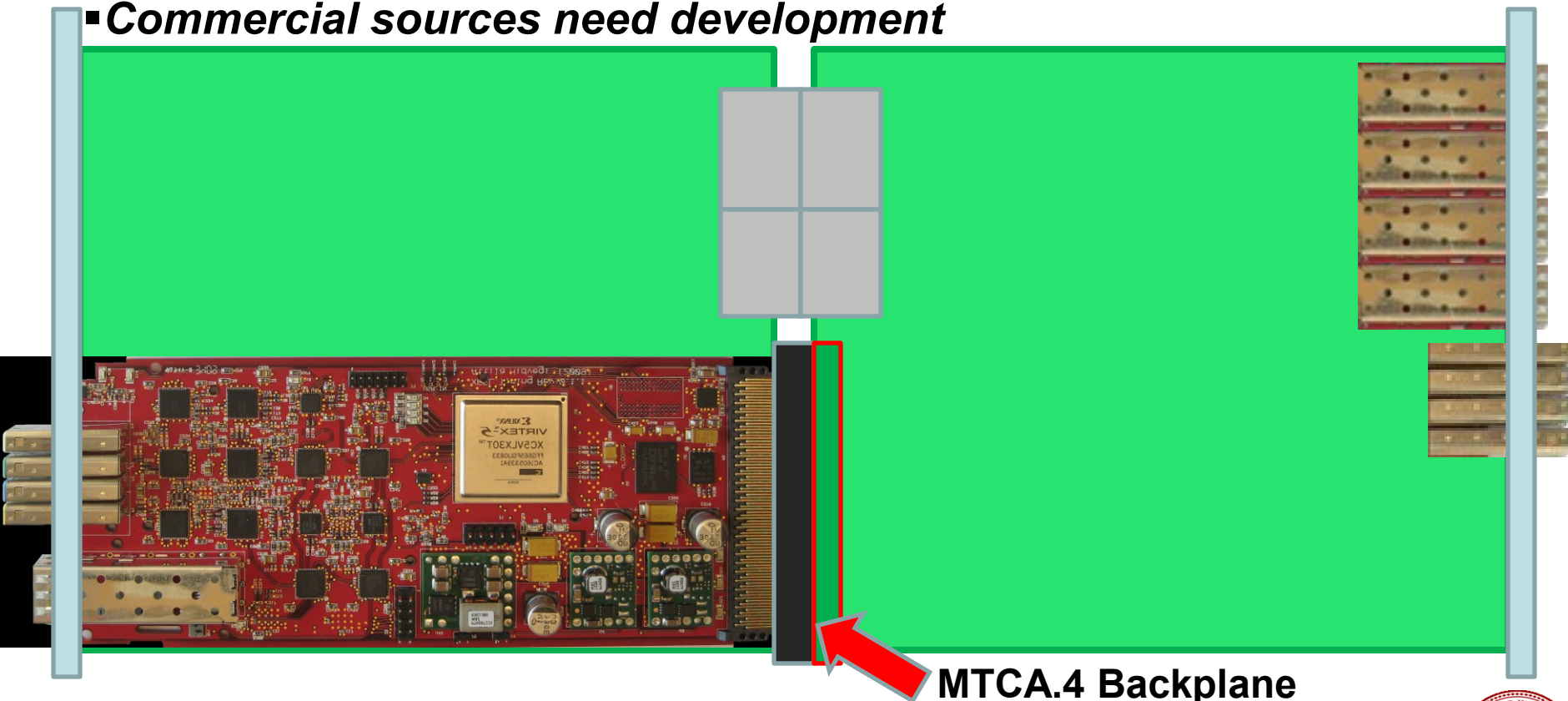
# 3.) *In Time for Emerging Opportunities*

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- Developments achieved (e.g.)
  - New standards functioning in several prototyping initiatives (DESY-XFEL, SLAC-LCLS, ITER, IPFN)
  - Software, firmware standards efforts gaining traction; need stronger user involvement
  - LCLSII next big machine on fast track; will meet targets for demos of LLRF, RF interlocks BPMs by end 2012 (2013 construction start)
  - Beginning collaboration with ESSB/IPFN
  - Other light sources showing interest
- Lone unfinished business item is COTS Timing

# MTCA.4 Timing AMC- $\mu$ RTM 1&2-Wide

- Double-wide design concept in progress DESY-Stockholm University
- Both single & double-wide MTCA.4 compliant
- Double-wide allows rear expansion to multiple receivers
- ***Commercial sources need development***



MTCA.4 Backplane

## 4.) *Demonstrate Broad Applicability*

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- A. Within Physics community:
  - ATCA instantly found use for new detector processing initiatives by SLAC, IHEP, others
  - New IO standard will help developers
  - Early MTCA single & double wide prototypes built for detectors with front panel IO,
  - MTCA.4 opens Generic AMC concept to decouple RTM designs, leverage Generic engineering costs (whether industry or lab), encourage interface standards, *interoperability*

# 4B.) Broad Applicability

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- B. Outside Physics community
  - Industry members urged committee to not label standards as “physics” standards because of perceived broad applicability outside physics
  - One 12-slot shelf vendor designed MTCA.4 10 Gbps backplane channels, higher module power to support enthusiastic *telecom* customers
- Far from being established but signs encouraging

# III. PCMG Lab-Industry Development Model

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- Two main features:
  - 1.) Collaboration on standards development
    - Brings skilled resources from industry to quickly progress into finished product
    - Two years to complete 2 standards with entirely new concepts very fast
    - Cost engineering investment from all players all working toward favorable outcome
    - Committee amazingly knowledgeable and generous with time
    - Requires mutually support both industry & lab goals

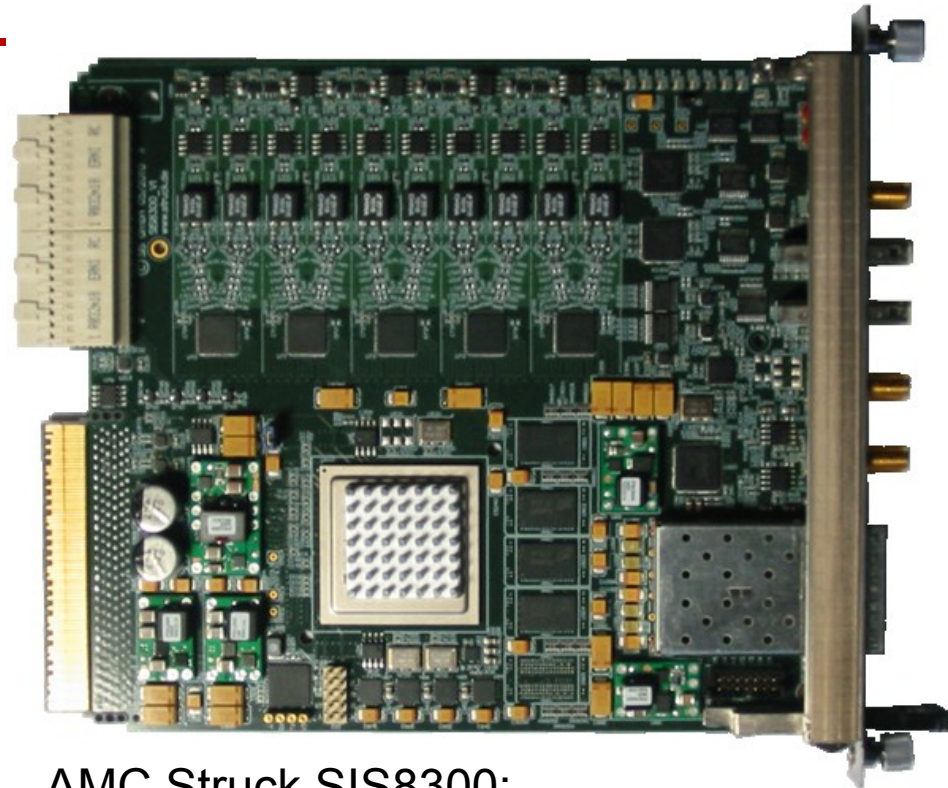
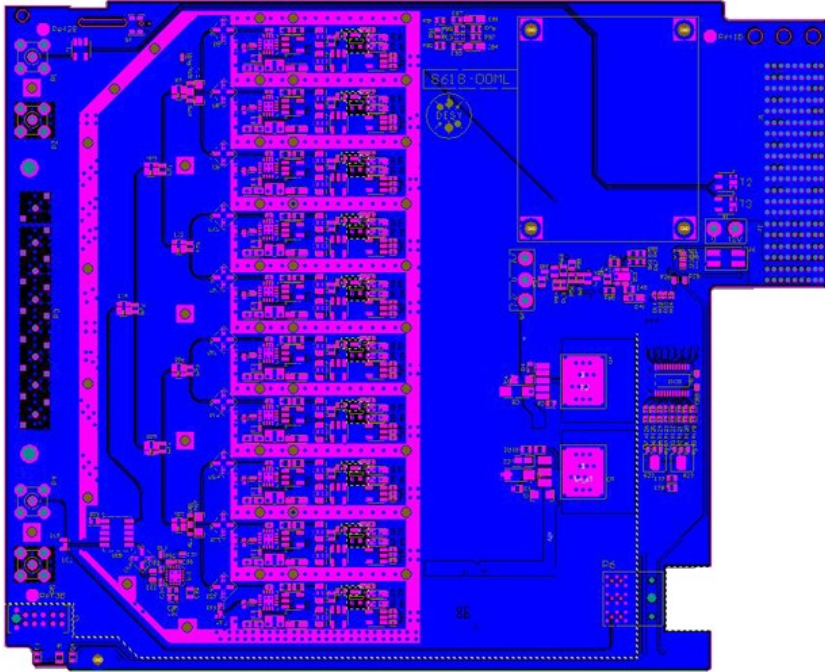


# III. Lab-Industry Collaboration2

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- 2. Collaborating on Generic Module approach
  - Speeds time to finished applications with parallel engineering efforts
  - Reduces costs
  - Leverages designs for whole community benefit
  - Creates new standard AMC-RTM interfaces in process

# Generic ADC-DAC



- $\mu$ RTM:
- 1.3GHz down converter
- Pulse shaper for photo diodes
- BPM interface

AMC Struck SIS8300:

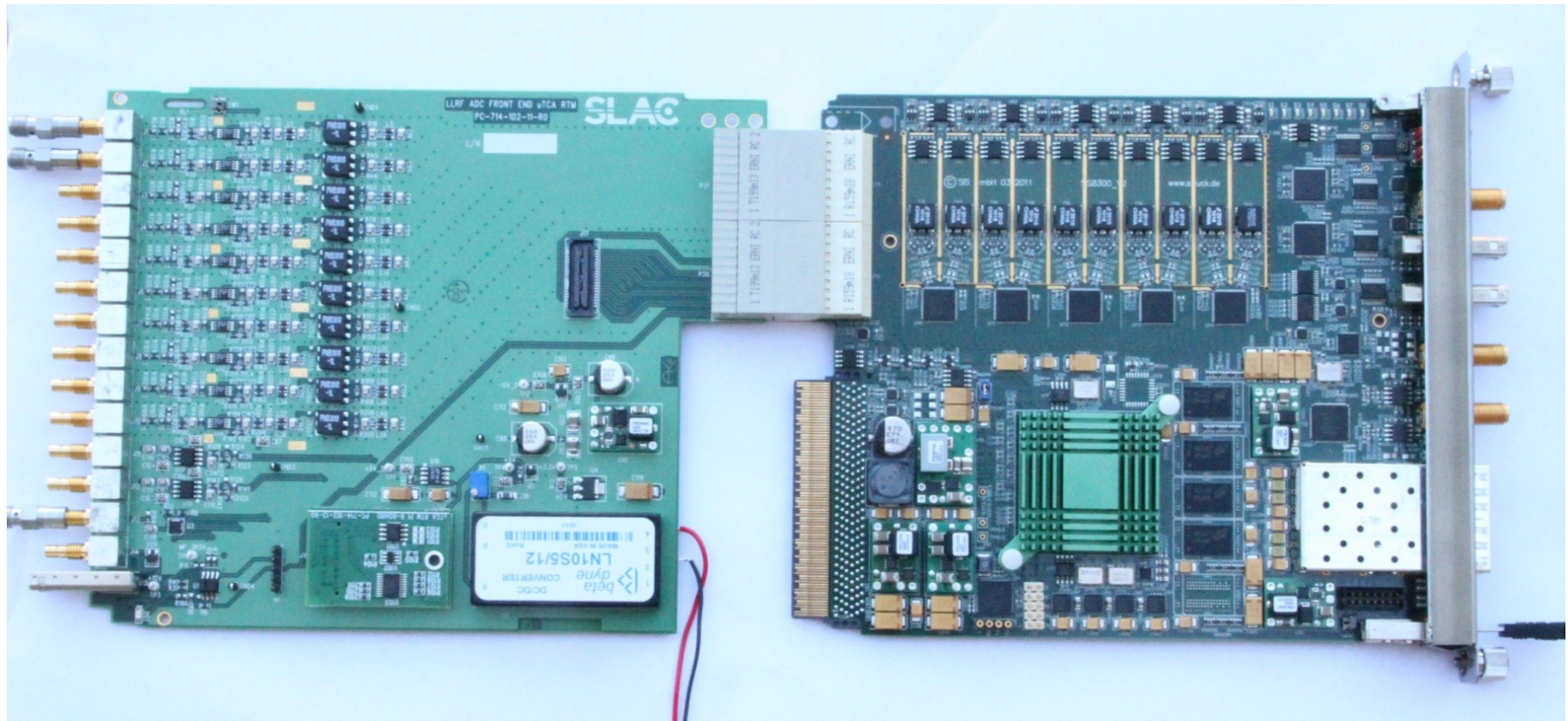
ADC: 10 channel, 16 bit, 125MSPS

FPGA: XILINX Virtex5

DAC: 2 channels

*Courtesy K. Rehlich, DESY*

# SLAC Fast ADC RTM & Struck SIS8300 (RF System Upgrade)



# SLAC Interlock RTM & TEWS651 FPGA (Klystron Interlock Upgrade)



# IV. Conclusions

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- Collaborations critical to meeting standard's goals:
  - “Time to market” for industry, “time to project readiness” for labs; lowering development, production costs
- Continues after development complete
  - In everyone's best interests, even competitors (as in PICMG 250 company consortium)
  - Necessary to service, extend standards into future
  - Should become fixed commitment in Lab culture

# V. Acknowledgments

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- Thanks to Founding Lab, Industry members DESY, FNAL, IHEP, SLAC, Cypress Point Research & TripleRing Technologies; and new member labs IPFN Lisbon, ITER, CERN, LBNL, Sincrotrone Trieste.
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