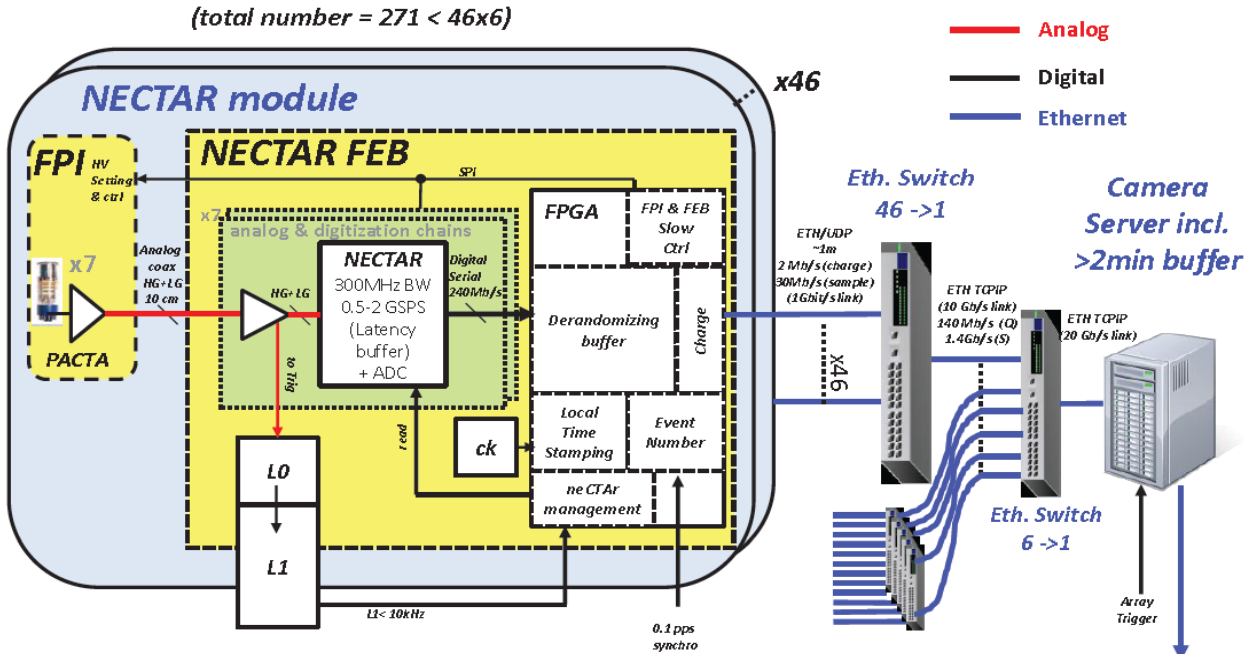
Timing Distribution, Time Stamp and Trigger
Discussion and questions

T.Leflour, A.Masserot, JL.Panazol

Presentation

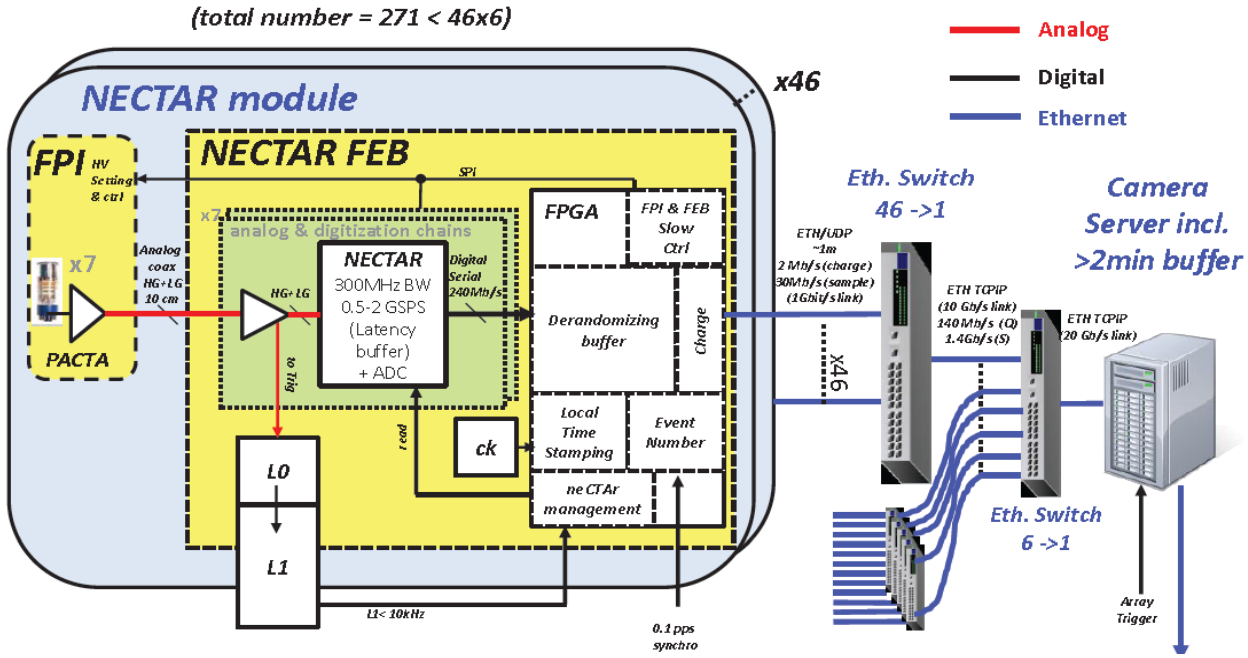
- Nom: Alain Masserot
- Ingénieur en informatique au LAPP
  - Temps réel
  - Architecture de système online et temps réel
- Expérience récente:
  - Virgo: Interféromètre de Michelson(bras de 3Km)
  - DAQ
  - Système de contrôle(asservissement) de l'interféromètre
- Rejoint CTA depuis le début de l'année

NECTArCam : Time stamp and clock



- Local time stamping driven by a free clock @ GHz:
  - function of this timestamp ?
- Event Number:
  - function of the Event number
  - role of the 0.1pps clock ?
  - Who drive the Event number counter ? L0/L1 triggers ?
  - Does the event number could be seen as a global and homogenous timestamp ?

NECTArCam :Global Timestamp and trigger



- Global Timestamp
  - Where the Global timestamp is available ?
  - Who put this global timestamp in the DAQ stream ?
- Trigger
  - Which relationship do we have with the others cameras inside the same array ?
  - Where this relationship is implemented: NECTAr module FPGA , CameraServer ?

CameraServer

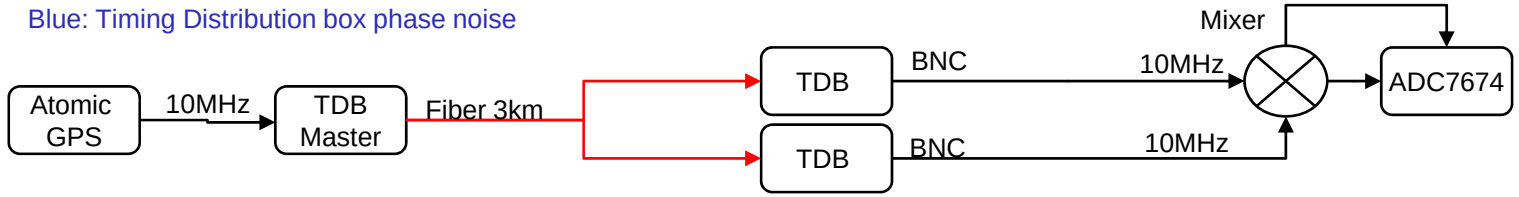
- Input flow: 7*16*2*16*47 *10KHz ≈ 1.68Gbits/s or 0.2GB/s
- CameraServer buffer length > 2min:
  - Where does this constraint ?
  - CPU Memory > 24GBytes
- Which are functions for the CameraServer ?
  - DAQ only
  - buffer waiting for the array trigger decision
  - Others
- Should we keep the CameraServer close the Camera ?
  - for Safety reasons only
  - Others

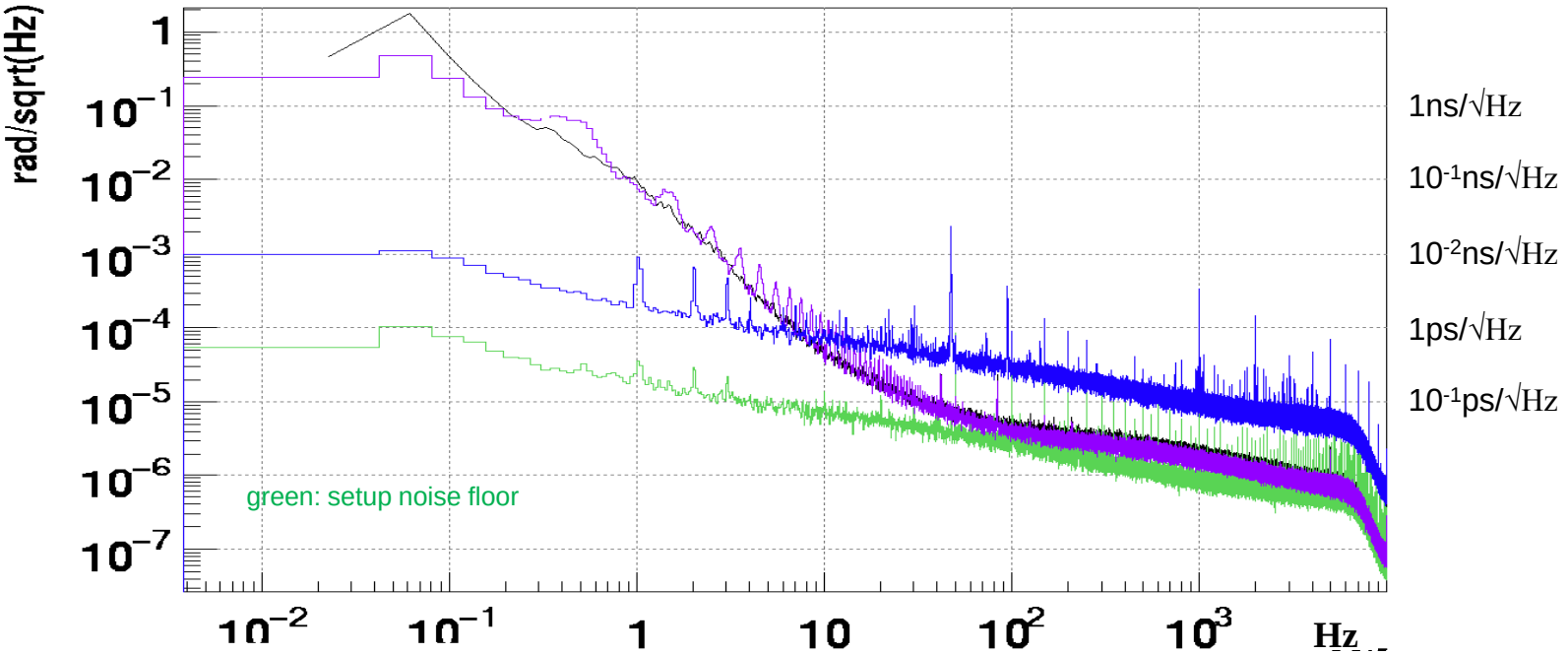
Virgo Timing Distribution

- Base on
  - a central Atomic GPS
  - And local oscillators locked on the 1PPS signal
- Distribute
  - the 1PPS and the GPS second timestamp using the IRIGB format
  - Over 3 Km using multimode optical fibers
- Timing Distribution Box (TDB) to translate from/to copper/optical media
- Fine tuning of the delay propagation (~ 1ns) using delay line
- At each local oscillator site:
  - 100MHz oscillator locked on the 1PPS
  - GPS Timestamp: Second: 32 bits, NanoSecond: 32 bits

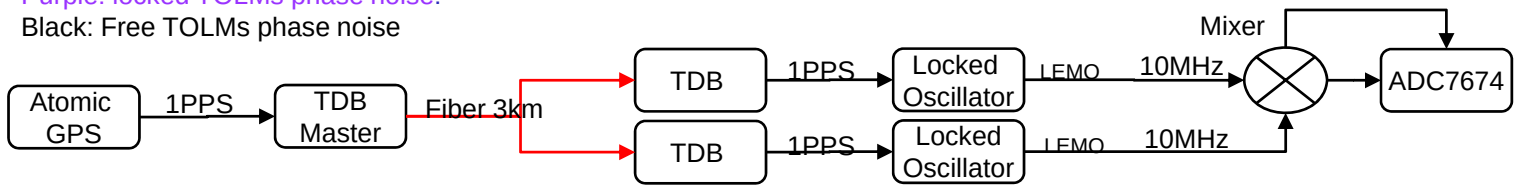
Virgo Timing : phase noise

Blue: Timing Distribution box phase noise





Purple: locked TOLMs phase noise:
Black: Free TOLMs phase noise



NECTArCam properties

- NECTAr chip
  - 2 DAQ channels (low and high gain)
  - 1 Trigger channel
  - Analog memory 1024 cells @ 0.5-2GHz (duration ~1us)
  - ADC 12bits@20MHz
  - 16 samples per event
- NECTar module
  - 7 pixels (7 NECTAr chips)
  - Readout FPGA with Ethernet
  - L0 trigger : based on 7 pixels analog sum > threshold
- NECTar Cam
  - L1 trigger :
    - based on L0 trigger from predefined trigger region in a camera
    - rate <10KHz. It's the camera trigger
  - Ethernet bandwidth: 47*10KHz * 3.584(Kbit/s) ≈ 47*36Mbits/s ≈ 1.68Gbits/s