# ANR SPLAM

## Working Groups 3-4-5 meeting
## LAPP
## Feb. 3rd, 2012

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# Outline

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# What to do for?

Interest of a spark generator:

- Selectable voltage
- Selectable capacitance
- Selectable timing

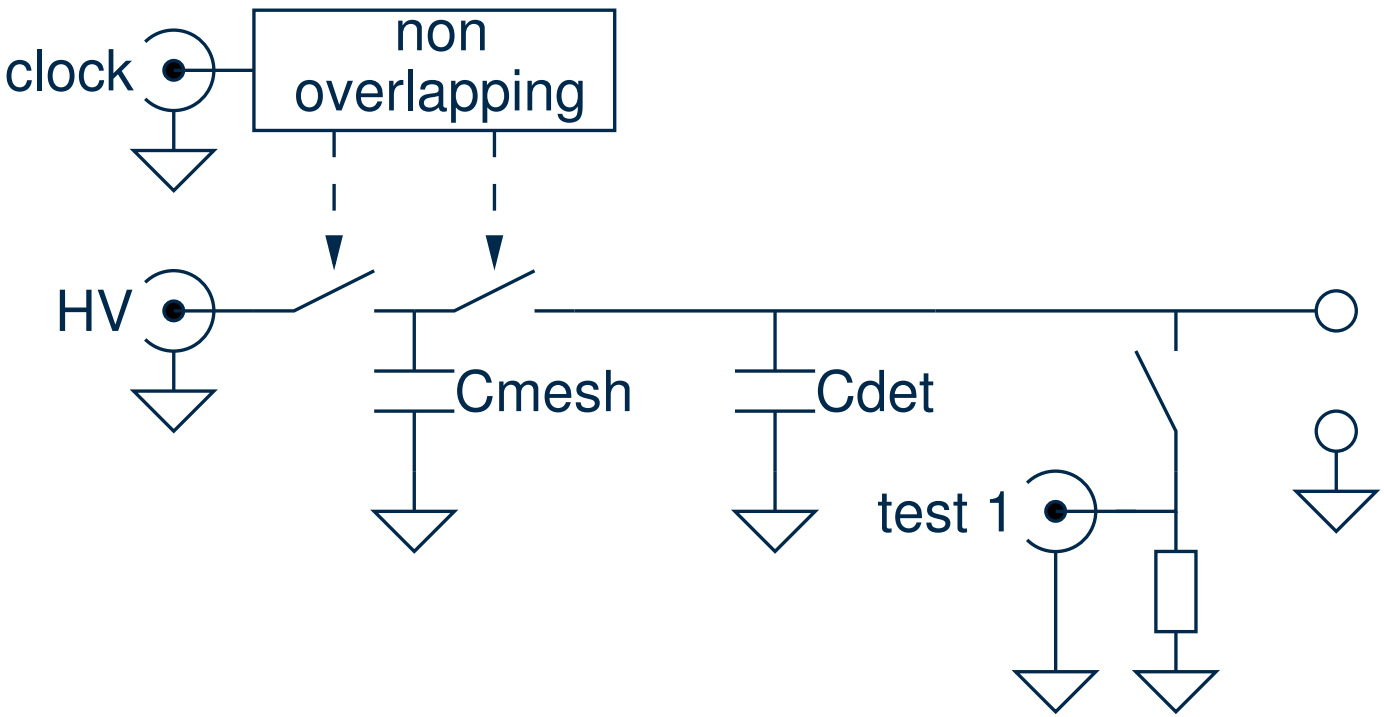
Can generate reproductible sparks!

These sparks are not detector sparks!

But, it help to compare protection structures.

# Principle schematic

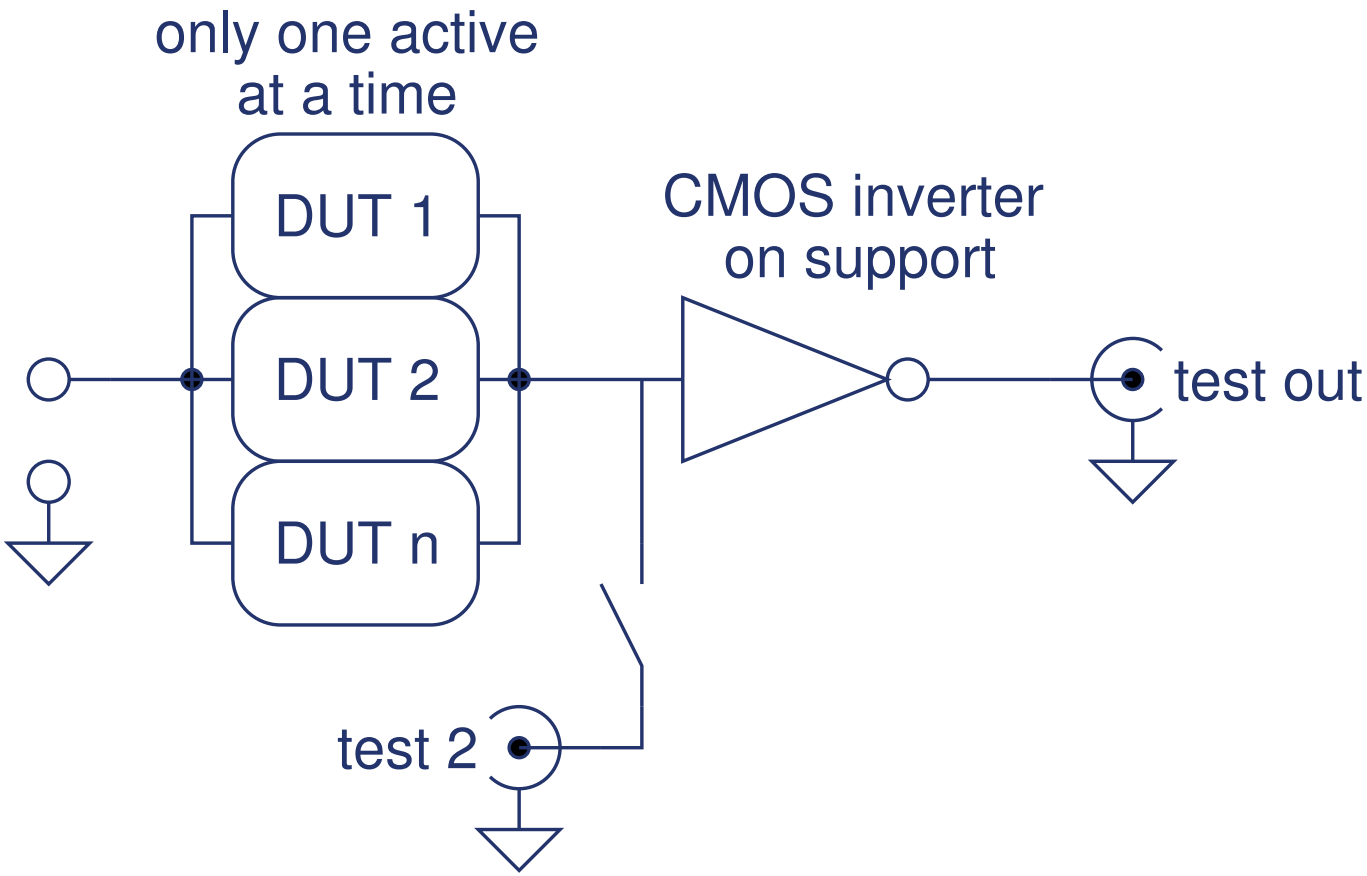
Step 1: Charge capacitor (Cmesh) with DC voltage
Step 2: Discharge this capacitor to Device Under Test (with optional Cdet)
*test 1* input may be used to test if DUT is still working.



# Outline

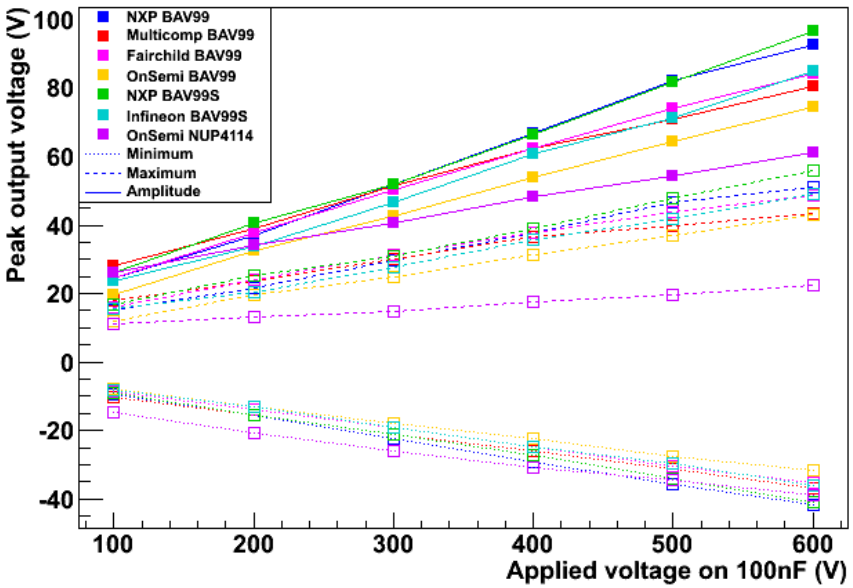
# Test board #1

Compare ability of different structures to protect a commercial CMOS inverter.
*test 2* input may be used to test if DUT/inverter are still working (in conjunction with *test 1* of spark board).

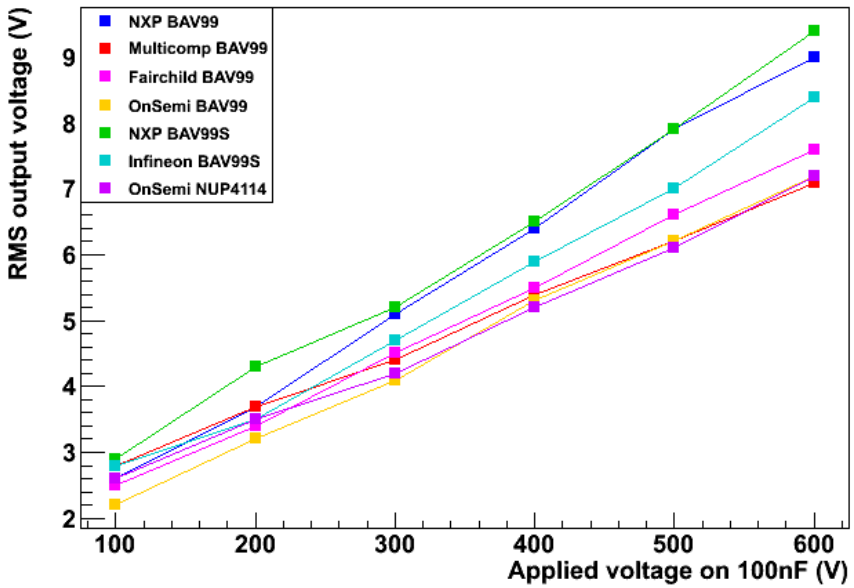


# Result of diodes comparisons (1/2)

A lot of parameter of residual pulses have been recorded. For example:



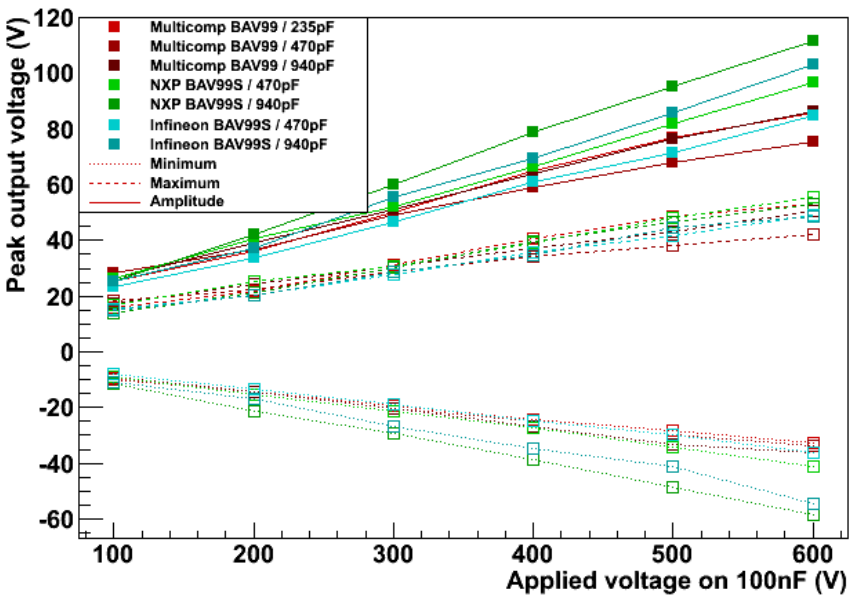

Voltage peak



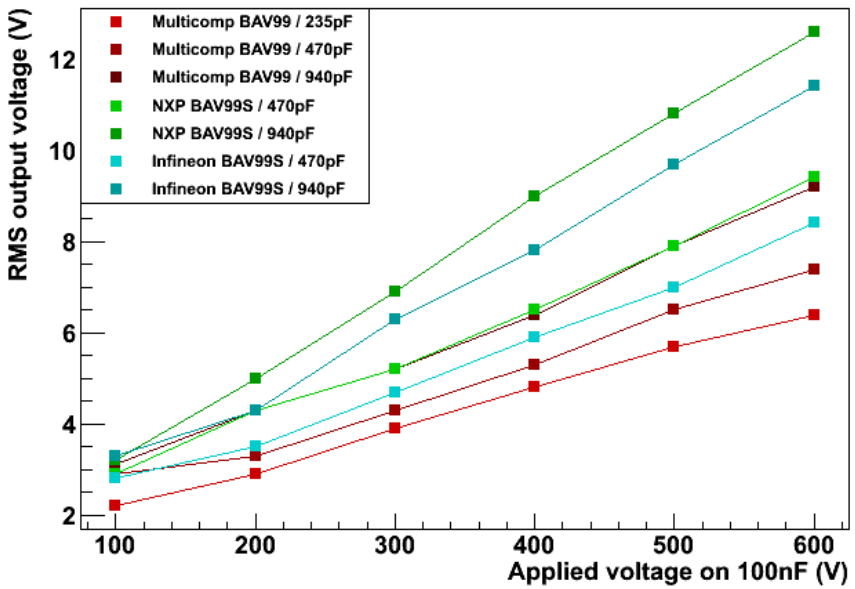

RMS voltage

# Result of diodes comparisons (2/2)

As a function of $C_s$:




Voltage peak




RMS voltage

# Conclusions on firsts comparisons

Conclusions:

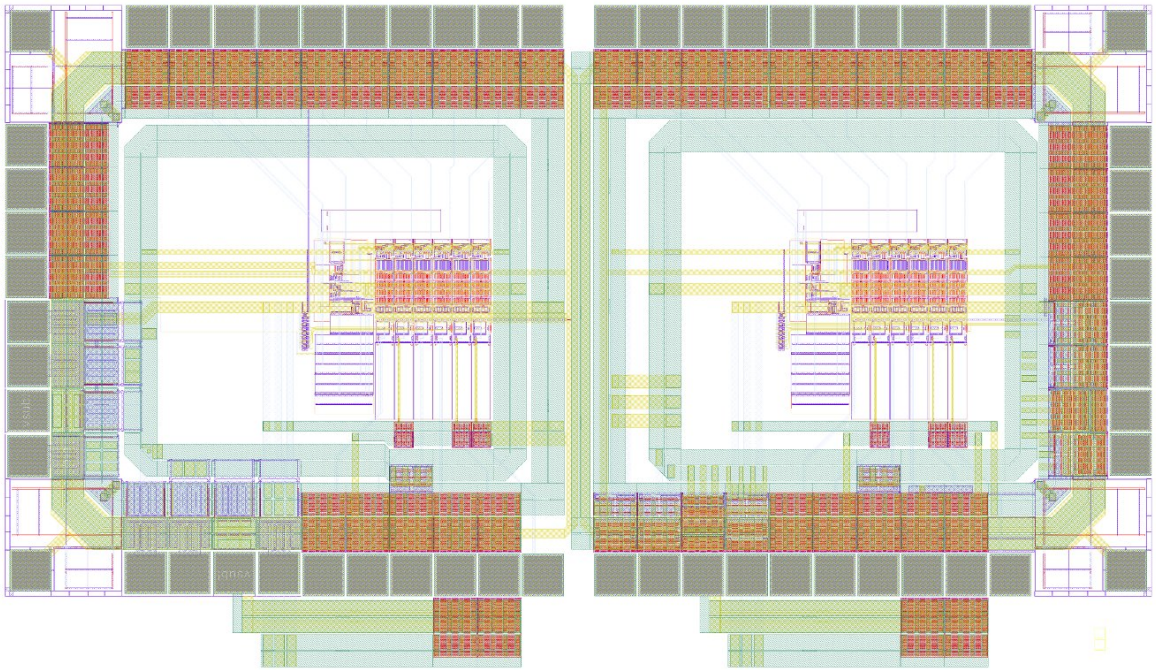
- There are obvious differences between diode manufacturers;
- NUP4114 are better than BAV99: we have updated our design!
- SMD capacitors dielectric other than NPO are not reliable (even high-voltage rated ones);
- Decoupling of diodes is very important for positive ringing suppression.

Still a lot of structures to compare and characterise, including a TOTEM protection chip.

# Outline

# ASIC from LAPP

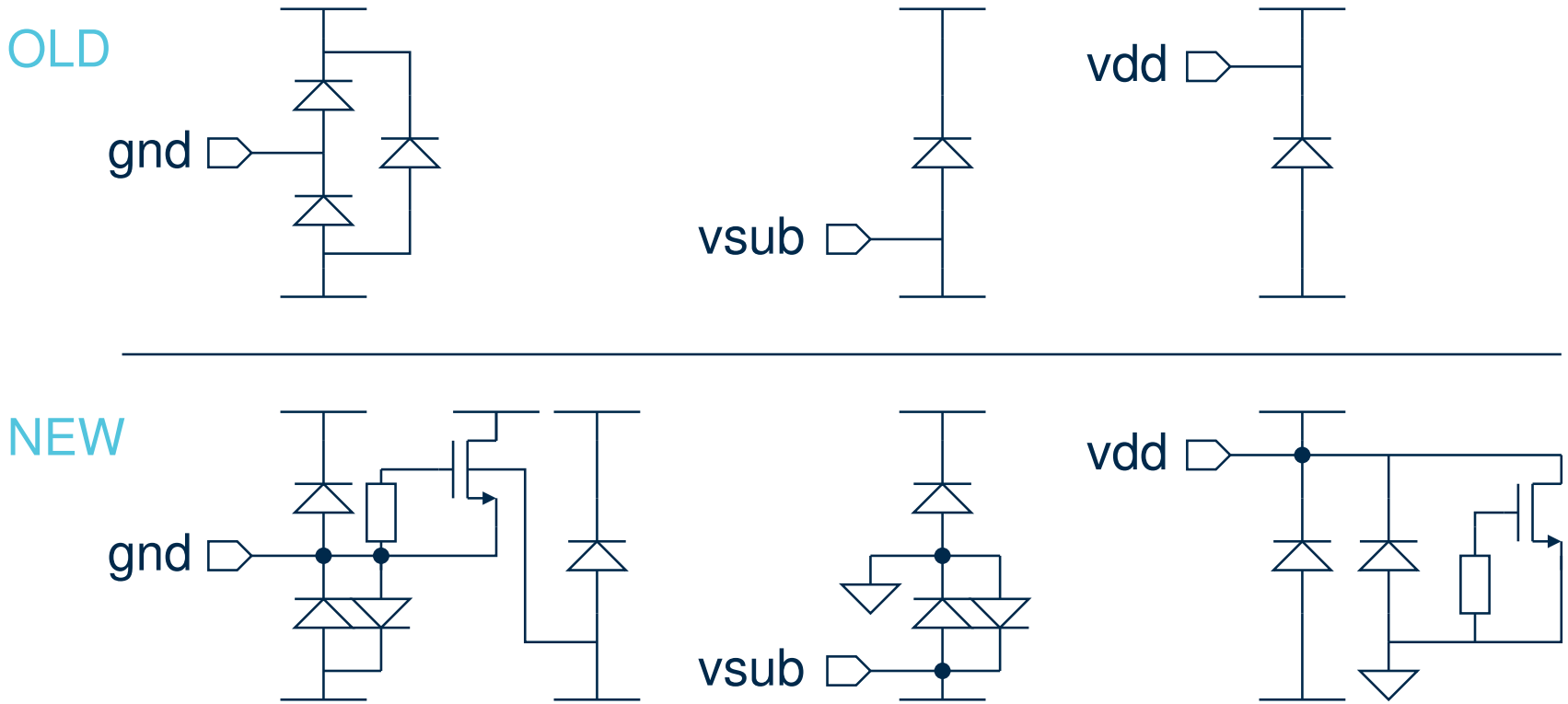
Funded by in2p3. Two savours of power supply pads, 6 kinds of i/o pads for each. Each i/o is connected to a MICROROC PA.



A dedicated testboard has been designed, to be used with spark generator.

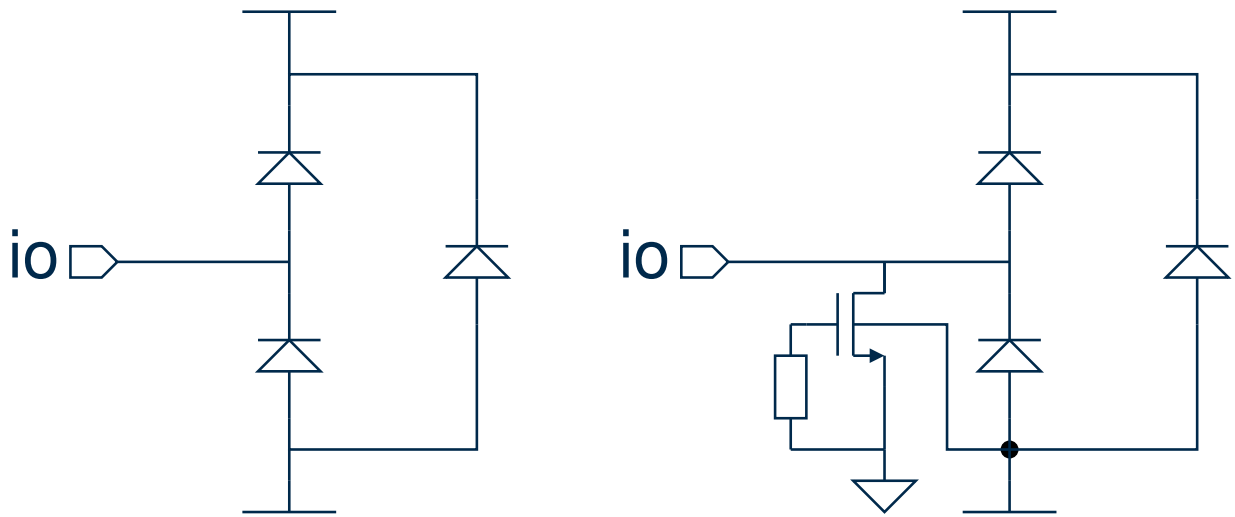
# Power supply

Each power supply pad set consists in 3 pads: vdd, vsub and gnd



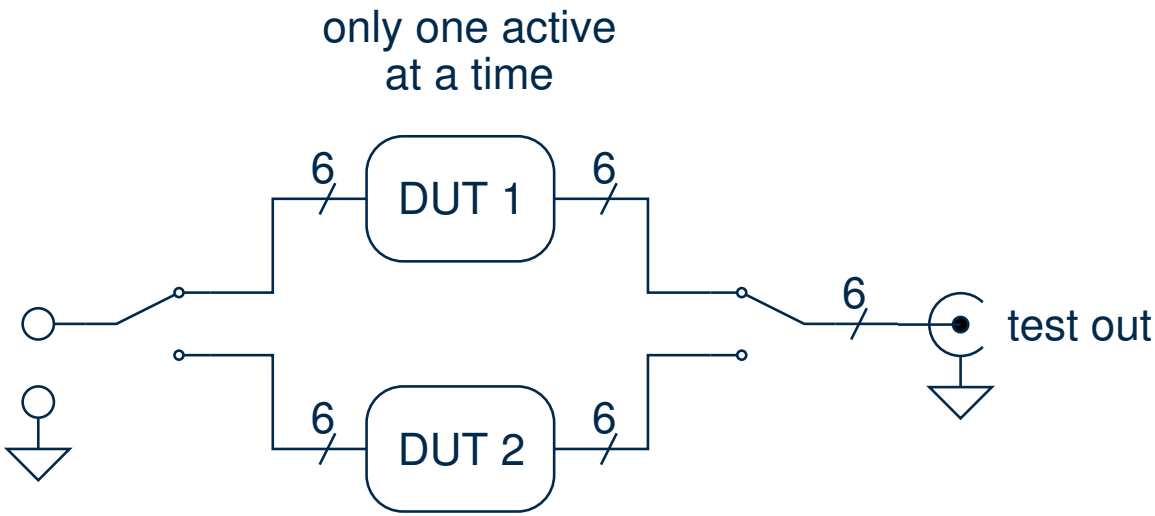
# Input/Output

6 kinds of i/o pads for each. Each i/o is connected to a MICROROC PA. Mainly variation of diode size for 5 inputs, and active protection for 1 input.



# Test board #2

Very simple test board (2 layers)...



# ASIC from CEA

Several hundred of diodes, on two type of silicon (epi and non-epi), seems very similar to Diracs diodes...
Must be packaged, will be compatible with test board #2.

# Outline

# Conclusions

- First results on external passive network
- Integrated electronic protections tests not started... we expect to replace external network with integrated protection
- An other ASIC will be designed this year: ideas, designers and collaborators welcome !